WHITE PAPER

Optimizing High-Speed Connector Models for Channel Design at 56 Gbps and Above

High-speed digital connectors used in Hyperscale Networks require both modeling and measurement correlation to meet the demanding bandwidth requirements of today's internet infrastructure. It is now critical to have high signal integrity throughout the whole channel from mezzanine systems to backplane interconnects to SERDES (serializer-deserializer) chipsets. Emerging applications using 56Gbps and above are requiring new methods of validation, compared to the traditional metrics of BER and eye diagrams, to avoid throwing channel margin away unnecessarily. The Channel Operating Margin (COM) figure-of-merit along with measurement/simulation correlation is becoming a critical part of the design cycle. The analysis of the test cases proposed herein will present an extensive validation of a high-speed connector for differential interconnects working up to 112 Gbps, by providing an in-depth analysis of such component, as a critical portion of the channel. A comprehensive correlation of the connector model to experimental results in terms of thru and crosstalk responses in both time and frequency domains provides a reliable connector model for the subsequent channel design. Comparison of new test methodologies will be shown to accurately predict how to optimize channel performance at today's ultra-fast data rates.

Analyze Multiport s-parameters with Signal Integrity SoftwareIn order to fully correlate and characterize high-speed digital connectors, it is critical to observe crosstalk in not only the time domain, but frequency domain as well.

KEYSIGHT TECHNOLOGIES

Introduction

The ever-increasing demand for faster communication rates beyond 28 Gbps calls for accurate characterization of the channel at the physical layer and the precise evaluation of its performances [1]-[5]. The channel design for chip-to-chip communication over backplanes and copper cables relies on the trade-off of several aspects in terms of physical and electrical constrains. Therefore, accurate prediction of required layout area, channel length and loss, crosstalk control, together to equalization schemes and topologies at both Tx (pre/de-emphasis) and Rx (CTLE and DFE) SERDES is necessary to minimize costs and avoid channel overdesign [6]. Therefore, the design margin for the channel to be beyond the pass/fail threshold should be appropriately evaluated. This channel design and optimization is even more relevant when data rate exceeds 100 Gbps (i.e. 112 Gbps PAM4 based link in the most recent Ethernet developments [7]). The chip-to-chip link over copper cable and backplanes typically employs high speed connectors [1], [8]. The channel engineering process may have control on the chip placement and fan-out, and the backplane interconnect layout up to the connector interfaces. However, the designer usually needs to rely on third party connector data when assembling the channel model for evaluating the overall performances. A reliable channel modeling and the consequent accurate prediction of its operating margin when external resources need to be employed, i.e. in the case of a connector, consists of two main steps. The first one is the validation of the available data (or model), and the second is the in-depth analysis of the connector performances for its reliable use. The aim of this paper is to present the validation of a high speed connectors for differential interconnects working up to 112 Gbps; moreover, the key steps for analyzing the performances of such type of channel components are deeply investigated to assess whether or not it can be reliably applied to the intended channel for chip-to-chip communications over backplanes.

The High Speed Connector

Model description

The sample component that is investigated in this paper is a high-speed connector for routing differential interconnects from/to PCBs [9]. The model provided by the vendor comes from a full-wave simulation (up to 50 GHz) of five differential pairs laid out in close proximity, such that the crosstalk among the pairs within the connector can be taken into account. An overview of the modelled pin pairs is reported in Fig. 1, with the five highlighted (circled) differential pairs. The full-wave model consists of a female/male assembly of the connector, where each connector part is attached to a multilayer PCB for appropriately setting external ports at the stripline cross-section of each pair. The ports are placed 1 mm after the via transition from the top layer (for connector attachment) to the inner stripline layer. Thus, the obtained S-parameter network is characterized by total 20 ports.

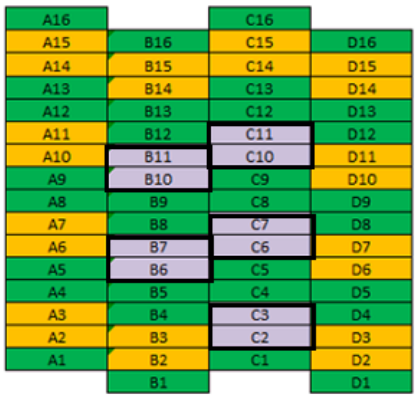

Figure 1. Overview of the connector pin map. The green (dark) pins are grounded, the circled bright gray pins are the pairs with ports set for S-parameter extraction, the yellow (bright gray) pins are terminated signal pins.

Measurement setup

A similar connector male/female assembly is also experimentally measured. However, the access to each pin for connection to the calibrated VNA port is achieved by routing the stripline in a PCB for about 3 in. Then the link reaches again the PCB external layer where a 2.4 mm coaxial connector make possible the connection to a modular vector network analyzer capable of measuring up to 53 GHz stop frequency. An overview of a typical measurement setup is shown in Fig. 2. The scalable VNA allowed a simultaneous measurement of 16 ports, thus one pair (C6-C7) is left floating, as highlighted by the inset in Fig. 2. The measured sample involves the PCBs portions not included in the full-wave mode. In these cases, the de-embedding is a powerful technique to get rid of the unwanted test fixtures.

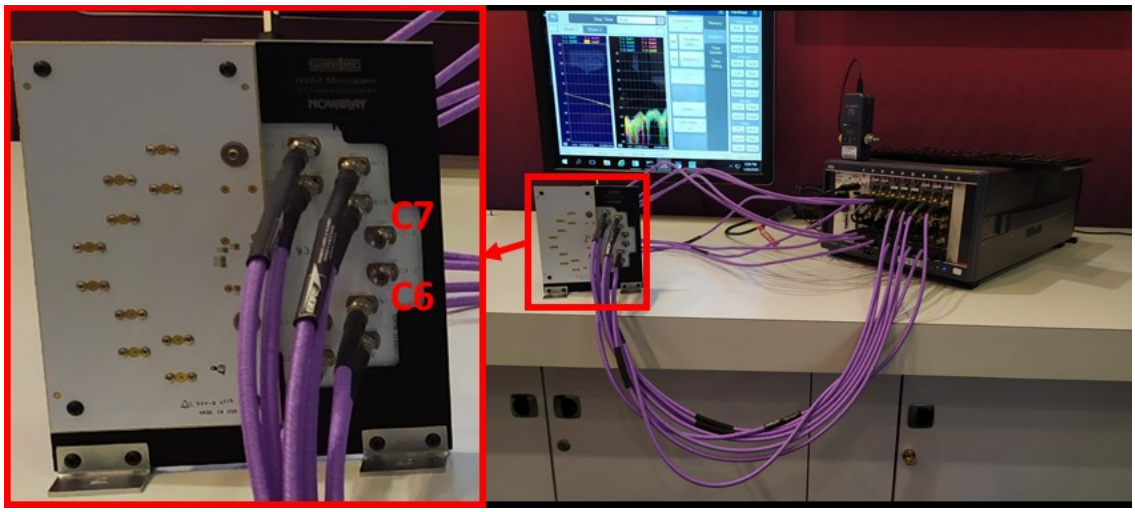

Figure 2. Measurement setup. The pair C6-C7 has not been measured.

Validation and performance evaluation

One of the most relevant parts of the paper concern the validation of the full-wave model described in Section II.A to be able to reliably use it in any high-speed channel design that involves such type of connector. Nevertheless, the validation steps described below are of general application and they can be readily followed when dealing with any type of connector or other types of channel passive components.

In the case considered herein there is not a direct correspondence between the simulated and the measured connector assemblies. The simulation model involves the 5 differential connector pairs highlighted in Fig. 1, and it is based on the female/male assembled connector together to a small portion (1 mm long) of striplines. The measured kit, instead, involves only 4 differential pairs extended about 3 ” from the connector up to the 2.4 mm coaxial connectors, as described in the previous Section II.B. The key step for a meaningful validation is to build an equivalent circuit model for the portion of the measured sample that was not included into the full-wave model. Once this task is accomplished, a one to one comparison can be provided and a deep analysis and validation of the full-wave model can be performed.

The first step consists on identifying the features of the 3” stripline portions and their relative transitions and discontinuities. This task can be accomplished by looking at the TDR response of the measured 16-port network, according to the data reported in Fig. 3. The 2.4 mm coaxial and transitions are made by few transmission line sections of about 100 Ω differential impedances, whereas the 4 measured stripline impedances are very similar (about 95 Ω, with ≈ 5 % variability along the line length) to each other. The impedance at the connector is also expected to be close to 95 Ω with a similar 5% variation. The responses in Fig. 3b tell that the crosstalk among adjacent pairs occurs only at the connector, although it is very small (the crosstalk peak is < 1mV with an impinging step of 1 V). This is confirmed by the timing of the FEXT and TDT responses. The NEXT arises a bit earlier than the FEXT (and TDT) since it begins at the connector input. Therefore, the equivalent hybrid (TL-based model combined to a full-wave connector model) model can be assembled as the one sketched in Fig. 4a. Fig 4b, instead,

reports the port numbering employed to the 16-port networks of both the measured kit and the model in Fig. 4a. It is worth to notice that the port number in the original 20-port network in Fig. 4a has been reduced to 16-port S-parameter by loading the C6-C7 ports with high impedance terminations.

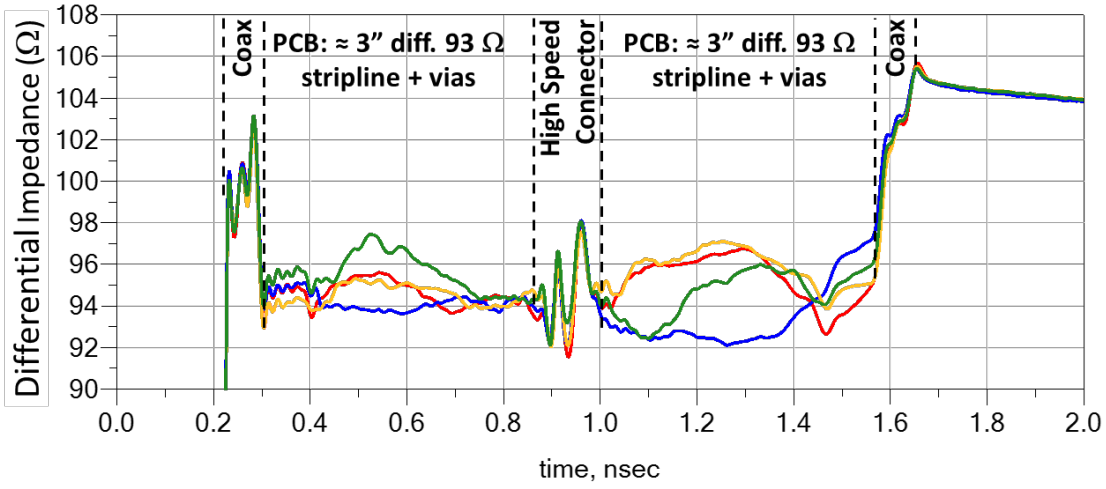

Figure 3a

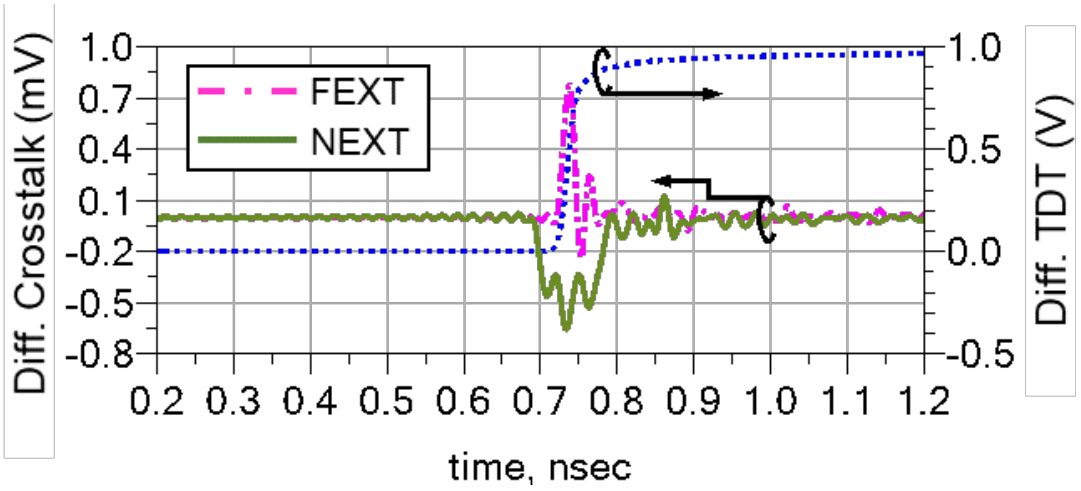

Figure 3b

Figure 3. (a) TDR response of the 4 measured differential pairs. (b) TDR differential crosstalk (between pair B6-B7 and pair B10-B11) and TDT responses of pair B6-B7.

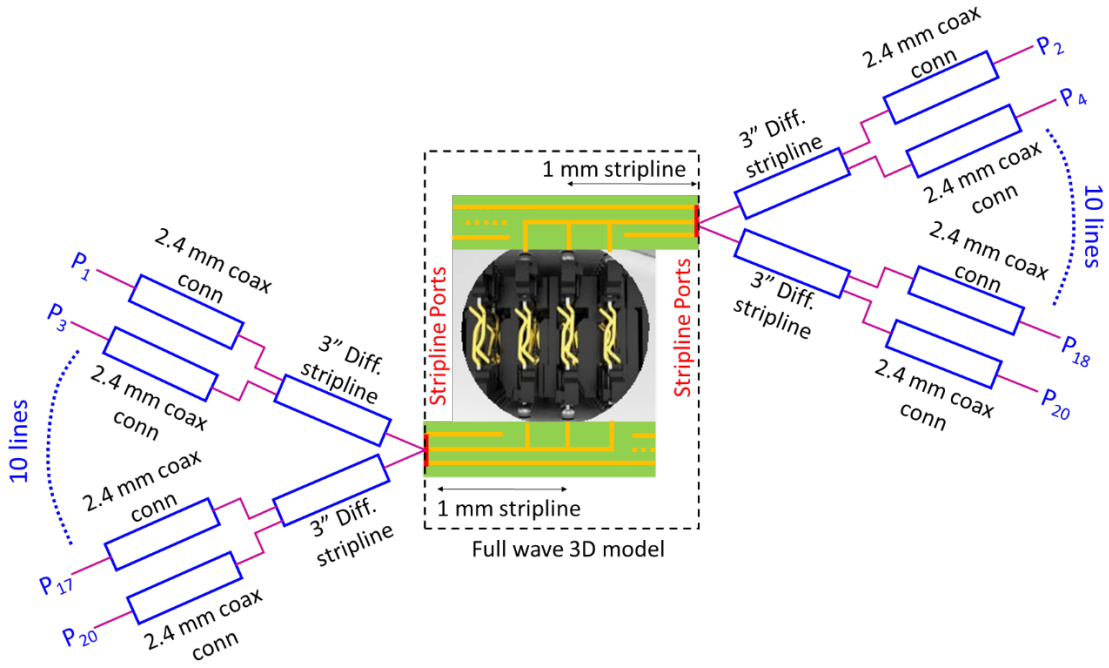

Figure 4a

B12	C11
B11	C10
B10	C9
B9	C8
B8	C7
B7	C6
B6	C5
B5	C4
B4	C3
B3	C2

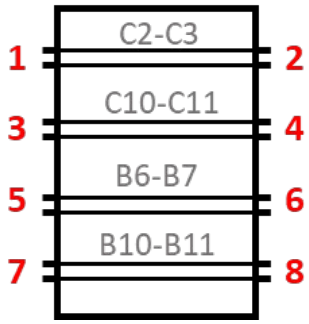

Figure 4b

Figure 4. (a) Schematic overview of the developed equivalent circuit to model the measurement kit. (b) Connector pin map and the corresponding port numbering of both measured and modelled networks

A first analysis is carried out for evaluating the impact of the open-ended equivalent TL-based model connected to pair C6-C7. The comparisons with and without the PCB striplines are provided in Fig. 5, together to the corresponding curve coming from the measured data. When no equivalent TL model with open ends is connected to the connector model at the C6/C7 some discrepancies may occur between modelled and measured data (i.e. the peak at 6 GHz, although of very small amplitude (≈ -70 dB). Whereas, when appropriately connecting such TL sections, the agreement between measurement and simulation is improved.

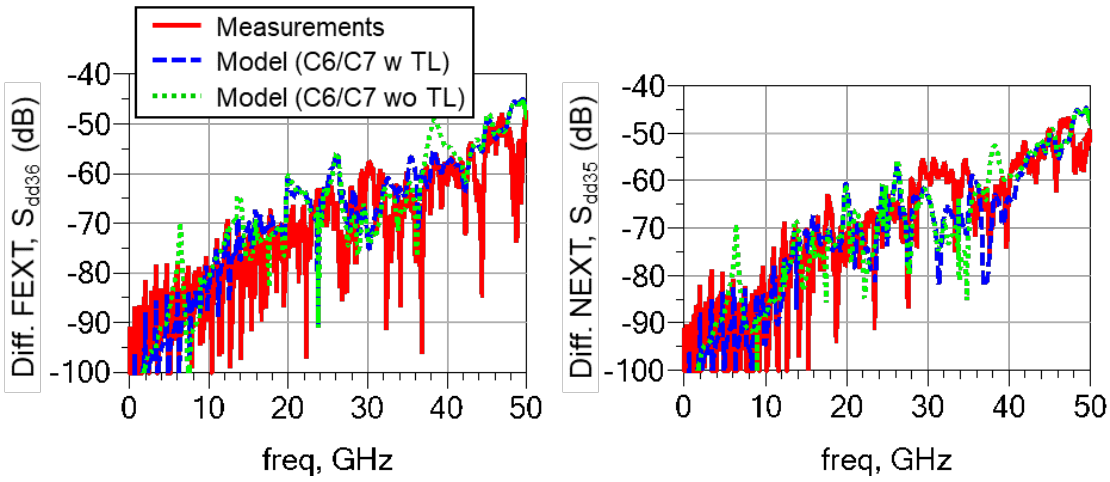

Figure 5. Comparison of FEXT and NEXT between measured and simulated equivalent circuit.

The model is further validated by reporting additional comparisons as shown in Fig. 6, in terms of TDR, crosstalk TDR response, and differential insertion and return losses. All comparisons in Figs. 5 and 6, about the crosstalk, reflection and thru in both time and frequency domains provide a very good agreement between the measured and simulated data, thus comprehensively validating the developed equivalent model. This multi-domain measurement analysis validated also the stand-alone full-wave model of the connector that can be readily employed for any channel design, i.e. a link between two PCBs assembled by such type of connector. Moreover, in terms of absolute value of crosstalk, the connector provides a good isolation among the pairs, of at least -40 dB up to 50 GHz. The model validation and the evaluation of performances is carried out also in terms of output eye diagram at 28 Gbps (NRZ), 56 Gbps (NRZ), and 56 Gbps (PAM4), as shown in Fig. 7. The eye diagrams based on measured connector kit and simulated model agree well;

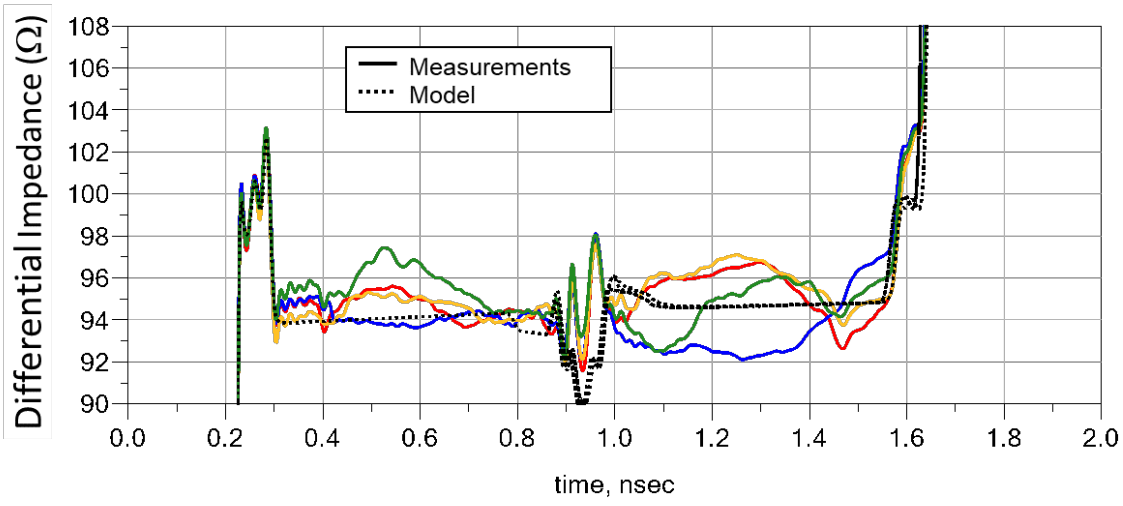

Figure 6a

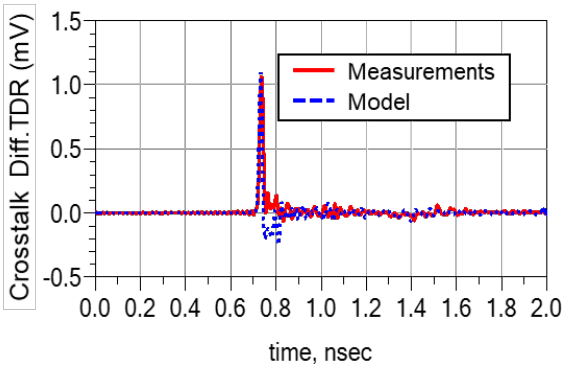

Figure 6b

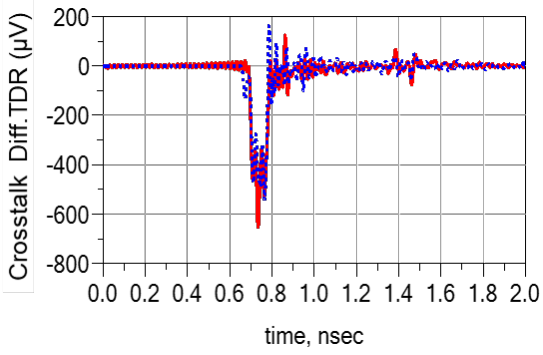

Figure 6c

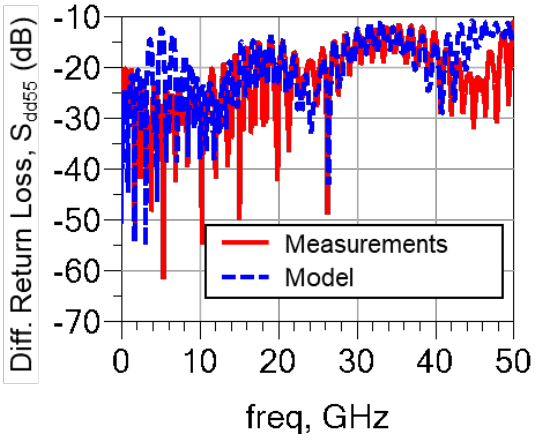

Figure 6d

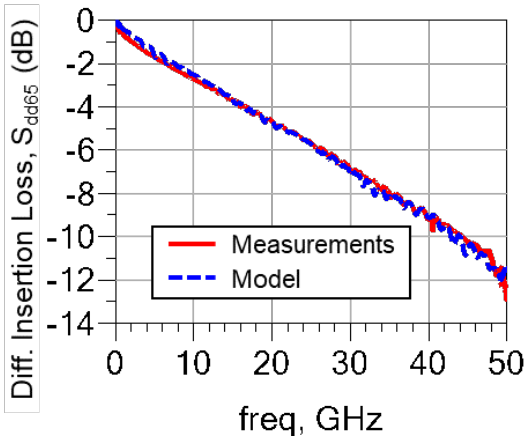

Figure 6e

Figure 6. Measurement vs. simulation. (a) Differential TDR response. Diff. crostalk TDR response between ports P5-P2 (b), and P5-P7 (c). Diff. return loss at port P5 (d) and diff insertion loss at ports P5-P6 (e).

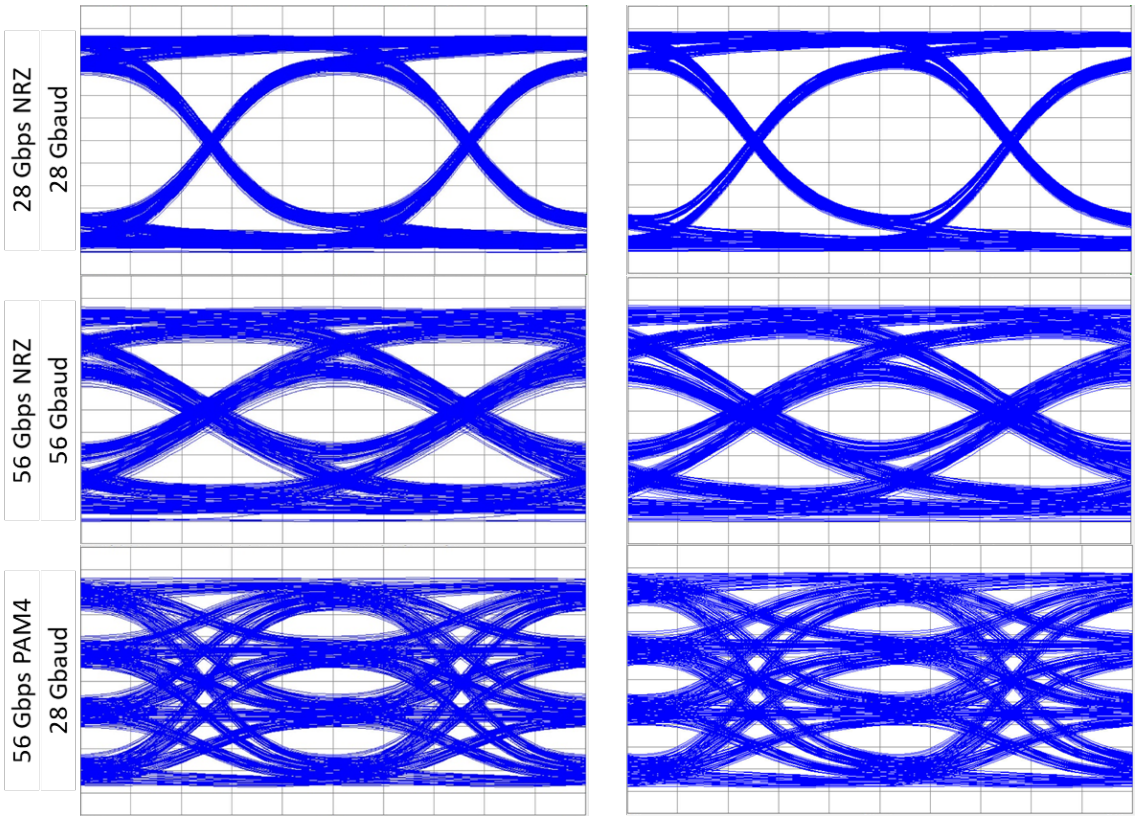

Figure 7. Eye diagrams at different data rates based on (a) measured connector kit, and (b) simulated equivalent circuit.

Channel Design

Channel architechture

The validated connector model is applied herein in a typical chip-to-chip communication scenario where two PCBs (PCB A and PCB B) assembled by the high-speed connector are involved. The channel described in Fig. 8 is developed within a typical simulation environment [11], and it includes the full-wave connector model that has been extensively validated in Section II. This example sets the victim pair at ports P5 (TX)-P6 (RX) – pair B6/B7, with the other three pairs set as NEXT contributions at the receiver side, as sketched in Fig. 8. The differential striplines placed on PCB A and PCB B are designed to have 90 Ω differential impedance, based on the following substrate parameters: Dk = 3.8, loss tangent Df = 0.005, trace width w = 6.2 mils, trace-to-trace spacing $s = 3\times w$. Two channel topologies are analyzed to investigate the impact of both losses (dependent on the stripline lengths L_A and L_B) and crosstalk (mainly dependent on d, since the crosstalk at the connector is demonstrated to be almost negligible):

- Ch1: L_A = 1”, L_B = 4”, pair-to-pair spacing $d = 3\times w$;
- Ch2: L_A = 7.5”, L_B = 4”, $d = 5\times w$;

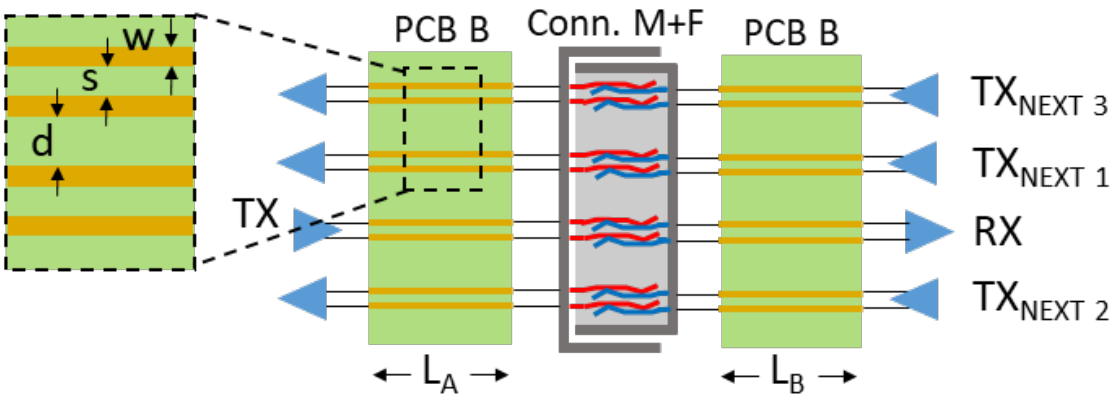

Figure 8. Channel architecture

Evaluation of channel performance

The two channel topologies Ch1 and Ch2 are simulated by using two different methods: first, the typical bit-by-bit transient simulation based on 2^{11} PRBS bit sequence that has been run in [10]. The second method is a statistical approach based on the evaluation of the Channel Operating Margin (COM), as defined by [12]. Both simulation methods included the same three crosstalk topology shown in Fig. 8, as well as driver noise and jitter whose amplitude is set by the COM channel configuration. According to the eye diagrams in Fig. 8, Ch1 may be implemented up to 28 Gbps, whereas Ch2 fails at all bit-rates due to the larger losses (longer PCB A striplines, L_A = 7.5”). However, when evaluated by the COM algorithm at the highest bit-rate (112 Gbps PAM4), both channels provide a COM value above the threshold of 3 dB, as defined by the IEEE standard for chip-to-chip communication over a backplane [7], 4.526 and 3.836,

respectively. Although the standardized procedure for COM evaluation takes into account a typical package model for both TX and RX, thus further increasing the channel losses, it is able to effectively incorporate and optimize the active equalization (pre/de-emphasis at the driver side, Continuous Time Linear Equalizer - CTLE and Decision Feedback Equalizer - DFE at the receiver side). The eye diagram standard metrics for high speed digital channels is no longer applicable for data rate exceeding 28 Gbps, where equalization is strictly required for achieving a functional channel.

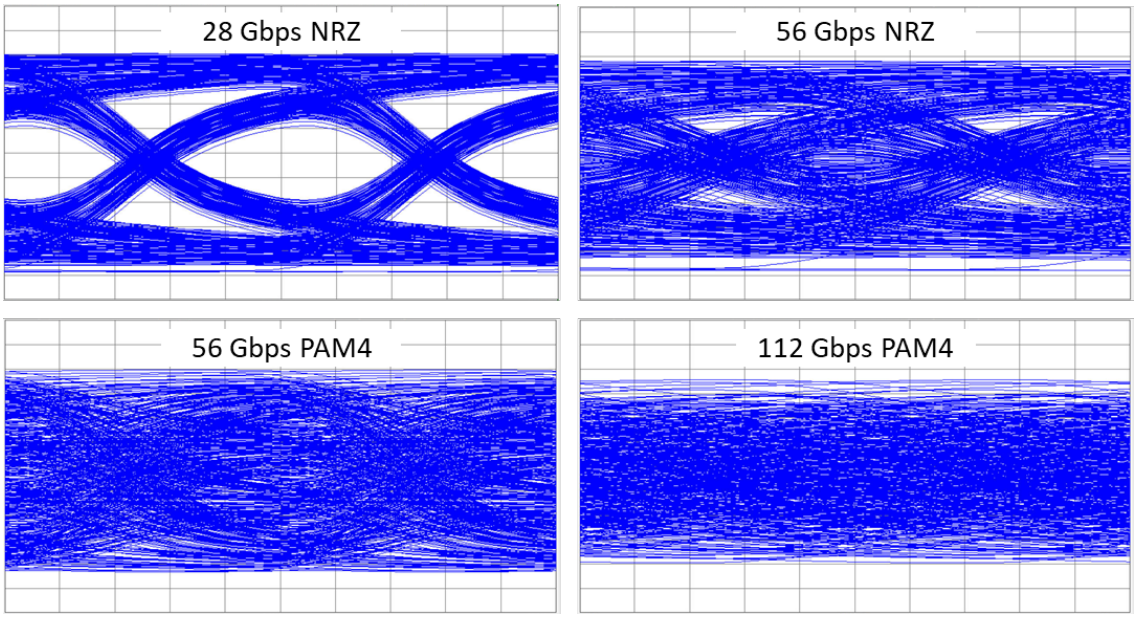

Figure 9a

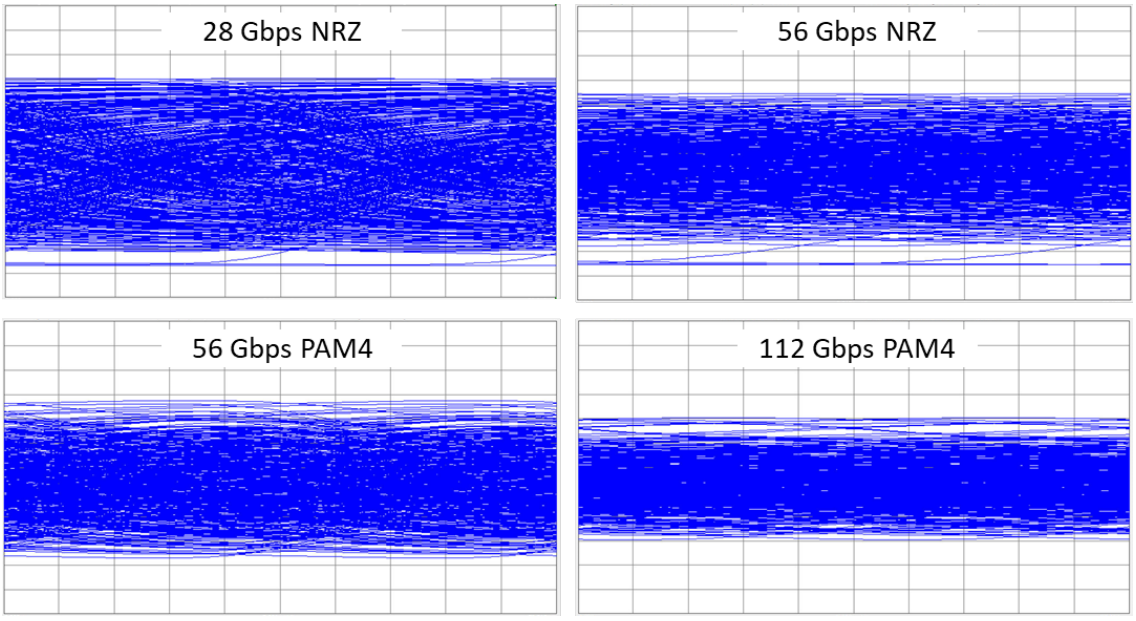

Figure 9b

Figure 9. Eye diagram evaluation of (a) Ch1, and (b) Ch2.

Conclusions

This paper has shown that accurate modeling is still useful to predict actual channel behavior, however, time or frequency domain measurements alone are not enough to qualify a channel capability. An overview of the steps to perform a deep validation of a connector model aimed at ultra-fast data-rate applications is provided, in terms of connector thru and crosstalk responses in both time and frequency domains. The described process can be effectively applied not only to the standalone connector, but also to more complex assemblies as well as to the complete channel. Once the channel is correctly modeled, the SERDES equalization and package parasitics need to be also considered to verify overall performance and standard compliance. The IEEE 802.3, OIF, and other forums are now adopting the Channel Operating Margin (COM), a Matlab script, to evaluate channel compliance for a given BER. The COM script takes into account the impairments such as, insertion loss, x-talk, chip noise, package dimensions, etc. and evaluates them in conjunction with the embedded SERDES equalization capabilities such FIR at the transmit, and CTLE and DFE at the receiver. In summary, newer higher speed links require an overall physical and electrical integral evaluation to reliably predict an acceptable channel BER performance.

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