Take the Mystery Out of Digital Testing

HOW TO PREP FOR 6 EMERGING TECHNOLOGY STANDARDS

KEYSIGHT TECHNOLOGIES

INTRODUCTION

Take the Mystery Out of Digital Testing

Each day, most of us indulge in internet streaming content – we watch funny animal videos, stream movies and TV shows, share videos and selfies. As every high-speed digital designer knows, the explosion of data-rich content, uploads and downloads, has created demands for more memory and higher transfer speeds. And the demand for more memory and greater speed continues to grow.

These demands drive new technology innovations with shorter development cycles than ever before. Achieving faster development cycles becomes increasingly challenging as faster speeds and low power requirements shrink design margins.

Don’t risk falling behind or getting caught with unexpected test challenges as you design the next generation of technology. This eBook will prepare you for the challenges ahead; use it as a guide to stay up-to-date on current and future digital standards.

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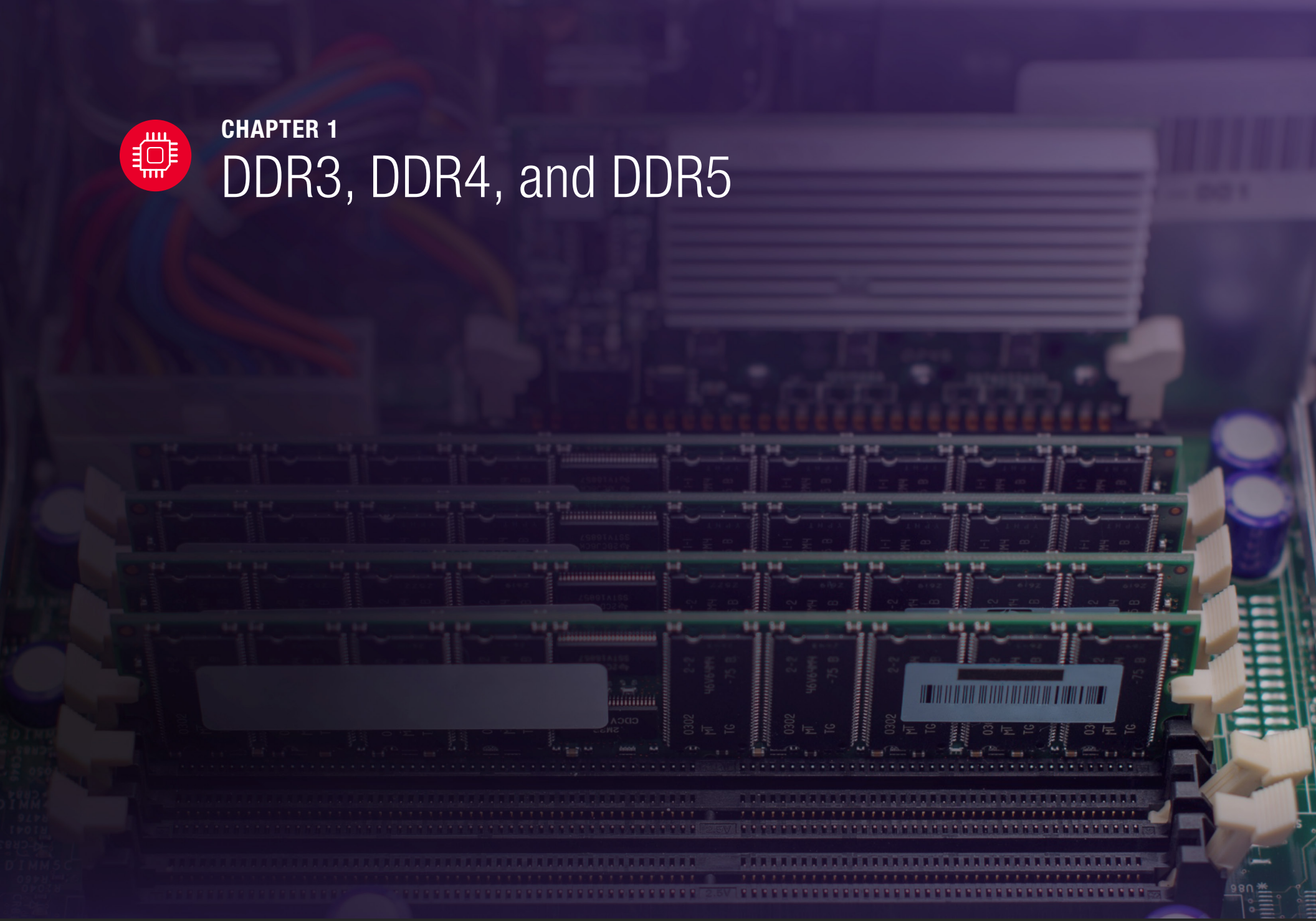


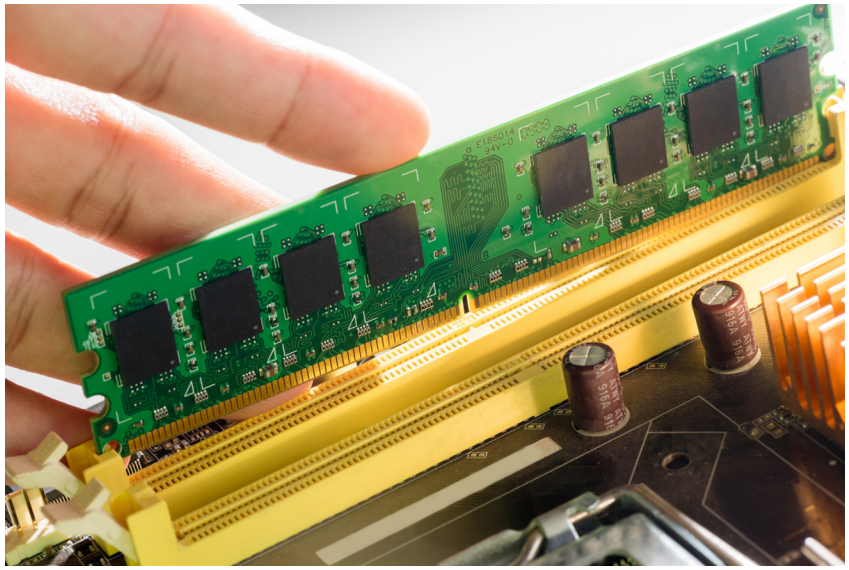
CHAPTER 1

DDR3, DDR4, and DDR5

CHAPTER 1

DDR3, DDR4, and DDR5

DDR (double data rate) is a memory chip technology whose development is primarily driven by servers within data centers. These data centers, as the hub of all data, have the greatest need for modern memory technology because they must meet the constant demand for lower power requirements, higher density for more memory storage, and faster transfer speeds. As servers drive the demand for next generation DDR, consumers benefit when existing and legacy generations become affordable. As they decrease in price, they make their way into our PCs and laptops.



The following table demonstrates how speed has doubled with each generation of the technology along with a decrease in voltage requirement and increase in memory. The standards body, Joint Electron Device Engineering Council (JEDEC), also added cyclic redundancy checks (CRC) and on-chip parity detection with the release of the DDR4 standard to improve data integrity by adding extra command and address transfer verification.

	Speed	Voltage	Max memory
DDR3	800 – 2133 MT/s	1.5 V	128 GB
DDR4	1600-3200 MT/s	1.2 V	512 GB
DDR5	6 GT/s	1.1 V	1TB

How You Can Prepare

The most common signal integrity challenges found in DDR designs are timing issues with the memory controller, so you'll need to adjust the timing between your board and memory controller. If you are testing DDR3 for timing issues, you can typically use set-up and hold-time measurements to verify the timing of your device. If you are testing DDR4 or DDR5 for timing issues, you should create a mask based on the standard's margin and tolerances for random jitter and bit error rate.

Additionally, DDR5 often requires equalization techniques to open the eye and correct for signal degradation through the channel. A high-bandwidth oscilloscope is the perfect tool to help with this testing. Oscilloscopes validate and debug the signal integrity of the signals (including eye size, rise and fall times, and power integrity), perform compliance testing, and apply equalization.

Data corruptions is another challenge with DDR designs. They can be caused by signal integrity or functional issues. If caused by signal integrity issues, the oscilloscope can be used as mentioned above.

Functional issues can result in data corruption and system crashes when memory devices do not receive the correct commands in the proper sequence or within specified timings. When testing for functional issues, use a logic analyzer. Logic analyzers are used to debug and validate the functional performance and protocol compliance of memory systems.

LEARN MORE

Learn more about DDR design and simulation, physical layer test, and protocol validation on the High-Speed Digital Design Double Data Rate (DDR) Memory webpage.

Recommended Test Equipment and applications for DDR:

- UXR-Series Oscilloscopes
- MXR Series Oscilloscopes
- U4164A Logic Analyzer
- Logic Analyzer Software B4661A
- D9010HSPO High Speed Protocol Software Bundle

CHAPTER 2

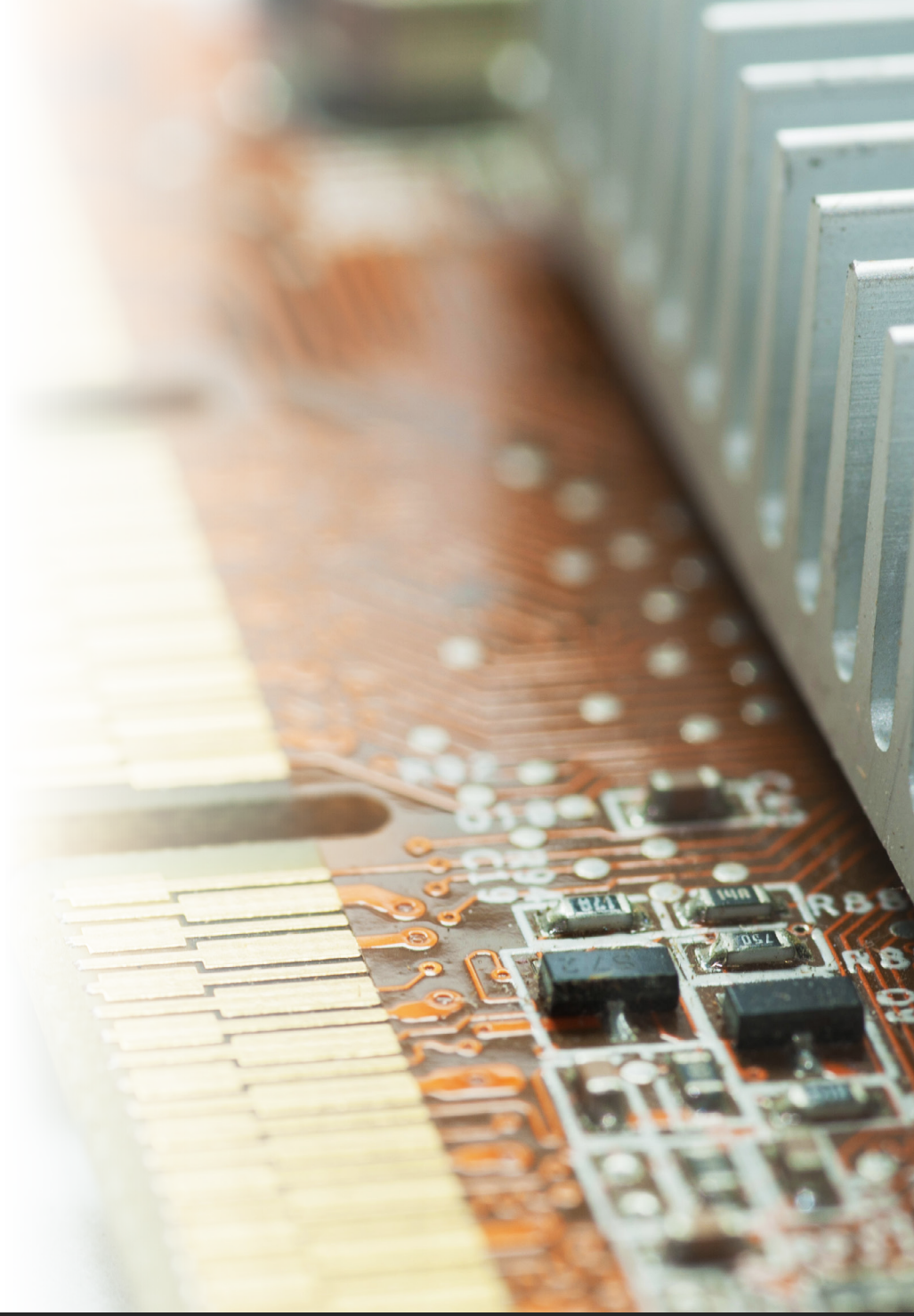
PCI Express 3, 4, and 5

CHAPTER 2

PCI Express 3, 4, and 5

The Peripheral Component Interface Express (PCI Express® or PCIe®) standard extends the functionality of computers to allow for the addition of networking cards, graphic cards, and other peripheral interfaces. This standard is a high-speed, differential, serial I/O technology. The PCI Special Interest Group (PCI-SIG®) defines the PCIe standard. Each generation of PCIe doubles the speed of the previous generation, meeting the growing consumer demand for speed:

- PCIe 3 = 8GT/s
- PCIe 4 = 16 GT/s
- PCIe 5 = 32 GT/s



How You Can Prepare

Because PCI was originally developed to support high-volume manufactured computers, the material cost associated with PCI designs was low. However, with increases in speed, the main design challenges are channel attenuation and reflections. Therefore, not only have development costs gone up, but test margins and channel length have decreased. PCIe 3.0 circuit traces can run up to 20 inches. PCIe 4.0 trace length is typically 10-12 inches. The trace length will be even shorter for PCIe 5. This will require you to not only reduce channel lengths within your design, but also upgrade to superior materials to reduce the effects of the channel, meaning you will need to make design changes at the silicon level.

To test a PCIe 5.0 transmitter, consider using a real-time oscilloscope with a minimum bandwidth of 32 GHz and high-signal integrity to ensure your signals are not distorted by your test equipment. When validating new silicon, you want to measure the transmitter output of the integrated circuit as close to the output pins of the device as possible. You will need to de-embed the loss attributable to any breakout channel between the balls of the package to the connectors used to attach the test fixture to your oscilloscope.

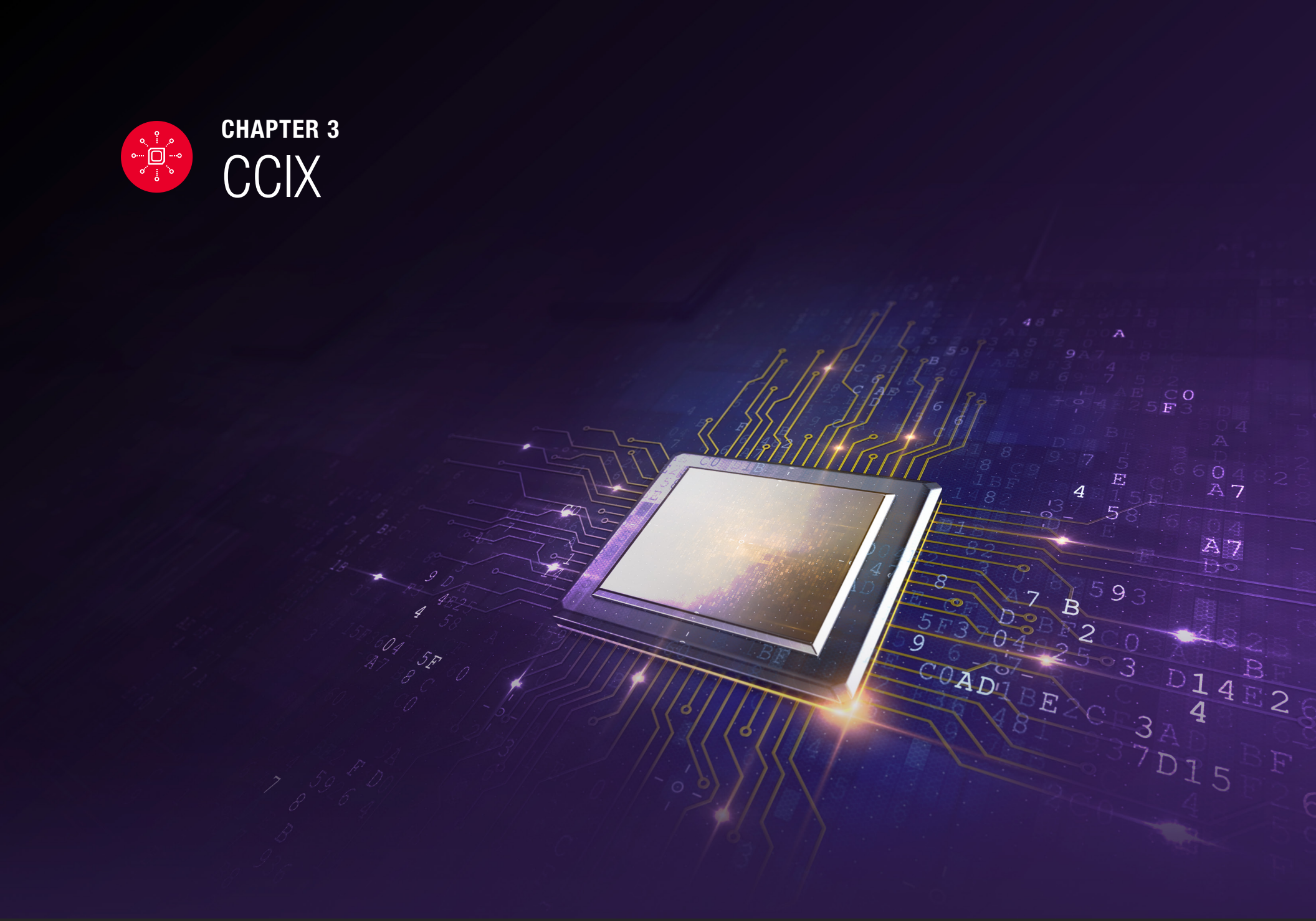
A Bit Error Rate Tester (BERT) can be used to test your receiver. In this test, a worst case PCIe 5.0 eye is carefully constructed using calibrated impairments and physical ISI traces to achieve a target eye height of 10 mV (post-equalization). The goal is to present a worst-case stressed eye to the receiver input and then count errors to determine the receiver's ultimate capabilities.

LEARN MORE

Learn more about PCIe design and simulation plus transmitter, receiver, interconnect, and protocol test on the High-Speed Digital System Design, PCI Express (PCIe) Data Sheet.

CHAPTER 3

CCIX



CHAPTER 3
CCIX

Innovative technologies such as Cache Coherent Interconnect (CCIX) are making their way into production. CCIX borrows the PCI Express physical layer, but change the function of the bus to allow for greater efficiency and faster speeds. While PCIe is currently at 16 Gbps, moving to 32 Gbps with PCIe 5.0, CCIX runs at 20 – 25 Gbps and there are plans to move to greater than 40 Gbps in the near future. This offers a way to increase the throughput of chip-to-chip communications.

In addition to being faster, CCIX enables cache coherency. Cache coherency ensures that changes made to multiple copies of shared data update through the system quickly. Therefore, CPUs can communicate faster to the rest of the system. This capability is not supported by PCIe.

The technology of CCIX is counting on the speed improvements of cache coherency and faster speeds in general to move an entire data center industry to specialize in CCIX for communication between CPUs and accelerators. Cache coherency is only effective if implemented in the CPU and accelerator components throughout the data center. If the entire ecosystem implemented cache coherency through CCIX, all components would receive automatic updates in their cache.

For transmitter tests of either PCI Express or CCIX, use a high bandwidth oscilloscope as a stand-in for your receiver. The UXR-Series oscilloscopes come in models from 13 – 110 GHz with ultra-low noise to support next generation technologies like PCIe 5.0 and CCIX.

LEARN MORE

Whitepaper: CCIX, A New Interconnect Technology

CHAPTER 4

USB Type-C

CHAPTER 4
USB Type-C

The USB Type-C connector supports high-speed data transport in a compact, reversible design. The connection supports connector standards for USB 2.0 through USB 3.1, Thunderbolt, MHL, DisplayPort, and more. The USB Type-C specification defines a 24-pin interface as well as silicon structure functionality in devices. The design is consumer friendly, with a slim, flippable connector. It also achieves data rates of 10 Gbps, with 40 Gbps within reach for two-lane operation. This is an advantage of using the high-performance Type-C connector instead of legacy USB connectors. Tablets, laptops, and mobile phones are universally beginning to take advantage of the low-profile and reversible connector.

Connecting between devices will be even easier for users, as they can connect in either direction and to more devices with multiple functions. However, the validation engineer's tasks when performing test validation has become more complex. It has grown from one set of USB tests to include USB 3.1 on both ports since the cable can be flipped, USB 2.0, Power Delivery, and any Alternate mode test regimens.

How You Can Prepare

For USB Type-C devices, the following functions will require test and validation:

- USB and DisplayPort signal analysis using a high bandwidth oscilloscope
- Thunderbolt over Type-C
- Transmit and receive in both orientations
- All protocols that will be transmitted
- Control of CC signal loading for power up, debug, and test
- Communication over CC line for
  - Power setup
  - Alternate mode (protocol) control
- Power Delivery communication channel, its protocol, and the VBUS profile including high current states
- Sideband communication channels when used to provide additional connections and alternate modes

Design and test engineers can save time and have more confidence in their test results when they use USB Type-C test hardware, software, and fixture tools. For example, a control fixture can manage power and control lines and enable the breakout of USB 3.1 signals from USB devices for system diagnosis and control. Protocol and decode software on an oscilloscope offers a quick way to decode and debug serial data with search and trigger capabilities. Equipping your lab with these test capabilities will ease the pains of testing and reduce manual labor.

LEARN MORE

To learn more about how to test USB Type-C and available test tools, read the Overcoming Test Challenges of USB Type-C Application Note

CHAPTER 5

Thunderbolt

CHAPTER 5
Thunderbolt

Thunderbolt is a hardware interface that supports several protocols through the USB Type-C connector. It enables a diverse collection of external devices to be connected to a computer. These external devices range from high-resolution displays and external memory drives to docking station – and they all can connect with the same USB Type-C connector previously described.

Thunderbolt was developed to simultaneously support high-speed data transfer, video bandwidth, and supply power on a single cable. New uses, such as 4K video, single-cable charging docks, external graphics, and built-in 10 Gigabit Ethernet networking, as well as devices with smaller form factors, are driving Thunderbolt technology. Thunderbolt 3 chipsets are deployed in servers, workstations, laptops, gaming PCs, industrial cameras, high-speed PCIe storage, displays, and adapters. Thunderbolt is now in its third generation with two independent 20 Gbps links into one 40 Gbps link. Thunderbolt 3 connects two 60 Hz 4K displays and provides 100 watts of power and more protocols than previous Thunderbolt generations, including DisplayPort, USB, and PCIe.

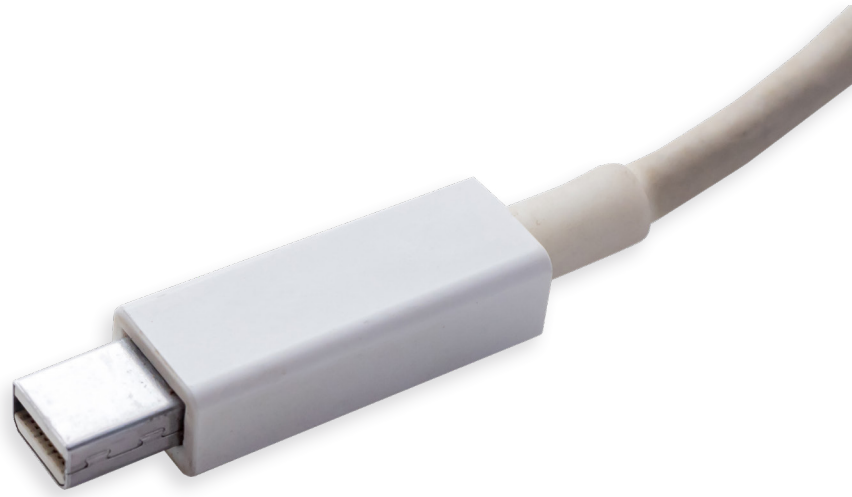
How You Can Prepare

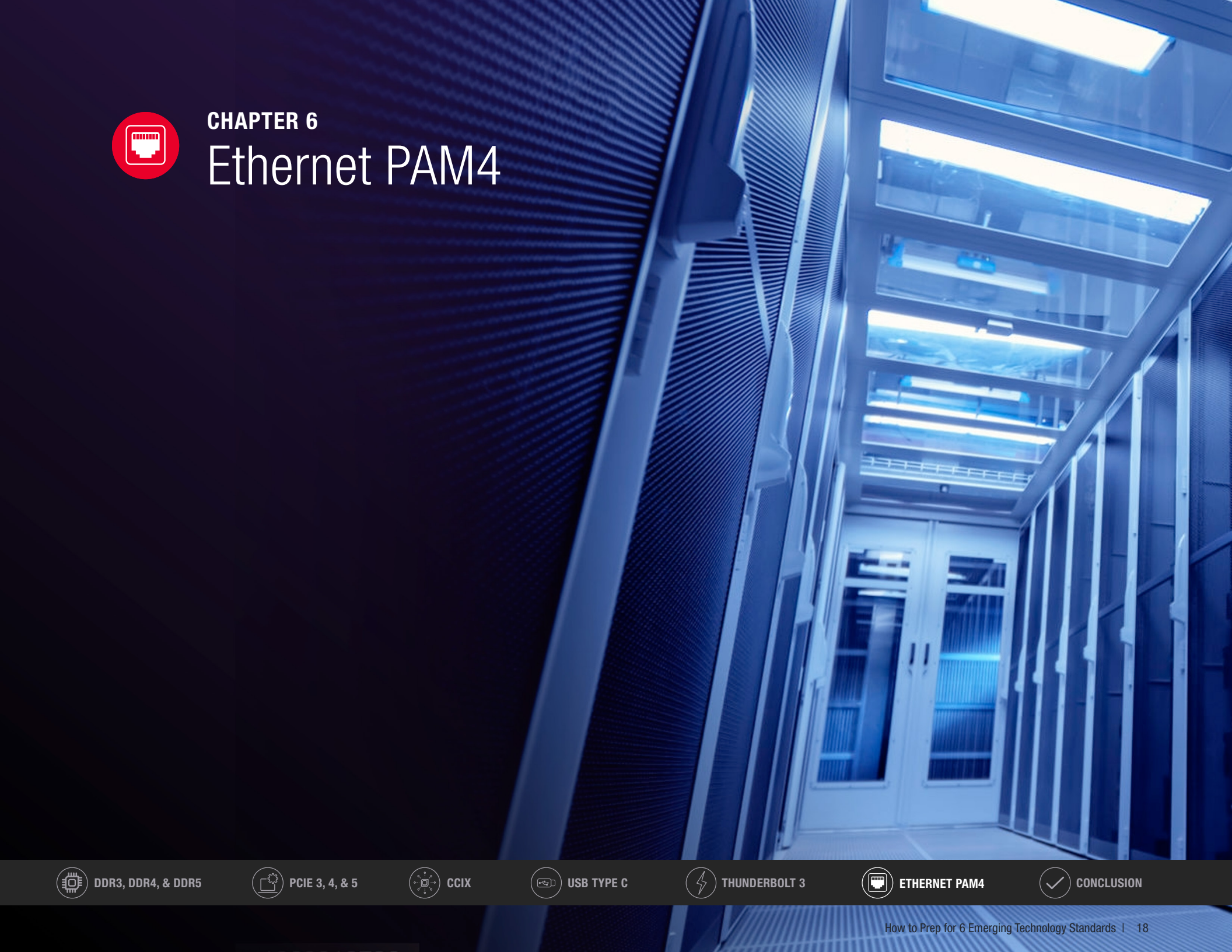
The original Thunderbolt and Thunderbolt 2 were relatively easy to test because they used an active cable and had open eyes at the transmitter and receiver. Thunderbolt 3 is more difficult because it incorporates a passive cable, which makes testing vastly more complex. At 20 Gbps, signals are significantly impaired when conducted electrically even over short distances with passive cables. Therefore, it is best to use transmitter and receiver equalization to compensate for the lossy channel's effects.

Use compliance software to quickly and easily verify and debug your Thunderbolt designs for silicon validation, as well as end products like storage devices or motherboards. Choose compliance software that matches the standard's test requirements and parameters of certification testing so you know how your design will perform during official certification.

LEARN MORE

Keysight's D9030TBTC Thunderbolt 3 Tx Test Software automates the test process and provides test reports using the standard's test requirements and parameters of certification testing.





CHAPTER 6

Ethernet PAM4

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Ethernet PAM4

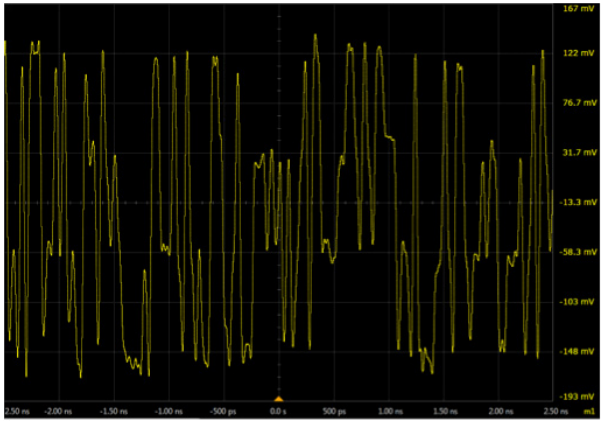


Figure 1: the time domain capture of a PAM-4 signal

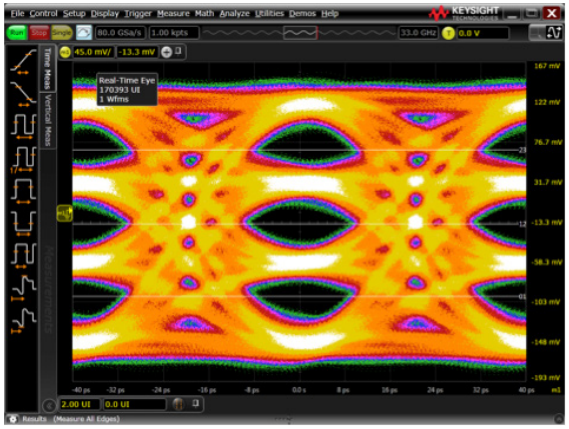


Figure 2: the bit-slice of this, showing the transition states overlapped, which creates an eye diagram

Like all the digital technologies mentioned in this eBook, Ethernet developments are driven by a greater demand for data. Faster speeds have already pushed the capabilities of what can be done with two bits, or NRZ (Non-Return to Zero) signals, so Pulse Amplitude Modulation 4 (PAM4) has become the de facto alternate solution. Instead of sending only two logic values, with one bit per symbol, PAM4 sends four values – two bits per symbol.

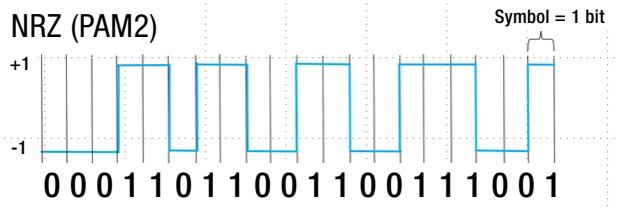


Figure 3: the idealised two-state NRZ digital signal

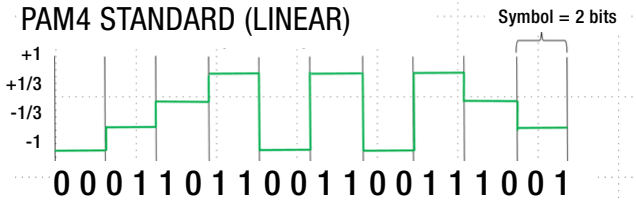


Figure 4: the idealised PAM-4 signal with respective voltage levels

How You Can Prepare

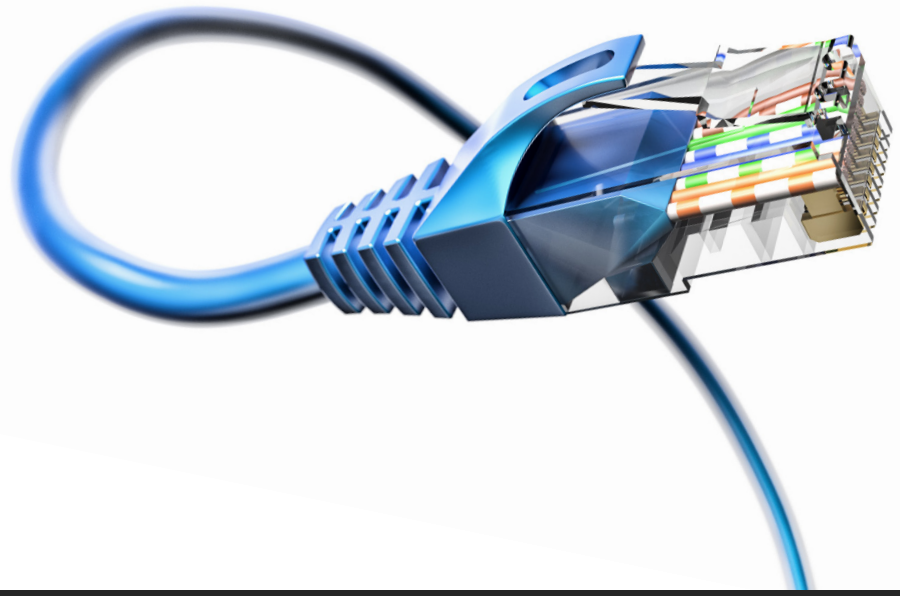
PAM4 transmits and receives four amplitude levels. This doubles the throughput for the same baud rate of an NRZ signal, but makes things more complex. Four distinct levels within the same total amplitude as an NRZ signal mean smaller eye openings and reduced margins. Keeping PAM4 eyes open, symmetrical, and un-skewed when transmitting data brings new challenges to designers.

Clock skew can have a significant impact on the vertical alignment of PAM4 eyes. Upper and lower eyes can become skewed relative to the middle eye, meaning the most significant bit may be arriving at a different time than the least significant bit. This creates symbol errors making it difficult or impossible for the receiver to recover the correct data.

Non-linearity and amplitude compression, where one eye becomes smaller than the others, can also be an issue. Each eye is the result of four distinct amplitudes, so if these amplitudes are distorted by compression or non-linearity, the receiver may interpret them incorrectly.

To prevent these distortions caused by the channel, use Forward Error Correction (FEC). It encodes the message redundantly, so the receiver can detect errors in the transmission and fix them.

For compliance testing, the UXR oscilloscope with D9010EBSC tests to standards set in IEEE802.3bs/cd.



CHAPTER 7
Conclusion

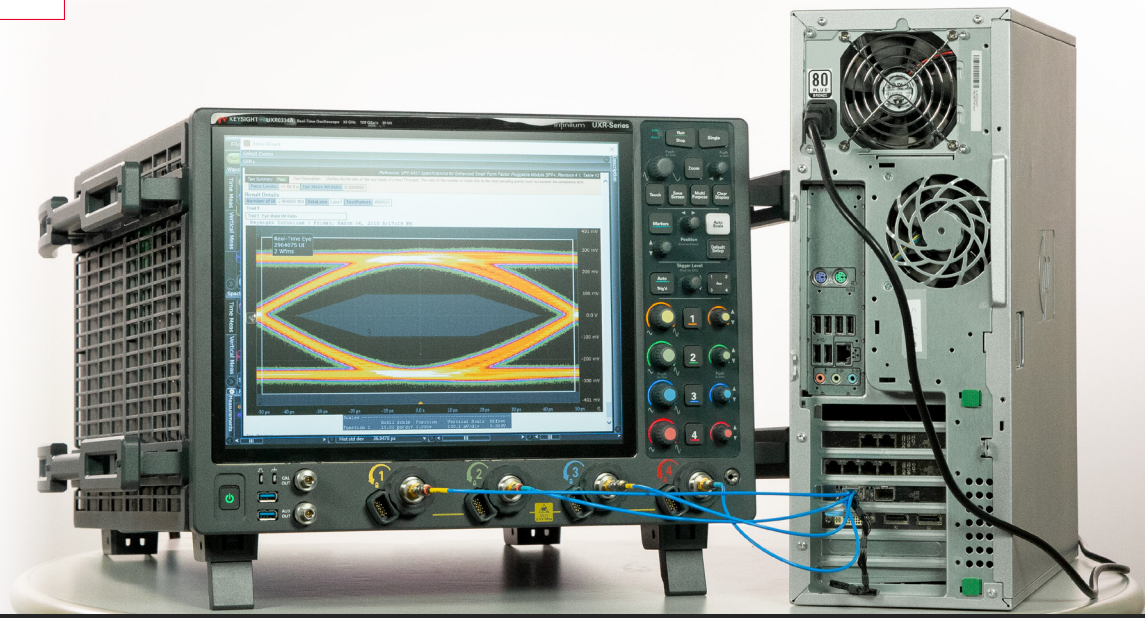
The explosion of data sharing, downloading, and uploading is generating a new demand for memory and transfer speeds.

The demand for speed is driving new technology innovations with shorter development cycles than ever before. At the same time, the need for speed means decreased margins, the result of faster speeds and lower power requirements. However, innovation in test equipment and test techniques is progressing to ensure test needs are satisfied. With proper preparation and testing of next generation technologies, you will get ahead of the curve.

LEARN MORE

Learn more about how the UXR Series can help validate your high-speed digital designs at www.Keysight.com/find/UXR

> Keysight's New Infiniium UXR-Series Oscilloscopes Deliver Industry-Leading Signal Integrity, Enabling You To Increase Margins and Open Eye Diagrams



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