GaN ASM-HEMT Modeling & Verification Workshop

CHEN, Jason

Application Engineer

2020.04.21

KEYSIGHT TECHNOLOGIES

Agenda

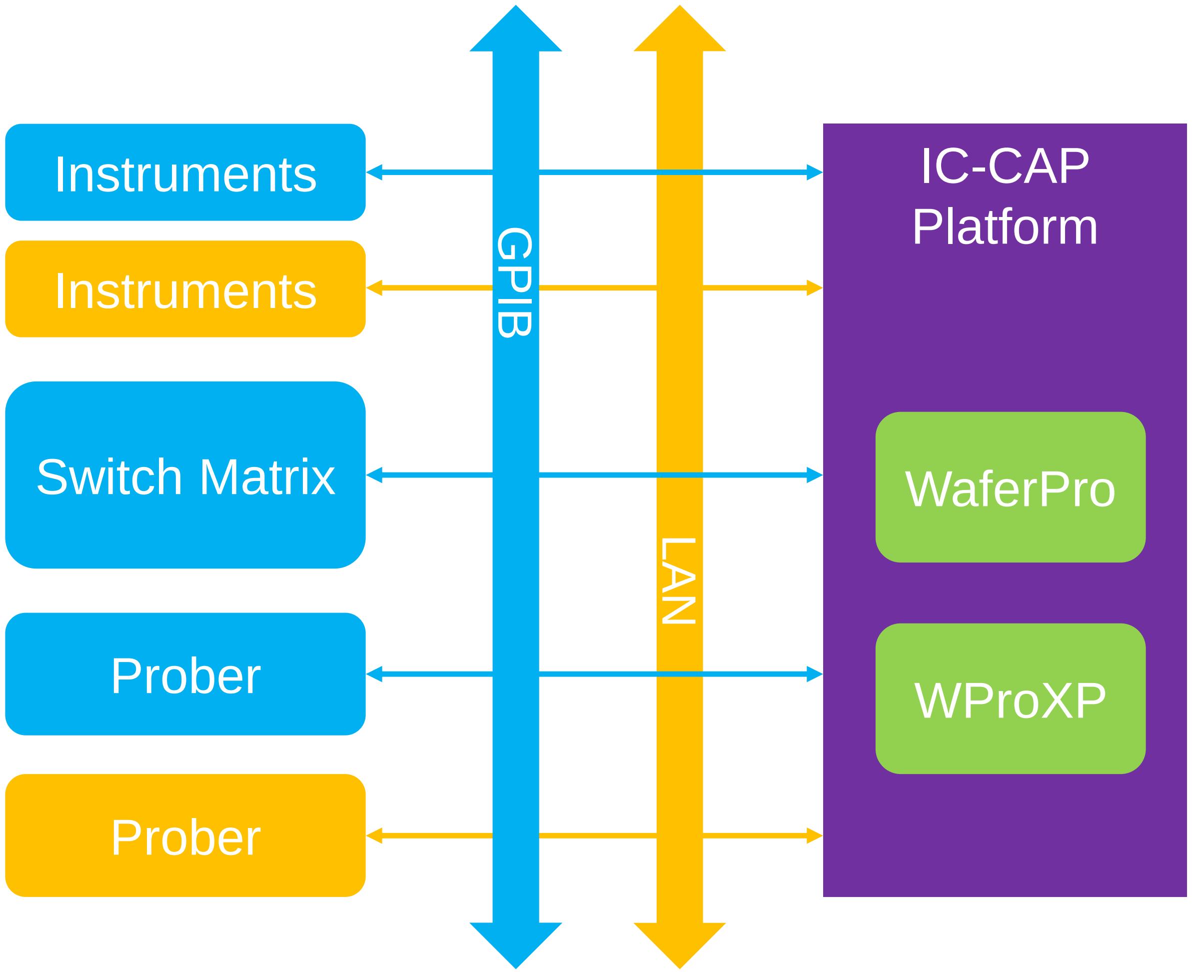
- Quick Start for IC-CAP
- Introduction to ASM-HEMT Model
- Introduction to CMC Modeling Kit (ASM-HEMT) in IC-CAP
- Export Model to ADS for Load-pull Simulation

Quick Start for IC-CAP

What is PATHWAVE Device Modeling : IC-CAP

- **Integrated Circuit Characterization and Analysis Program**
- Integrate measurement and modeling on the same platform
- Support various simulators and python script
- Support customized GUI and extraction flow
- Suitable for highly customized modeling, such as RF and Power devices

IC-CAP Measurement System



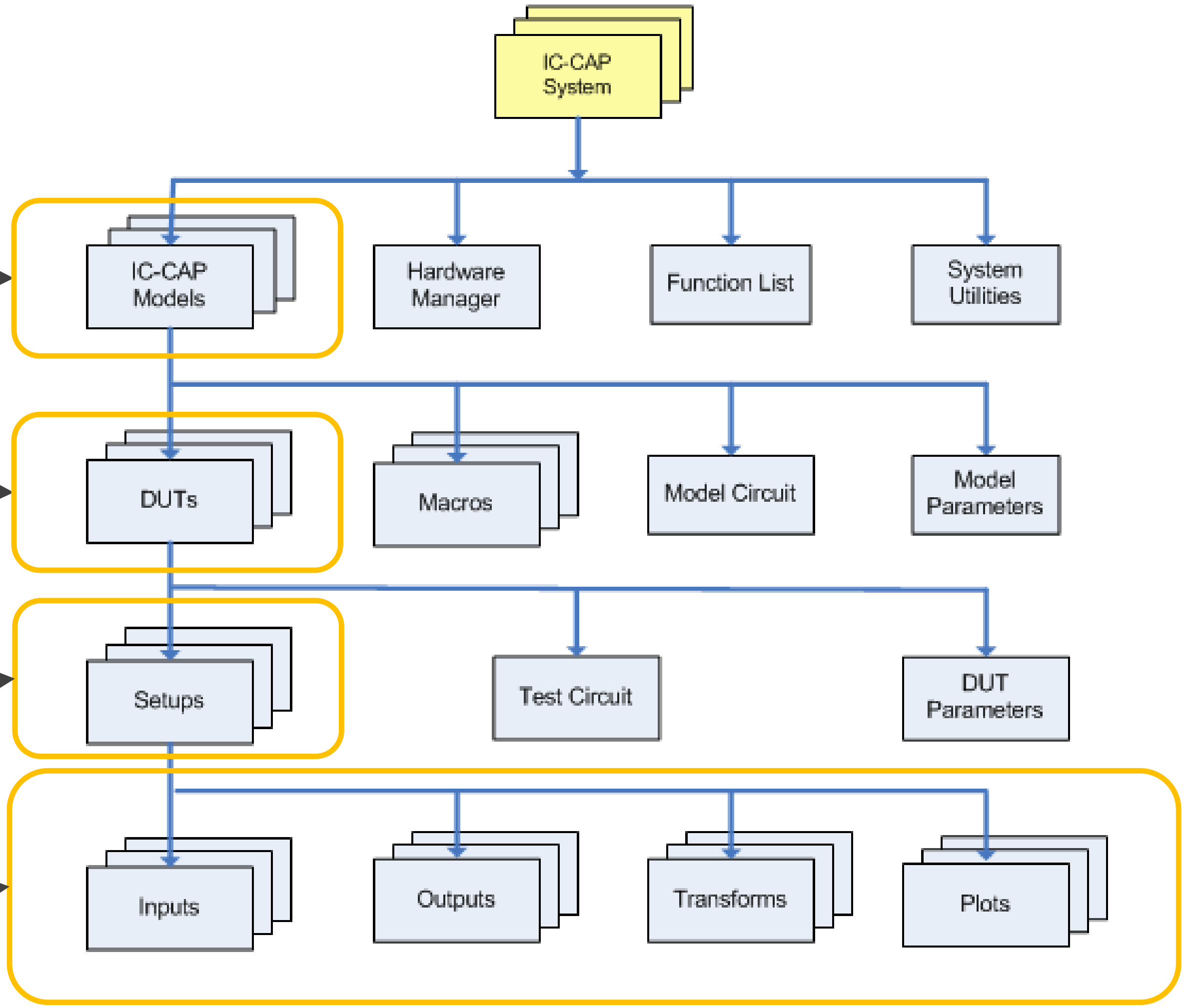
IC-CAP System Organization

Different types of model, such as HEMT, MOSFET, BJT

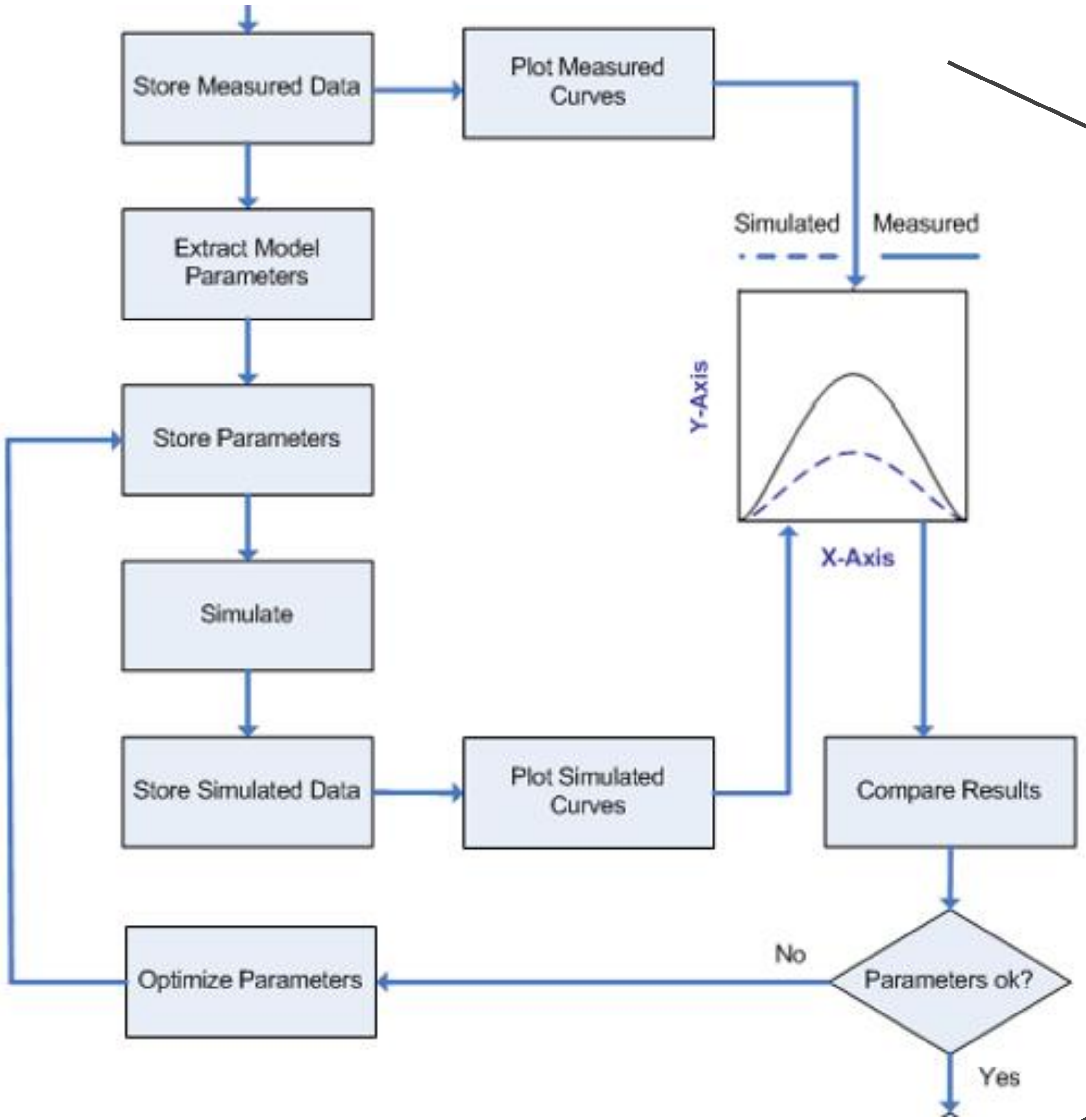
Different dimensions of same type of model, such as A100x10, A100x8

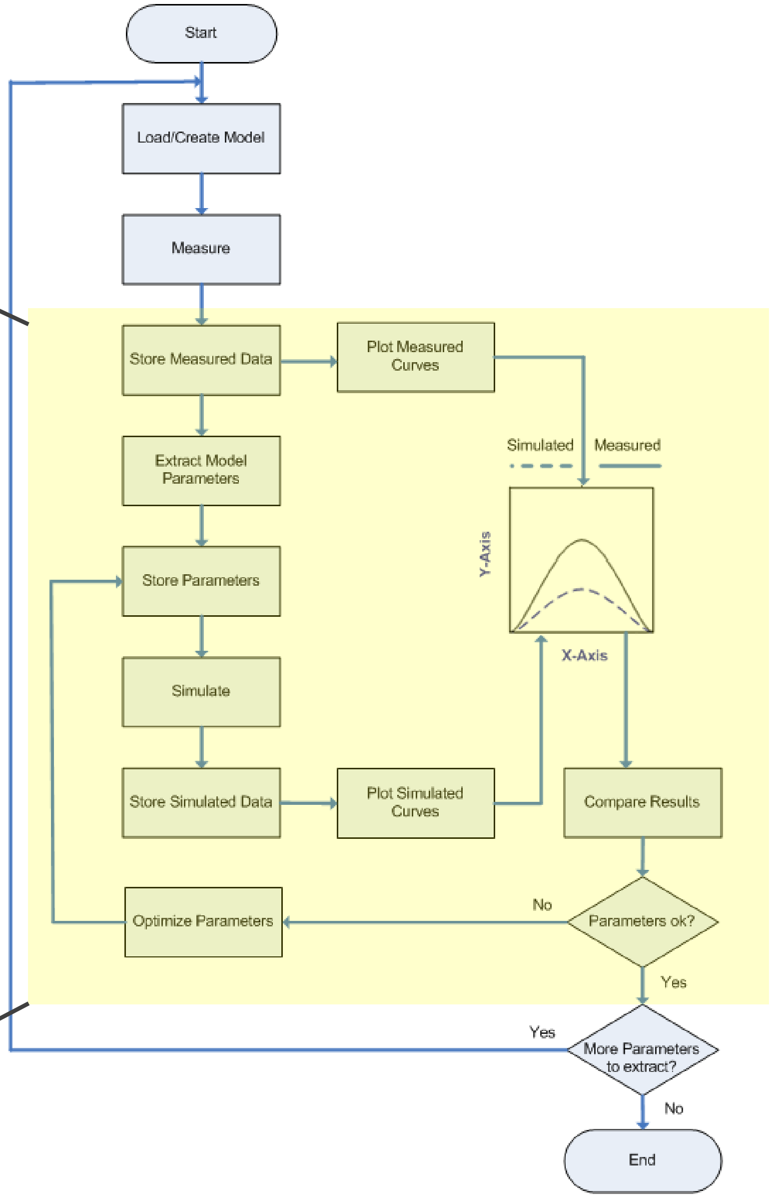
Different measurements of the same device, such as IdVg, IdVd, Sparam

Configurations and Extractions of the same measurement



Typical Modeling Flow

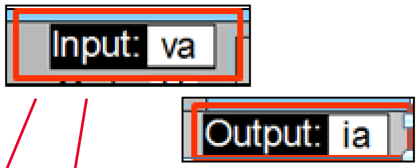


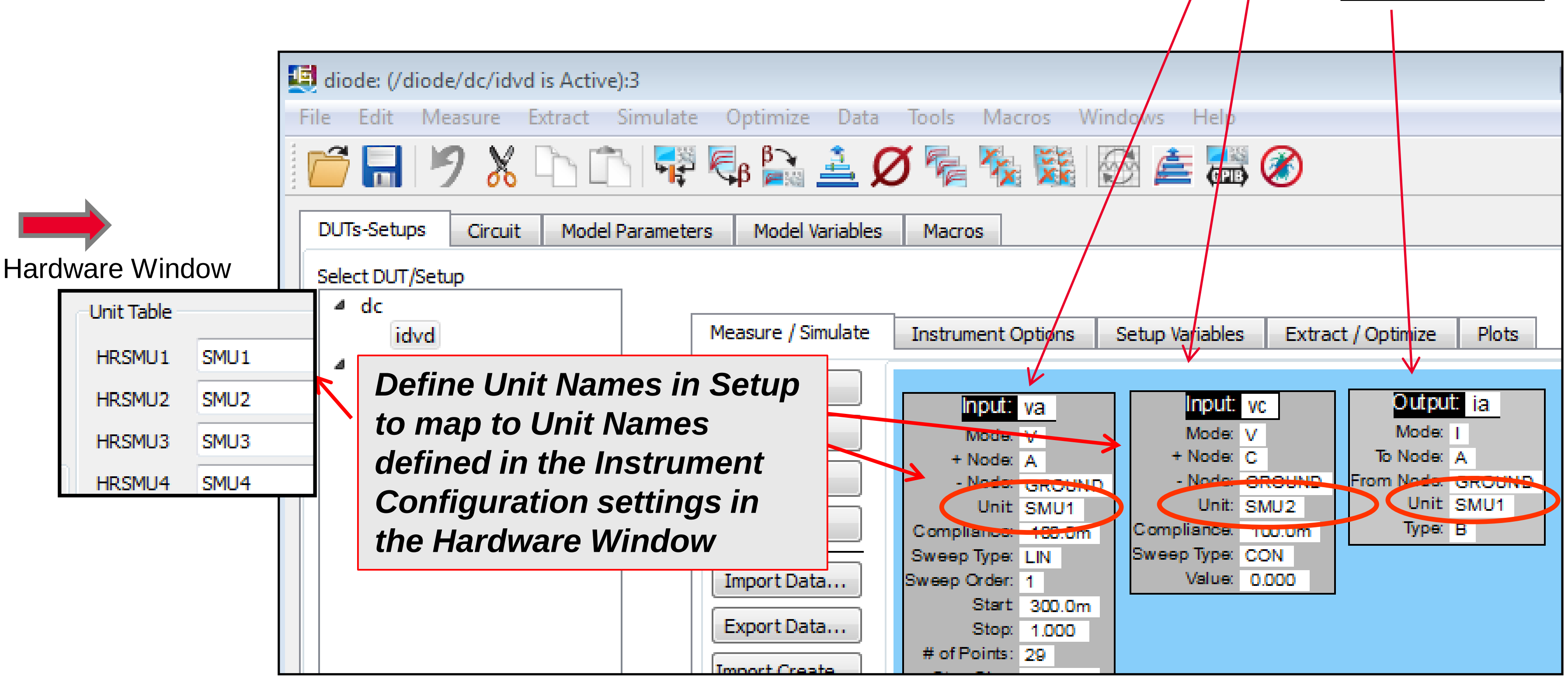


How Measurement Works

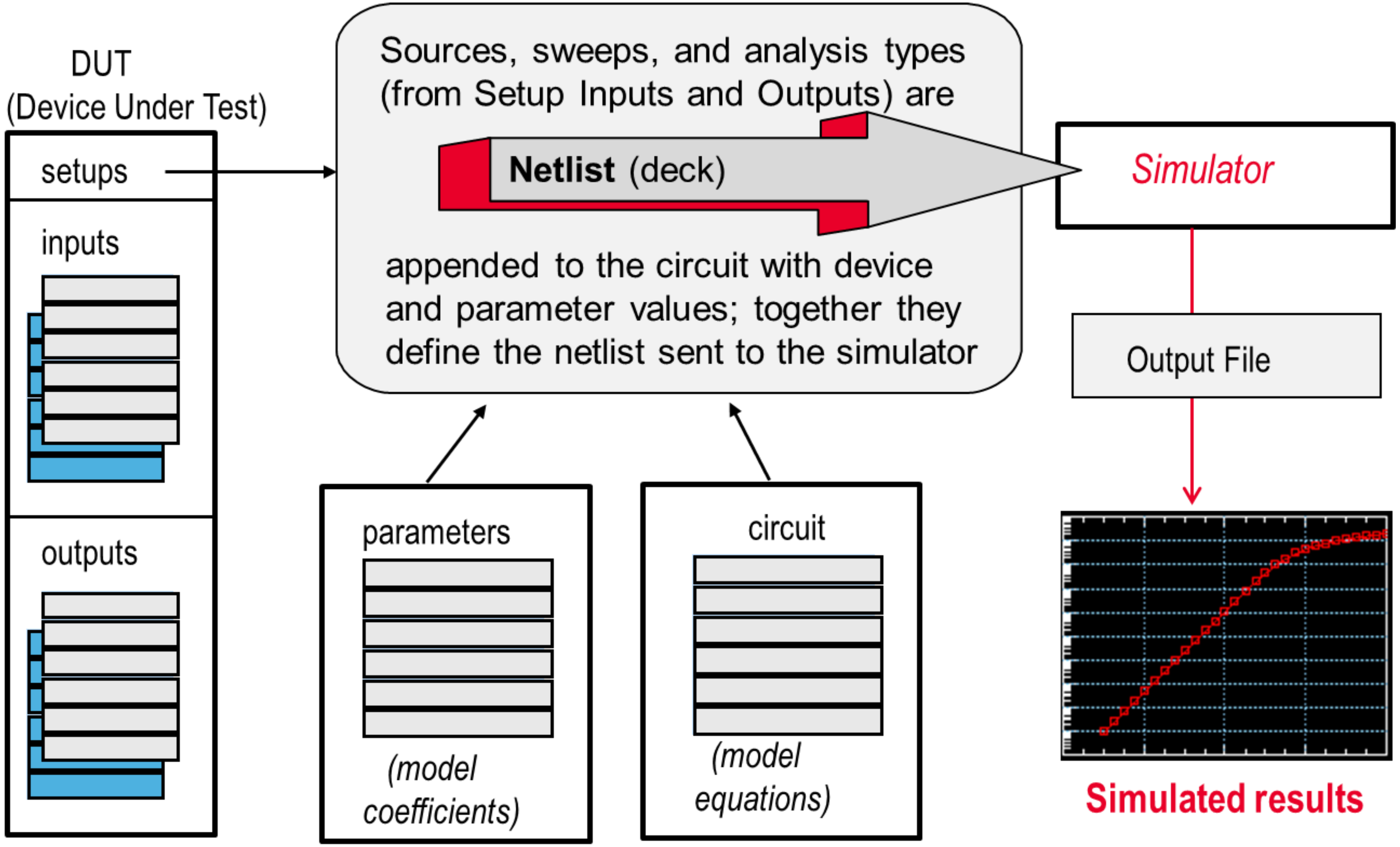
Inputs: Define the Stimulus/Bias to be applied

Outputs: Define the Data to be Measured





How Simulation Works



Introduction to ASM-HEMT Model

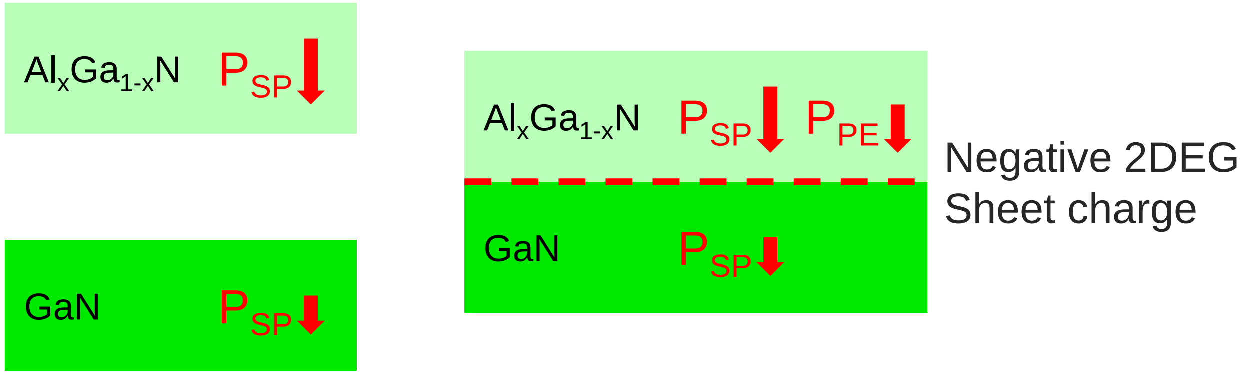
ADVANCED SPICE MODEL FOR HEMT

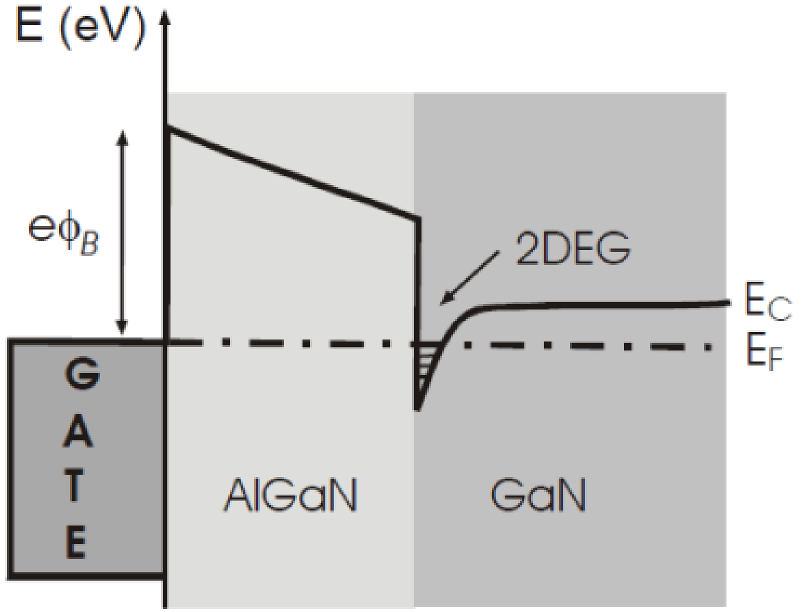
GaN HEMT Devices

HOW DOES A GAN DEVICE WORK?

- Difference between $Al_xGa_{1-x}N$ and GaN **spontaneous polarization (P_{SP})** creates a sheet charge at the interface.
- Difference in lattice constants leads to mechanical strain and piezoelectric effect **(P_{PE})**

- quantum well at the heterojunction interface → 2 Dimensional Electron Gas (2-DEG)
  - very high mobility
  - Low resistance





ASM-HEMT Model Overview

Electrostatics: Analytical Solution of Schrödiger’s & Poisson’s → 2-DEG Charge, Ef, Surface Potential

Transport: SP-Based Current & Charge Model → I-V, C-V, DIBL, Rd, Rs, Vel. Sat., ...

Higher-order Effects: Noise, Trapping, Self-Heating, Field Plate → DC, AC, Transient Harmonic Sim., Noise, ...

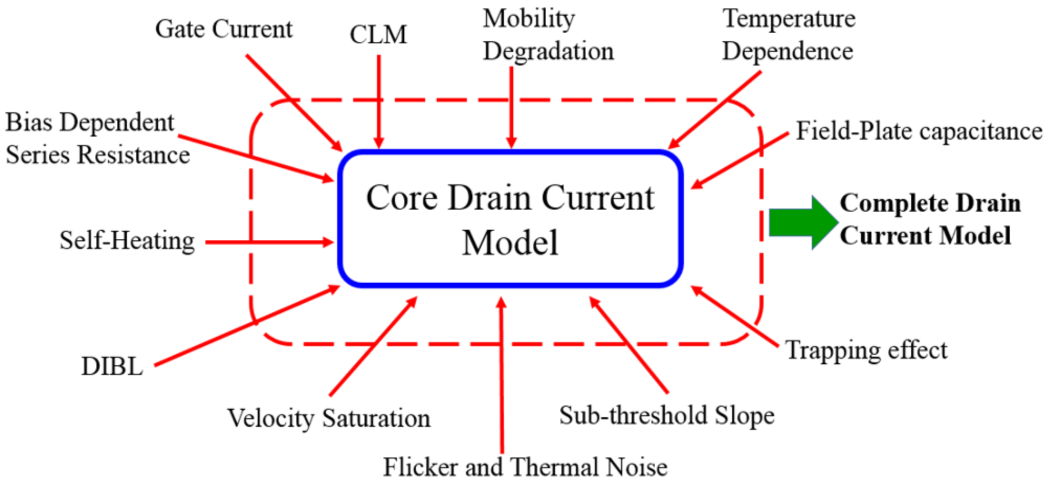
Source: Prof. Yogesh Chauhan

Advantages of Surface Potential-based Model

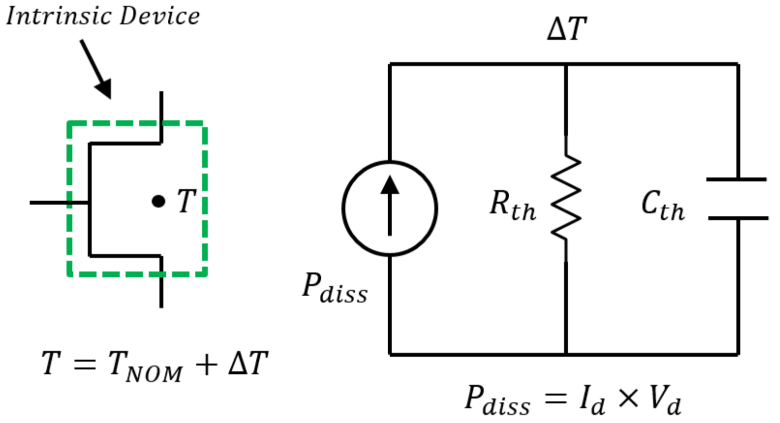
- Better Model Scalability – L, W, NF, Lsg, Ldg, Temperature etc.
- Better Temperature Scalability
- Device Insight
- Better Statistical Behavior
- Accurate Charges and Capacitances
- Less number of parameters – Easier parameter extraction
- Uses a single expression for all regions – Faster convergence, smooth derivatives
- Inherent Model Symmetry and Continuity

Source: Prof. Yogesh Chauhan

Core Model & Parameters



Real Device Effects Incorporated into the Model



Self-Heating Effect

Core Model Parameters

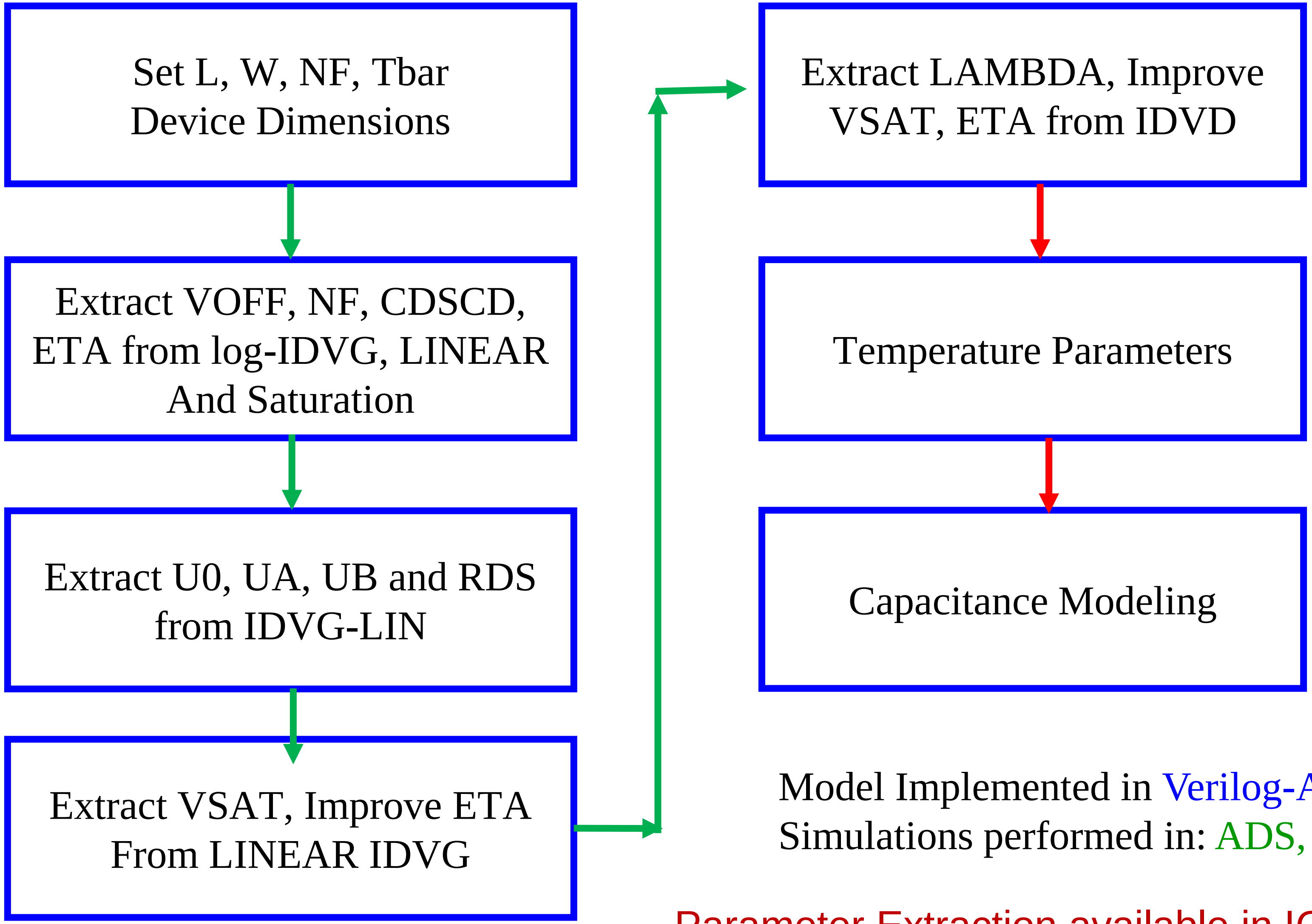
Parameter	Description	Extracted Value
V_{OFF}	Cutoff Voltage	$-2.86\ V$
N_{FACTOR}	Subthreshold Slope Factor	0.202
C_{DSCD}	SS Degradation Factor	$0.325\ V^{-1}$
η_0	DIBL Parameter	0.117
U_0	Low Field Mobility	$33.29\ mm^2/Vs$
N_{SOACCS}	AR 2DEG Density	$1.9e+17\ /m^2$
$V_{SATACCS}$	AR saturation velocity	$157.6e+3\ cm/s$
R_{TH0}	Thermal Resistance	$22\ \Omega$

Core drain current expression

$$I_{ds} = \frac{\mu_{eff}}{\sqrt{1+\theta_{sat}^2\psi_{ds}^2}} \frac{W}{L} C_g N_f \left[V_{go} - \left(\frac{\psi_s + \psi_d}{2}\right) + V_{th}\right] \times \psi_{ds}($$

Source: Prof. Yogesh Chauhan

Model Parameter Extraction

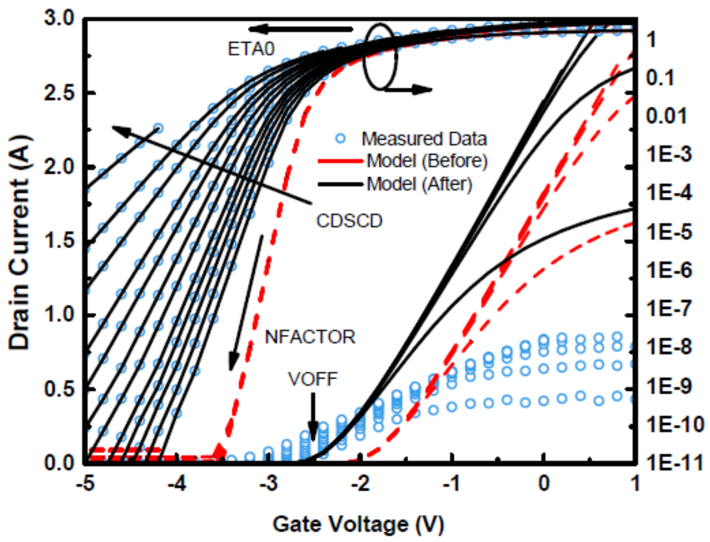


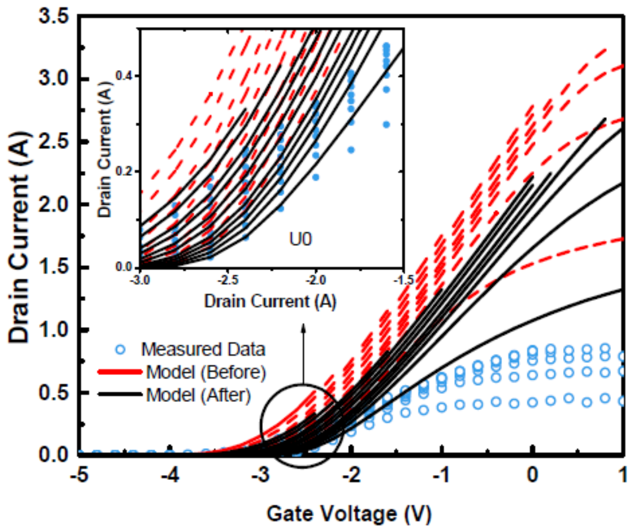
Model Implemented in Verilog-A
Simulations performed in: ADS, Spectre, HSPICE

Parameter Extraction available in IC-CAP Software

Source: Prof. Yogesh Chauhan

Extraction from Id-Vg curves





Start with $I_d - V_g$ characteristics in the <u>log scale</u>

ETA0 – DIBL Parameter

NFACTOR – Sub-threshold slope parameter

CDSCD – Captures the drain voltage dependence on the sub-threshold slope.

VOFF – Cut-Off Voltage

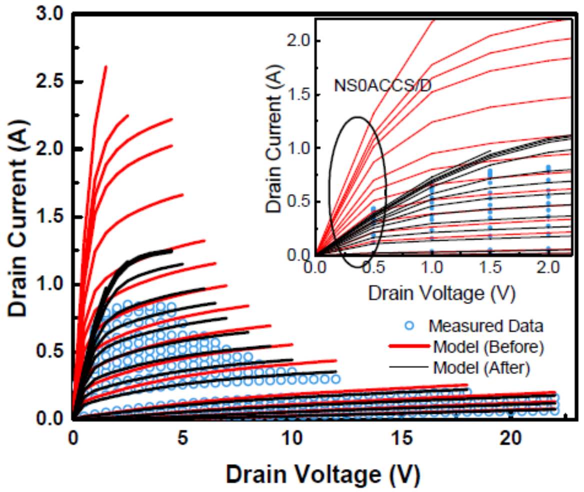
$I_d - V_g$ characteristics in the <u>linear scale</u>

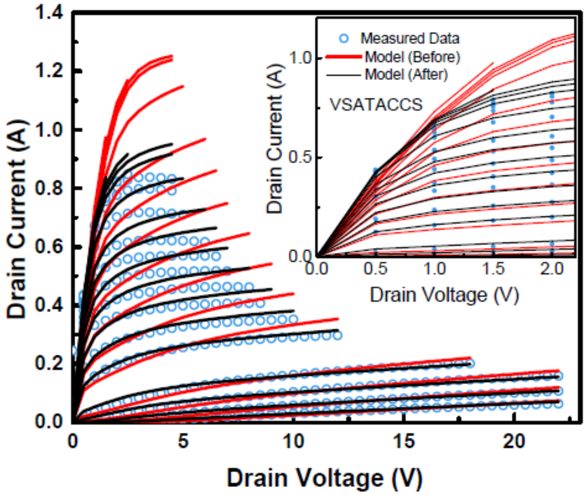
U0 – Low field mobility

UA, UB – Mobility degradation parameters

Source: Prof. Yogesh Chauhan

Extraction from Id-Vd curves





$I_d - V_d$ characteristics

- ***VSAT*** – Velocity saturation parameter
- ***UA*, *UB*** – Mobility degradation parameters

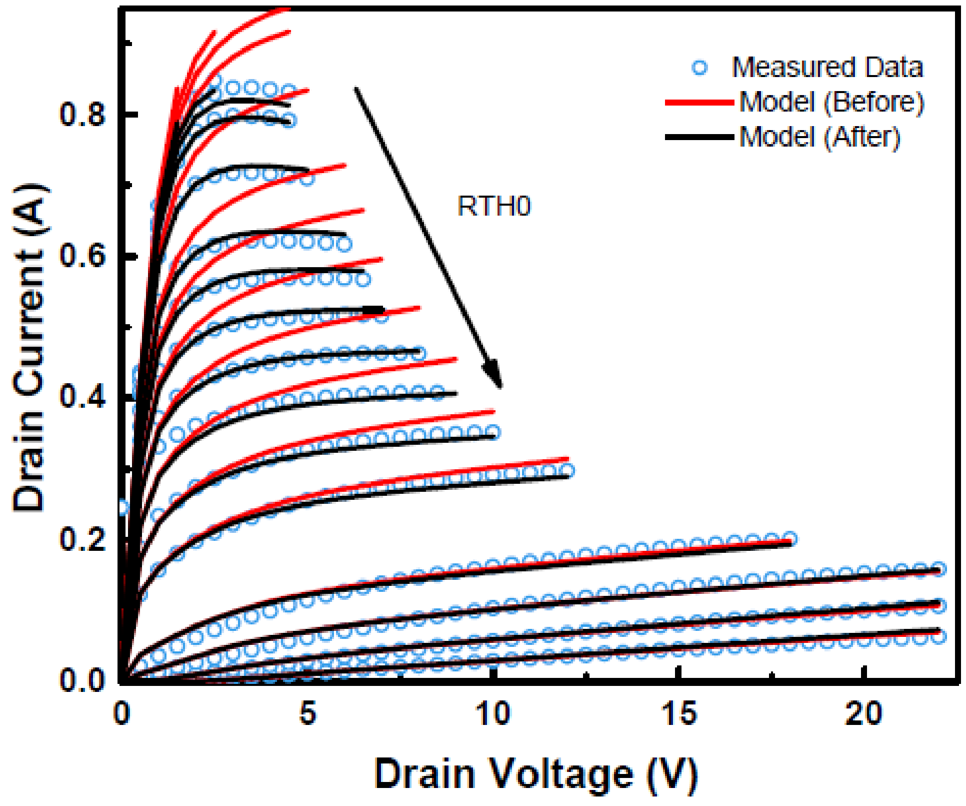
Access Region Parameters extracted from $I_d - V_d$ characteristics:

- ***NS0ACCS(D)*** – 2DEG density in the access region.
- ***VSATACCS*** – Saturation velocity in the access region.
- ***U0ACCS(D)*** – Low field mobility in the access region.

U0ACCS(D) independently tunes the access region resistance around $V_{ds} = 0$ and helps extract g_{ds} at that point.

Source: Prof. Yogesh Chauhan

Parameter Extraction – Self Heating



$I_d - V_d$ characteristics – <u>Self Heating Parameters</u>

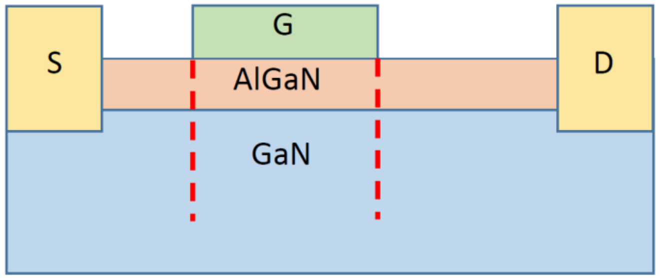
- ***RTH0*** – Self heating resistance.
  - Decides the rate of temperature increase with increasing current.

Temperature dependence parameters to observe the effects of the temperature increase on IV characteristics:

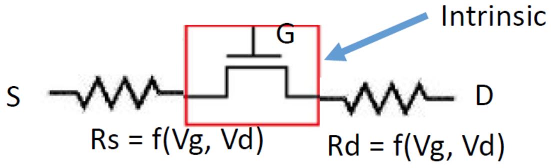
- ***UTE*** – Temperature dependence of mobility
- ***AT*** – Temperature Dependence for saturation velocity

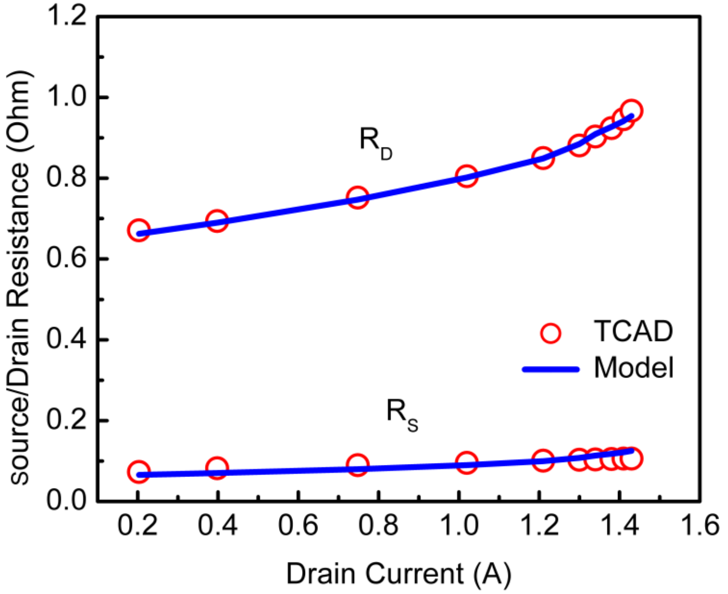
Source: Prof. Yogesh Chauhan

Nonlinear source/drain access region resistance model



$$R_J = \frac{L_J}{q\mu_n n_{s0}} \qquad J = S, D$$





$$I_{acc} = Q_{acc} \cdot v_s = Q_{acc} \cdot v_{sat} \cdot \frac{V_R/V_{Rsat}}{\left[1 + \left(\frac{V_R}{V_{Rsat}}\right)^{\gamma}\right]^{\frac{1}{\gamma}}}$$

Nonlinear variation of source/ drain access resistances with Ids.

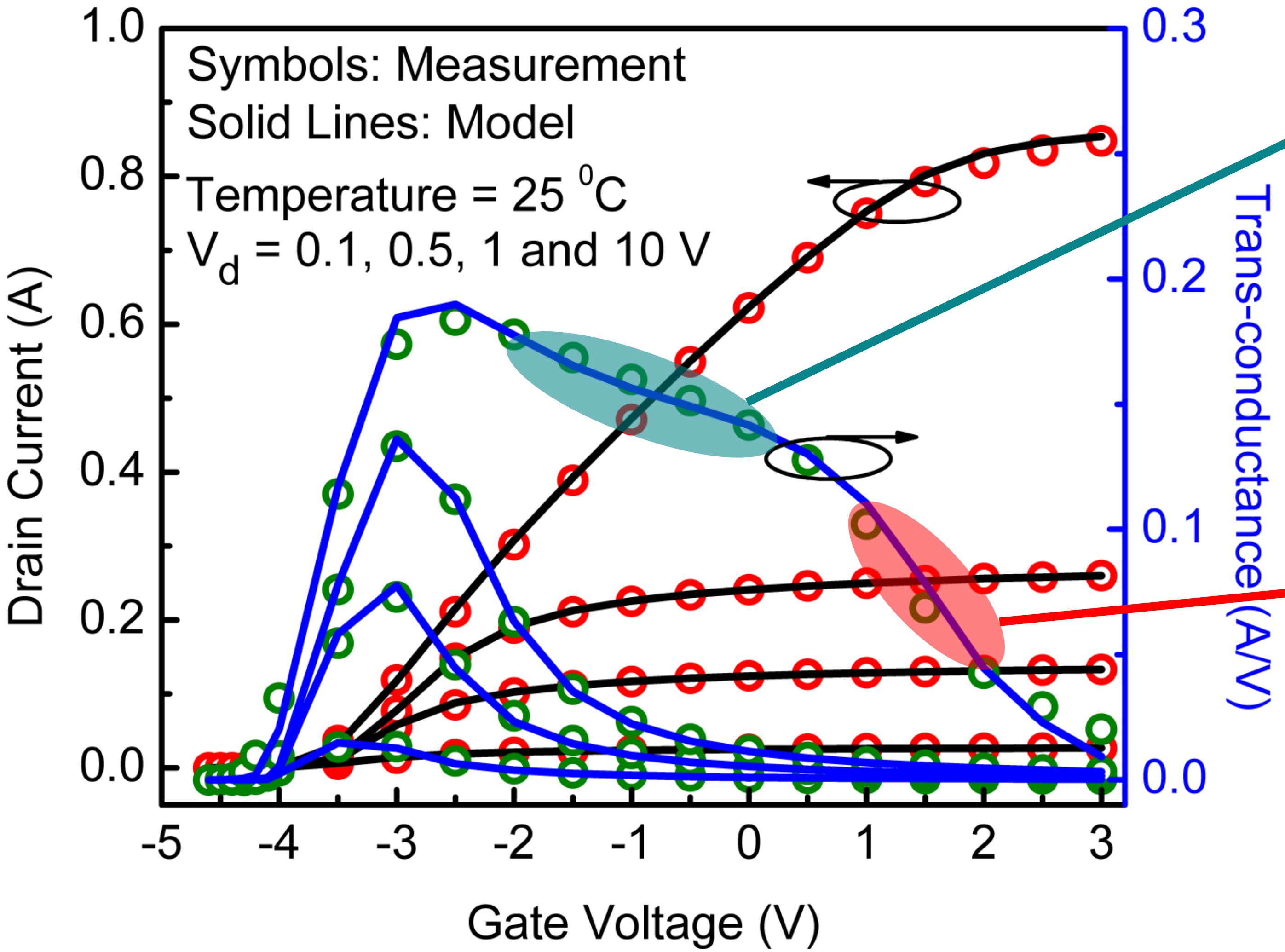
$$R_{d/s} = \frac{V_R}{I_{acc}} = \frac{R_{d0/s0}}{\left[1 - \left(\frac{I_d}{I_{acc,sat}}\right)^{\gamma}\right]^{\frac{1}{\gamma}}}$$

Geometrically scalable

$$\mathrm{I_{ds,acc}} = \frac{\mathrm{R_c}}{\mathrm{W \cdot N_f}} + \frac{\mathrm{L_{acc}}}{\mathrm{W \cdot N_f \cdot q \cdot N_{S0ACCS} \cdot U_{0ACCS}}} \times \left(1 - \left(\frac{\mathrm{I_{ds}}}{\mathrm{W \cdot N_f \cdot N_{S0ACCS} \cdot V_{SATACCS}}}\right)^2\right)^{-1/2}$$

Source: Prof. Yogesh Chauhan

$R_{d/s}$ Model – Effects on Transconductance g_m



The first slope in g_m
→ velocity saturation in the access region.

Second slope in g_m
→ self-heating in the device.

Reason: Self heating has significant impact at high gate and drain biases where the current is high.

Source: Prof. Yogesh Chauhan

Modeling of Temperature dependence

$R_{d/s}$ increases significantly with increasing temperature

Temperature dependence of 2-DEG charge density in the drain or source side access region:

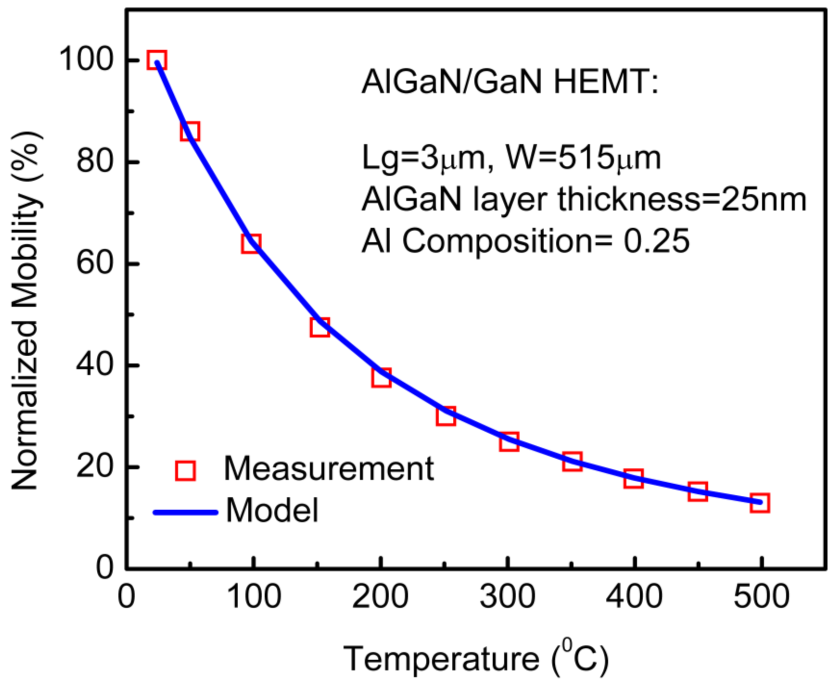
$$n_{s0}(T) = NS0ACC \cdot \left(1 - KNS0 \cdot \left(\frac{T}{TNOM} - 1\right)\right)$$

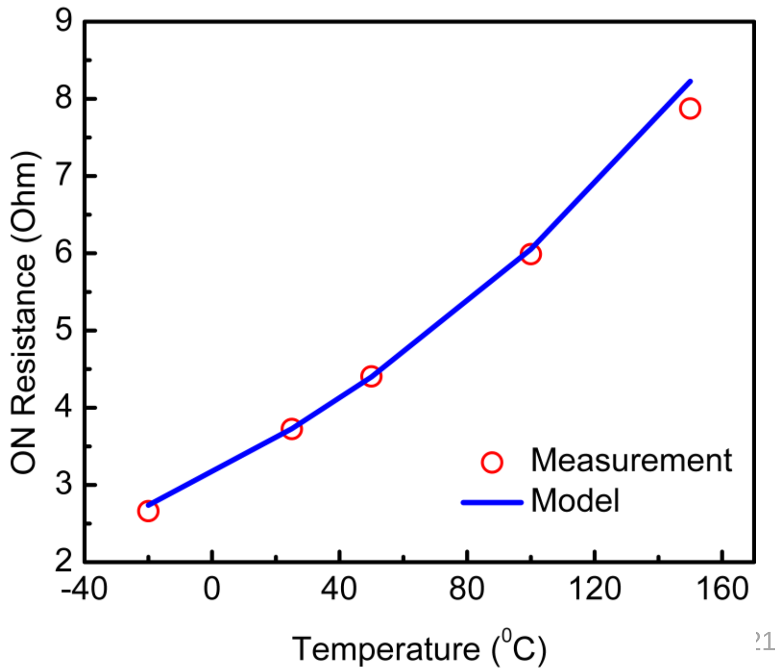
Temperature dependence of Saturation Velocity:

$$V_{sat}(T) = VSATACCS \cdot [1 + ATS(T - TNOM)]$$

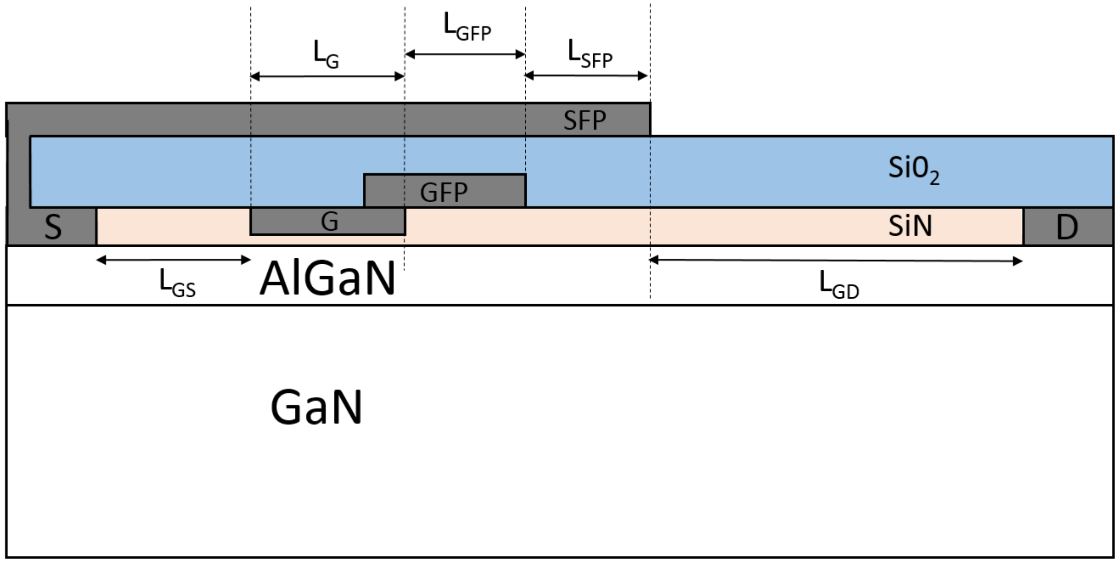
Temperature dependence of electron Mobility:

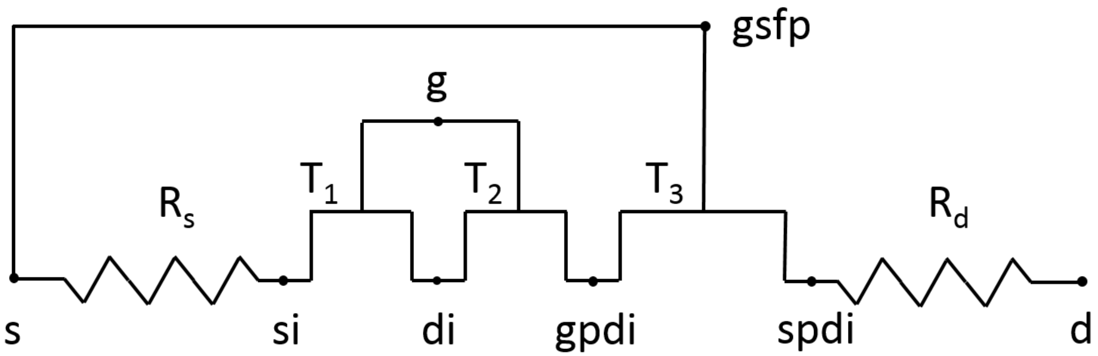
$$\mu_{acc}(T) = U0ACC \cdot \left(\frac{T}{TNOM}\right)^{UTEACC}$$

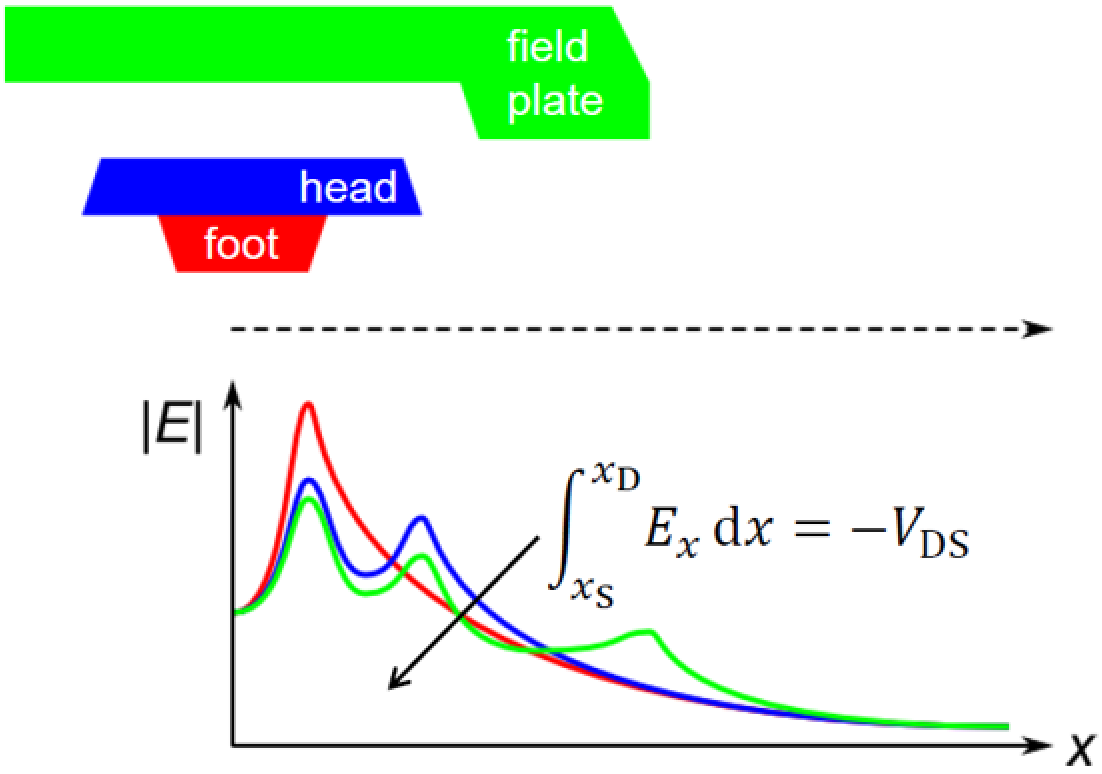




Modeling of Field-Plates in HEMTs

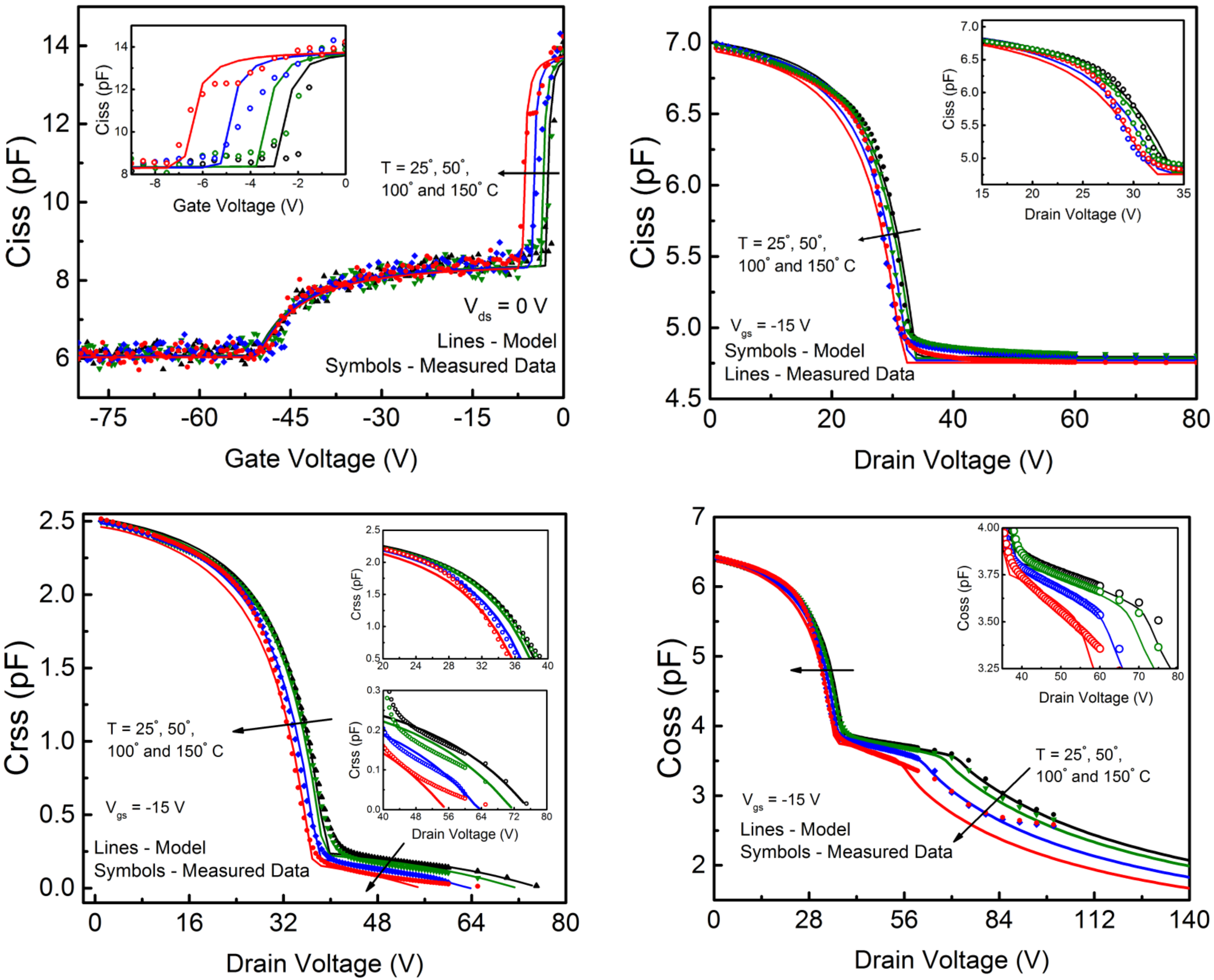






Affects capacitance and breakdown behavior.

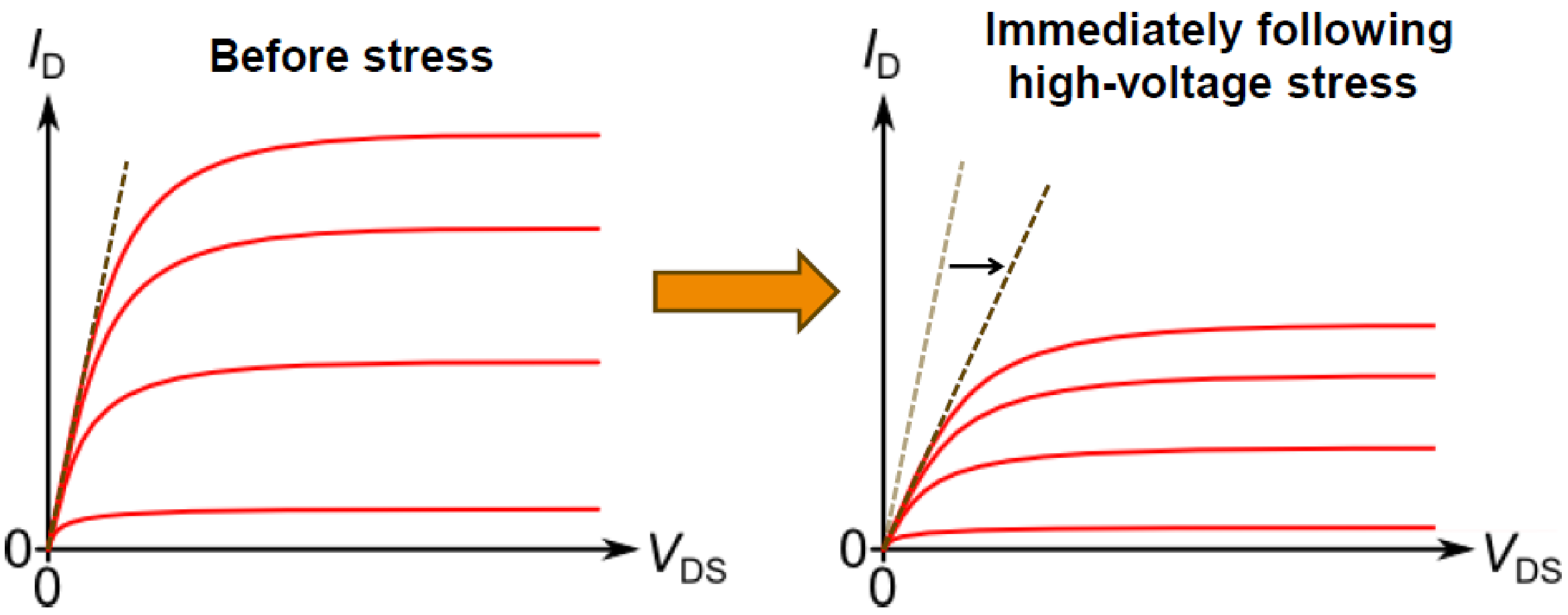
Field-Plate Capacitance Modeling



Source: Prof. Yogesh Chauhan

Current Collapse

- On-state current temporarily reduced following off-state stress



- Also known as **dynamic R_{on}**
  - On-state resistance depends on recent history of device biasing

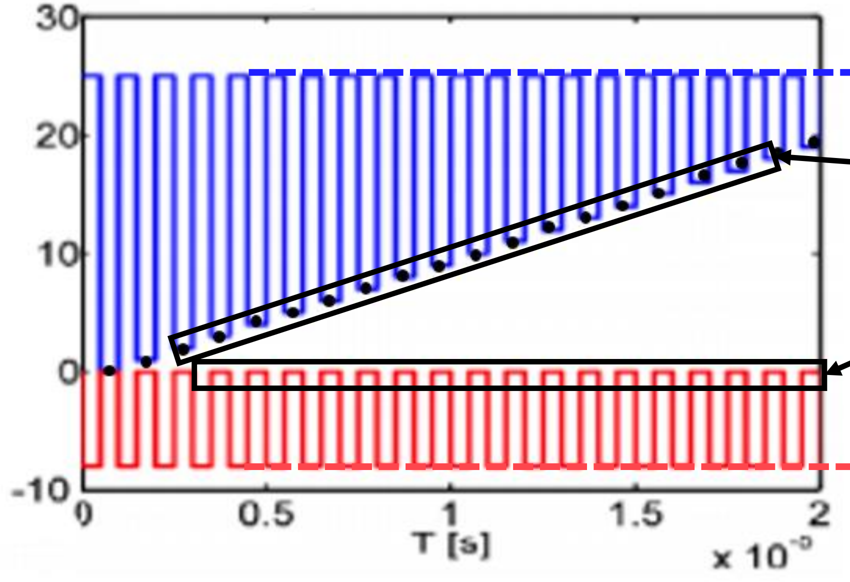
Stephen Sque - ESSDERC tutorial Sept. 2013

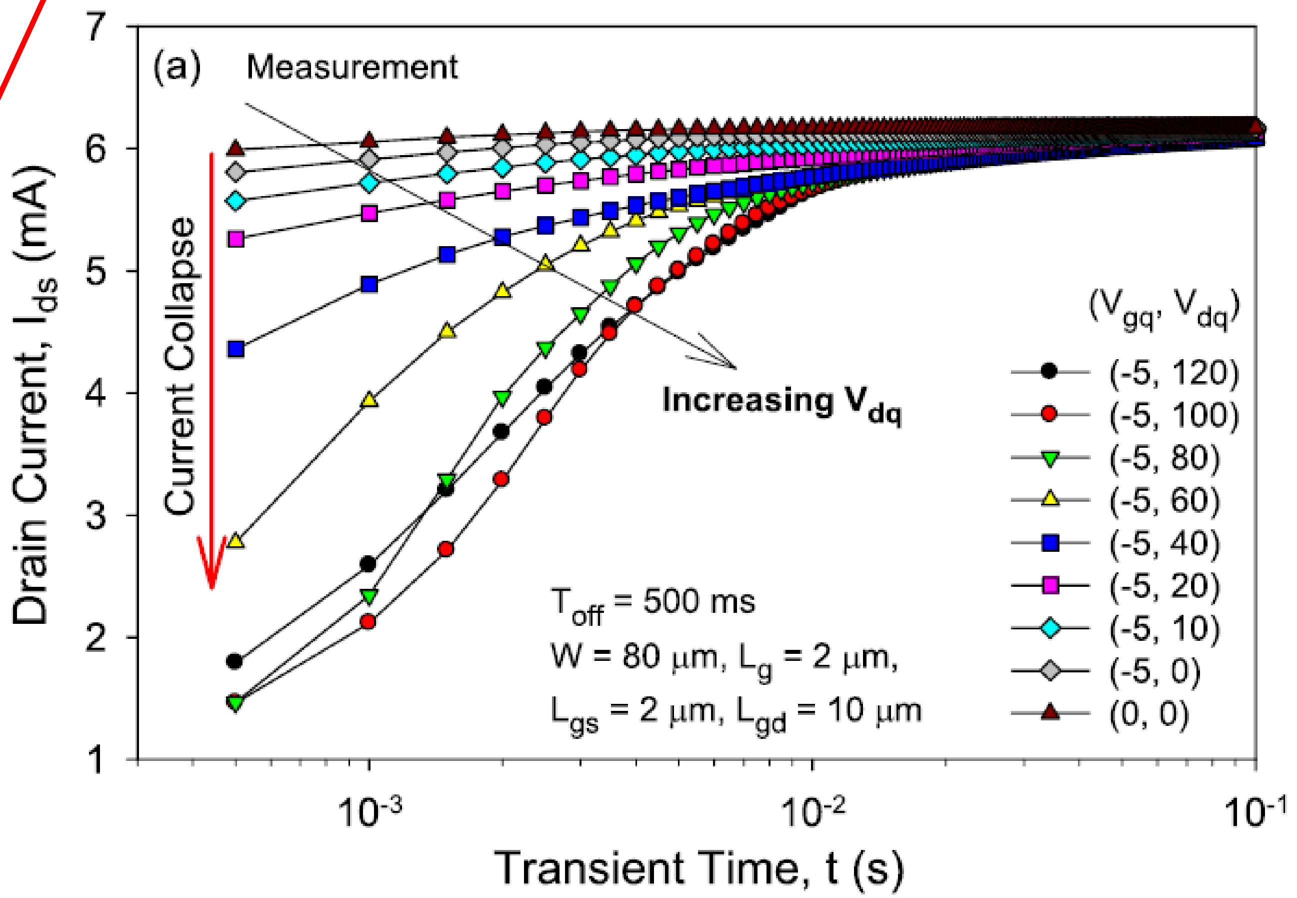
Source: Prof. Yogesh Chauhan

Pulsed IV Measurements

Quiescent Bias Condition

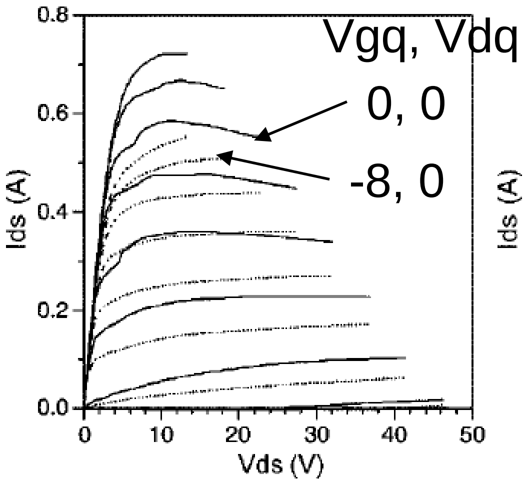
Measurement during pulse condition

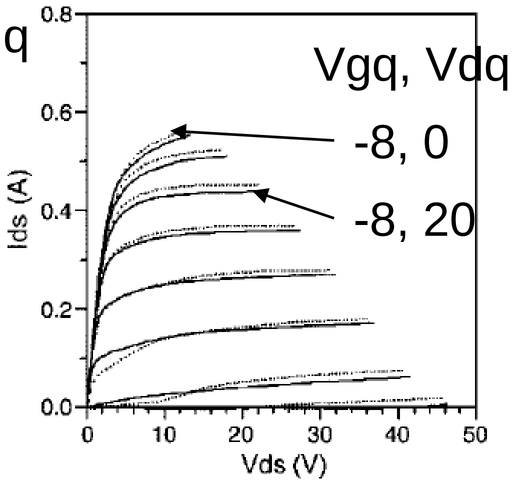


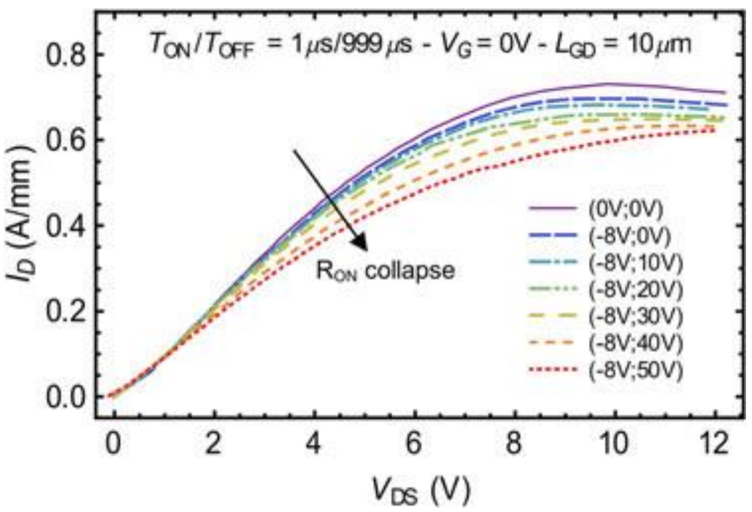


Source: Prof. Yogesh Chauhan

Pulsed IV Measurements







Gate-lag

- **Vdq = 0V**
- **Vgq = Deep OFF condition:**

A strong field through the AlGaN layer. No field through buffer (since Vds = 0). Only surface traps activated.

Drain-lag

- **Vdq = A significantly positive voltage**
- **Vgq = Deep OFF condition:**

A strong field through the AlGaN layer as well as the buffer. Both surface and buffer traps activated.

R_{ON} Collapse:

Trapping reduces the 2DEG concentration and leads to an increased on-state resistance.

Source: Prof. Yogesh Chauhan

Trap Model

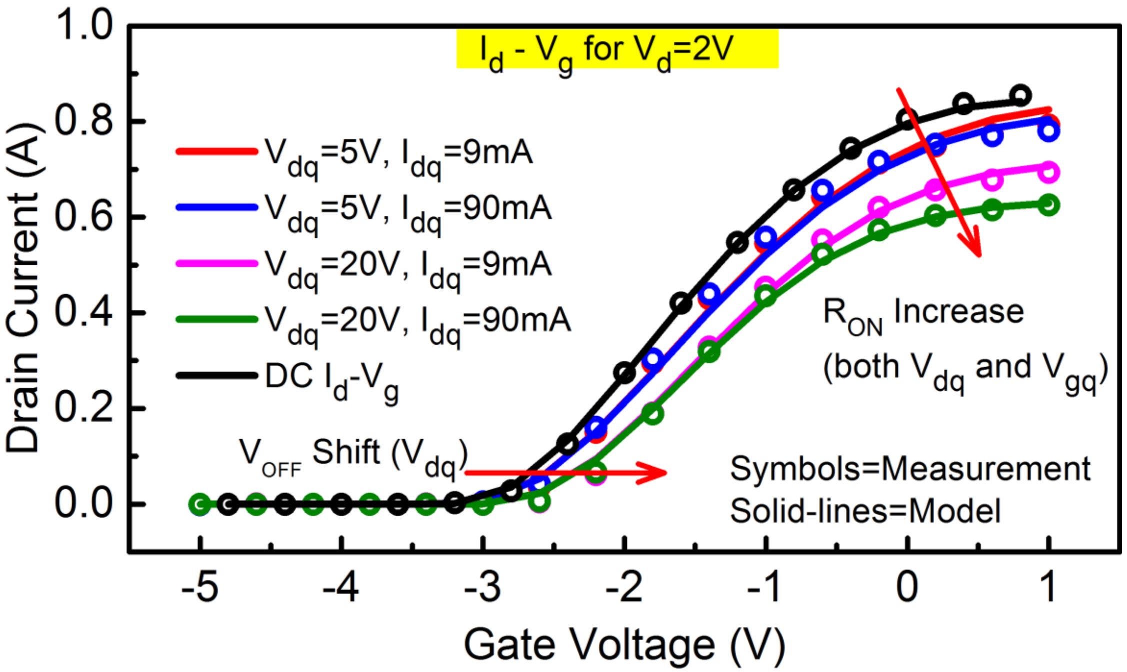
TRAPMOD=2

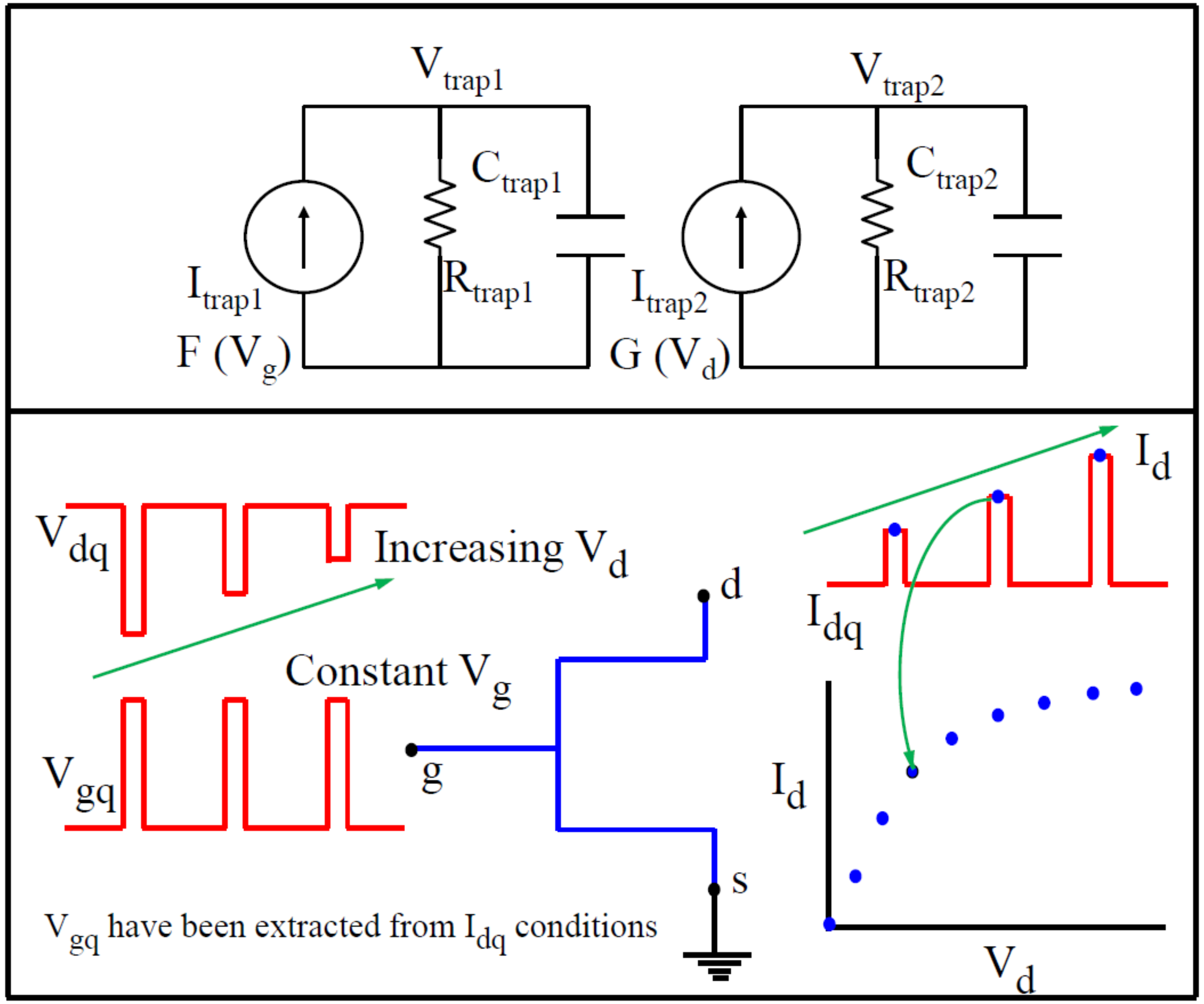
$$V_{OFF}(Trap) = V_{OFF} + (V_{OFFTR} \cdot V_{trap2})$$

$$\eta_0(Trap) = \eta_0 + (\eta_{0TR} \cdot V_{trap2})$$

$$C_{DSCD}(Trap) = C_{DSCD} + (C_{DSCDTR} \cdot V_{trap2})$$

$$R_{ds}(Trap) = R_{ds} - (R_{TR1} \cdot V_{trap1}) + (R_{TR2} \cdot V_{trap2})$$

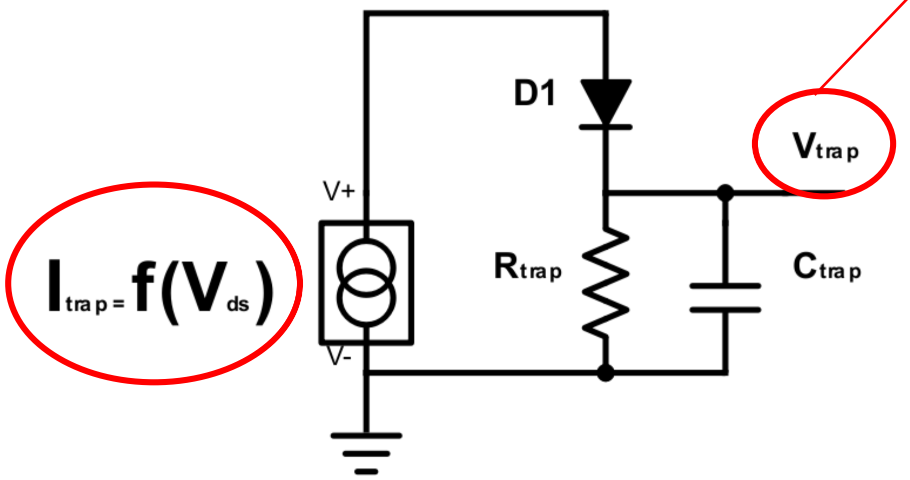




Pulsed-IV Scheme used to simulate the P-IV Characteristics in IC-CAP

Other Trap Models in ASM-HEMT

TRAPMOD=1



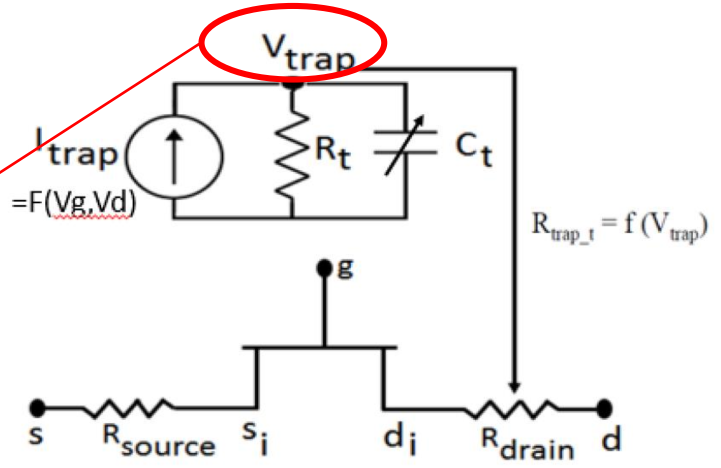
V_{trap} is then used to tune:

- Cut-off voltage
- DIBL
- Source and drain access resistances

TRAPMOD=3

A single sub-circuit to capture the dependence on both V_g and V_d by using V_{gd} instead of V_{gs} and V_{ds} separately.

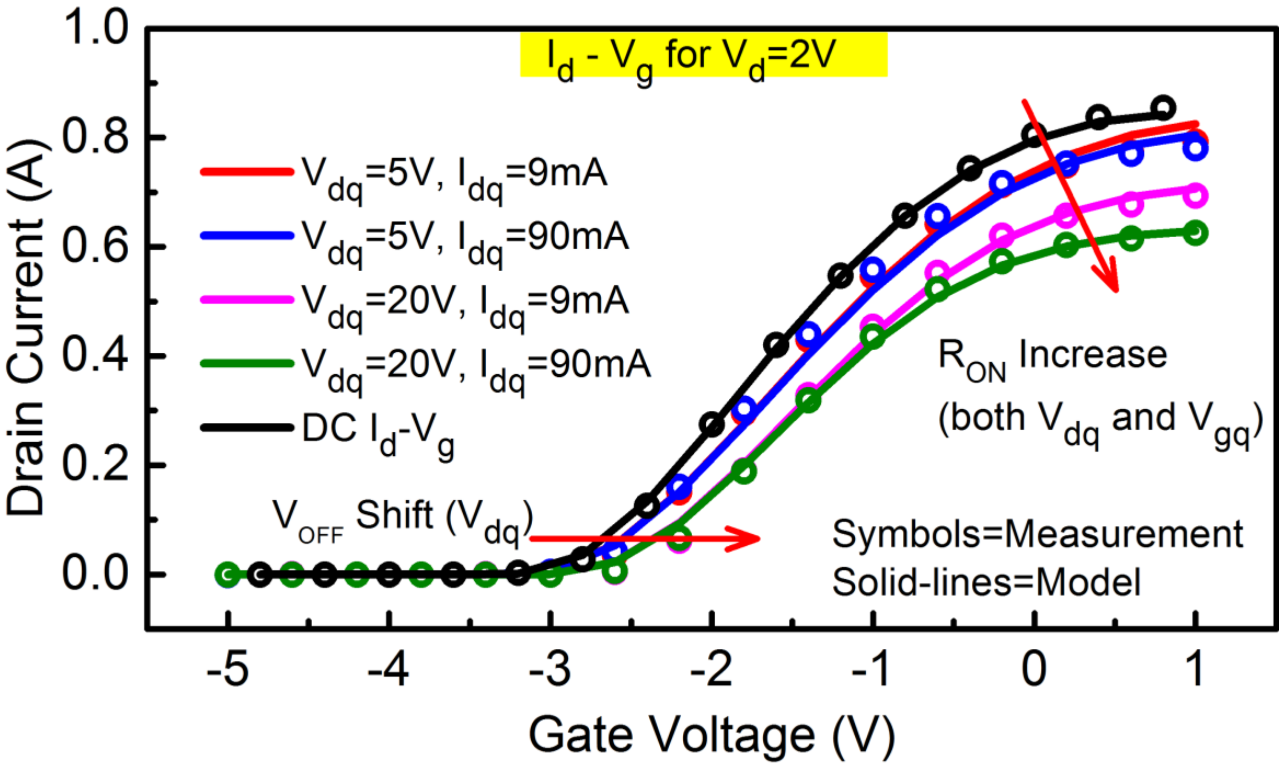
- V_{trap} is used to model the V_{gd} dependence on just the drain-side access region resistance.
- Recommended for modeling the GaN power device dynamic ON-resistance.
- An empirical temperature dependence is also included.



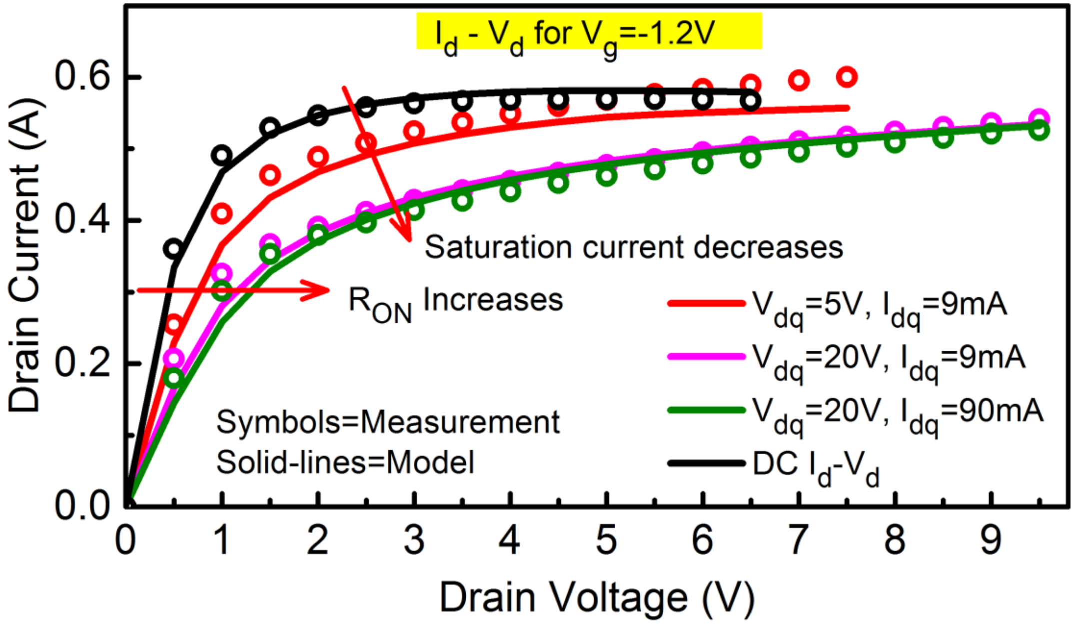
Source: Prof. Yogesh Chauhan

Trap Model

The trap model accurately captures Dynamic-R_{ON} and knee walkout.



Pulsed – IV chacteristics for multiple quiescent conditions



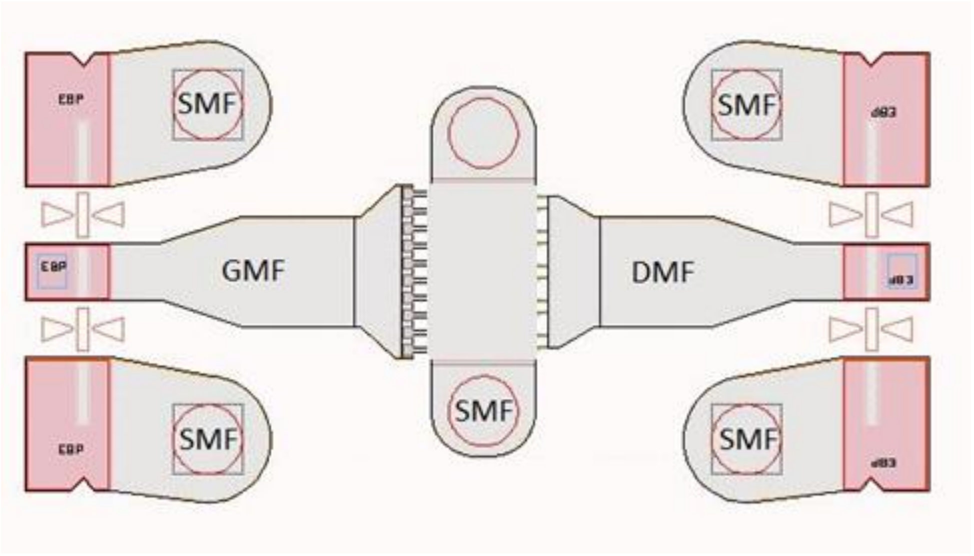
Knee walkout → linearity and efficiency

Pulse Width – 200 ns, Duty-cycle 0.02 %

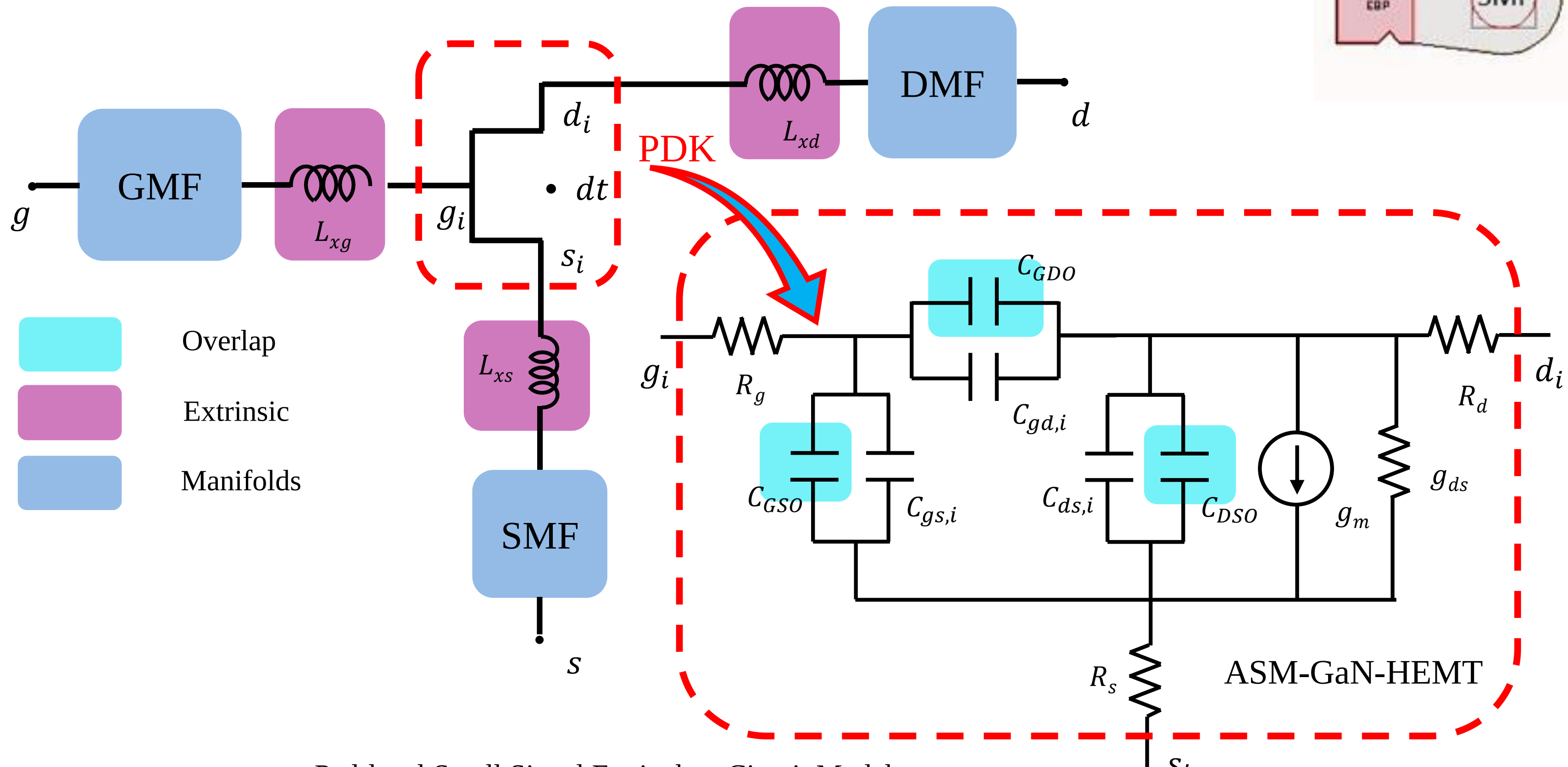
Source: Prof. Yogesh Chauhan

RF Model & Extraction

- Model
  - Core surface potential based PDK
  - Access region resistances included in core
  - Bus-inductances in extrinsics



Device Layout



Pad-level Small Signal Equivalent Circuit Model

CGSO, CGDO, CDSO bias-independent capacitances

intrinsic capacitances: $C_{GS,i}$, $C_{GD,i}$ and $C_{DS,i}$ bias dependent

Source: Prof. Yogesh Chauhan

RF Model & Extraction

- Three step methodology
  - De-embed manifolds
  - Extract the intrinsic core model - Using low frequency Y-parameters
  - Extract Inductances - Using high frequency Y-parameters

Measure S-parameters including de-embedding structures → Convert to Y-parameters → Extract L, C, g_m, g_{ds}, R_g etc.

Source: Prof. Yogesh Chauhan

RF Model & Extraction

Three step methodology

1. De-embed manifolds
2. Extract the intrinsic core model - Using low frequency Y-parameters
3. Extract Inductances - Using high frequency Y-parameters

[1]

$$Y_{11} = \frac{\omega^2 {C_{gg}}^2 R_g}{1+\omega^2 {C_{gg}}^2 R_g^2} + \frac{j\omega C_{gg}}{1+\omega^2 {C_{gg}}^2 R_g^2}$$

$$Y_{12} = -\frac{\omega^2 C_{gd} C_{gg} R_g}{1+\omega^2 {C_{gg}}^2 R_g^2} - \frac{j\omega C_{gd}}{1+\omega^2 {C_{gg}}^2 R_g^2}$$

$$Y_{21} = \frac{g_m - \omega^2 C_{gd} C_{gg} R_g}{1+\omega^2 {C_{gg}}^2 R_g^2} - \frac{j\omega (C_{gd} + g_m C_{gg} R_g)}{1+\omega^2 {C_{gg}}^2 R_g^2}$$

$$Y_{22} = g_{ds} + \frac{\omega^2 (C_{gs} C_{gd} R_g + R_g C_{gd} C_{gg} (1+g_m R_g))}{1+\omega^2 {C_{gg}}^2 R_g^2} + j\omega C_{ds} + \frac{j\omega C_{gd} (1+g_m R_g) + j\omega^3 C_{gs} C_{gd} C_{gg} R_g^2}{1+\omega^2 {C_{gg}}^2 R_g^2}$$

[1]

- The effect of bus-inductances is ignored at low frequencies (assumption)
- Drain & Source access region resistances ignored from hand analysis (not an assumption, it is an advantage)
- Ignore some terms at low frequency (~ 10 GHz) (assumption)
- Very simple – only need to adjust overlap capacitances & gate finger resistances (advantage)

$$[\mathbf{Y}] \approx \begin{bmatrix} \omega^2 {C_{gg}}^2 R_g + j\omega C_{gg} & -\omega^2 C_{gd} C_{gg} R_g - j\omega C_{gd} \\ g_m - j\omega (C_{gd} + g_m C_{gg} R_g) & g_{ds} + j\omega (C_{ds} + C_{gd}(1+g_m R_g)) \end{bmatrix}$$

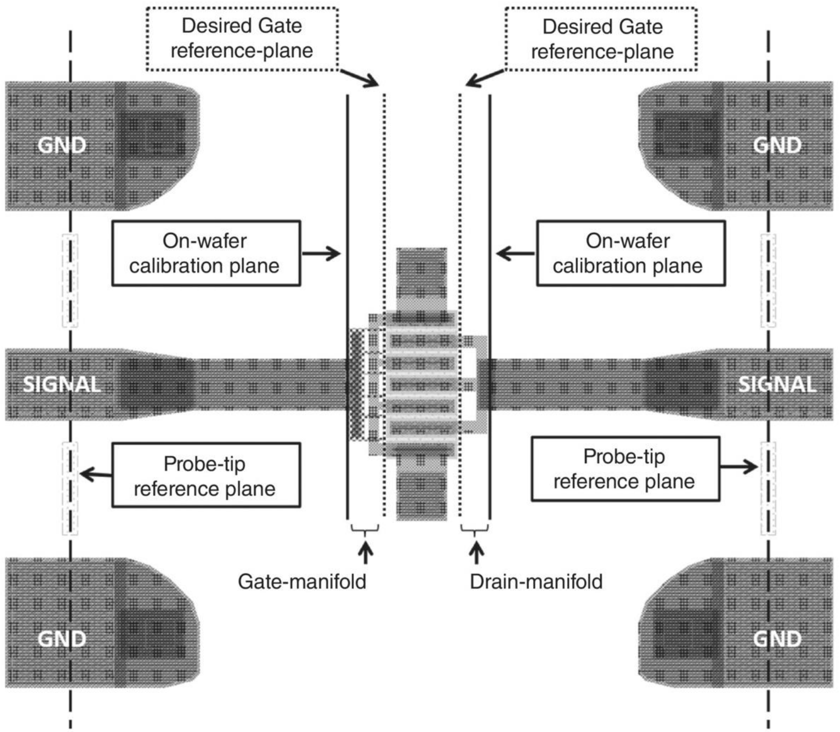
$$\begin{bmatrix} C_{gs} & C_{gd} & C_{ds} \\ g_m & g_{ds} & R_g \end{bmatrix}$$

$$\begin{bmatrix} (\mathrm{Im}[Y_{11}] + \mathrm{Im}[Y_{12}])/\omega & -\mathrm{Im}[Y_{12}]/\omega & \mathrm{Im}[Y_{22}]/\omega - C_{gd}(1+g_m R_g) \\ \mathrm{Re}[Y_{21}] & \mathrm{Re}[Y_{22}] & \mathrm{Re}[Y_{11}]/(\omega^2 C_{gg}^2) \end{bmatrix}$$

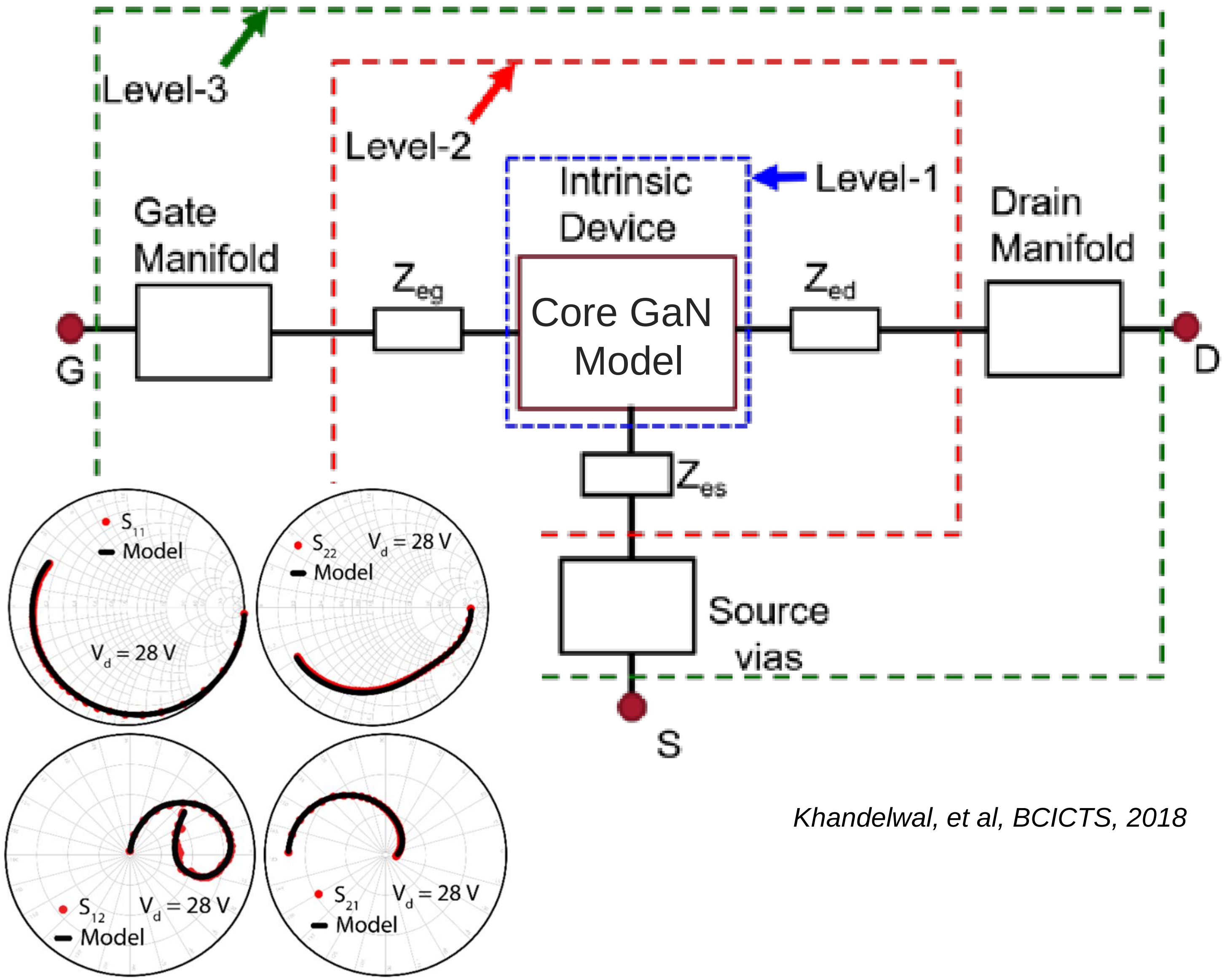
[1] I. Kwon *et al.*, *IEEE Trans. Microw. Theory Techn.*, **50 (6),** [2002]

Source: Prof. Yogesh Chauhan

RF Model & Extraction



Nonlinear Circuit Simulation and Modeling, Cambridge University press



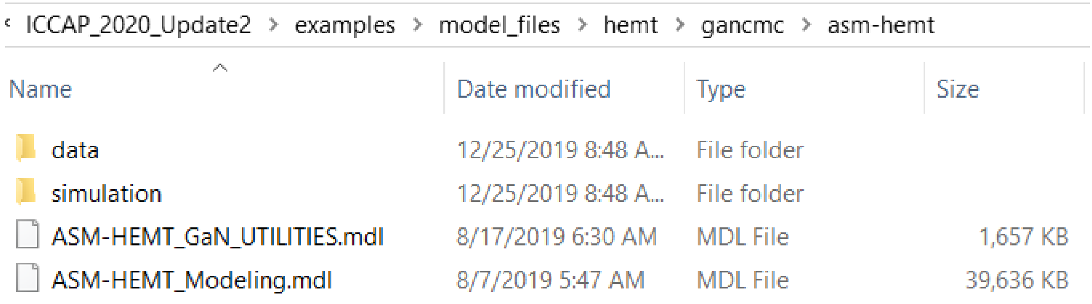
Khandelwal, et al, BCICTS, 2018

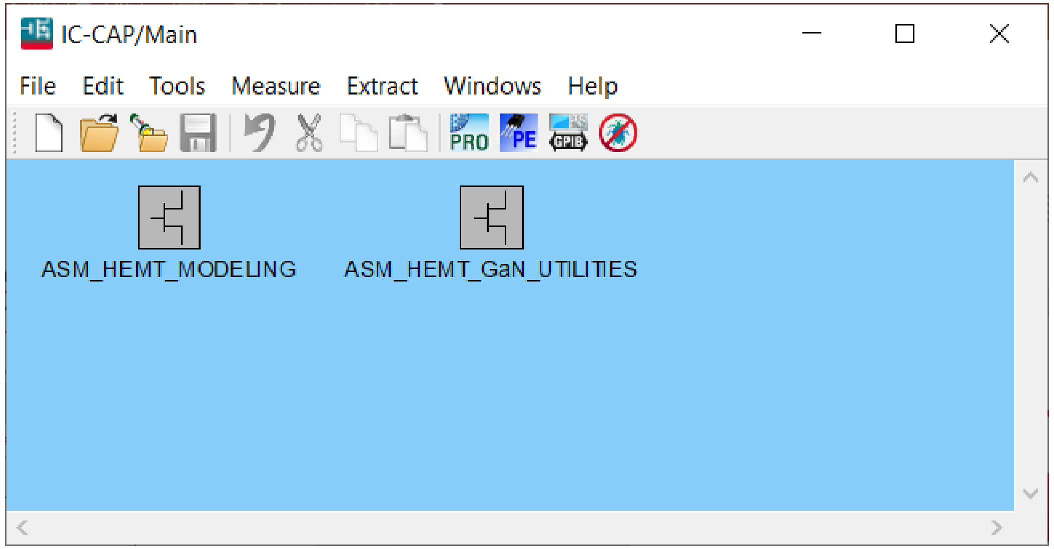
KEYSIGHT TECHNOLOGIES

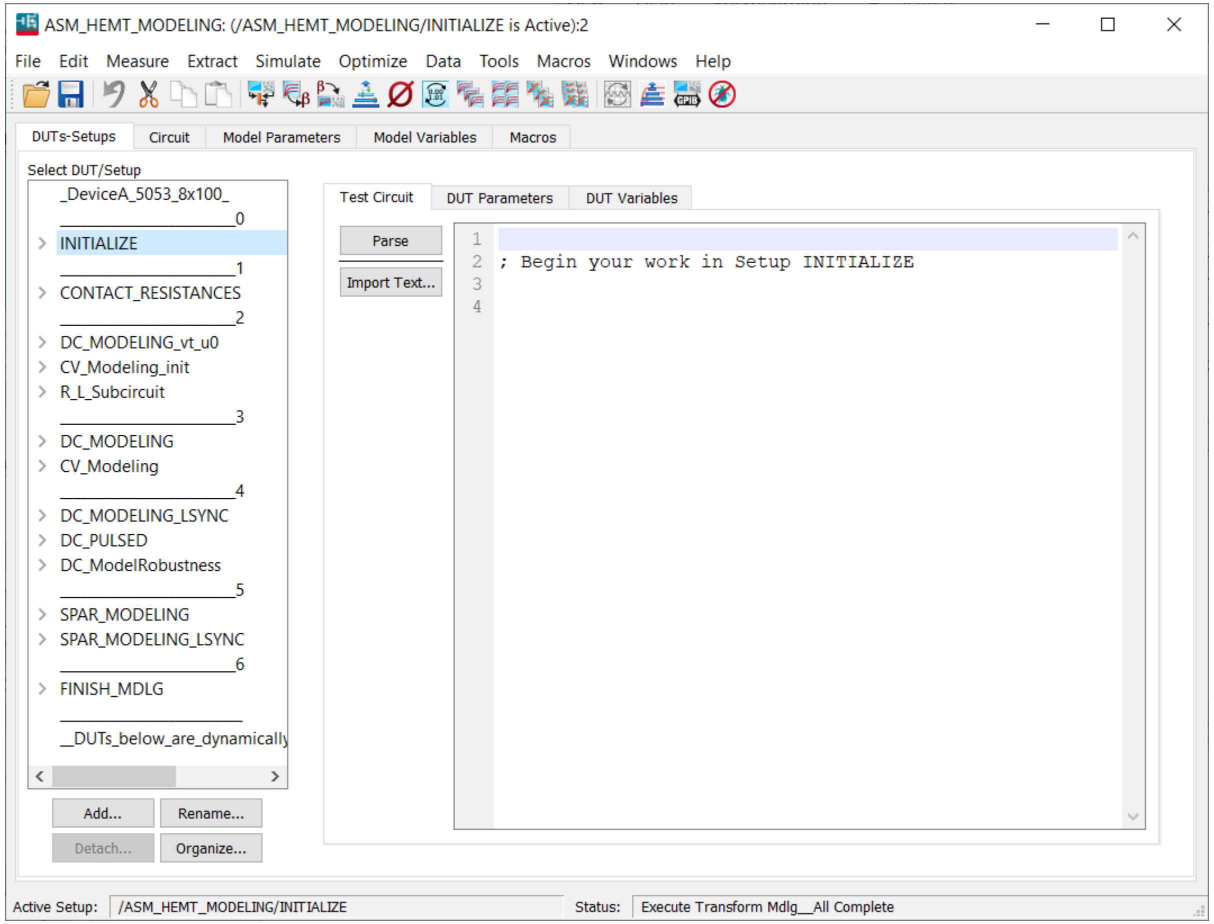
Introduction to CMC Modeling Kit (ASM-HEMT) in IC-CAP

Open Example Model Files

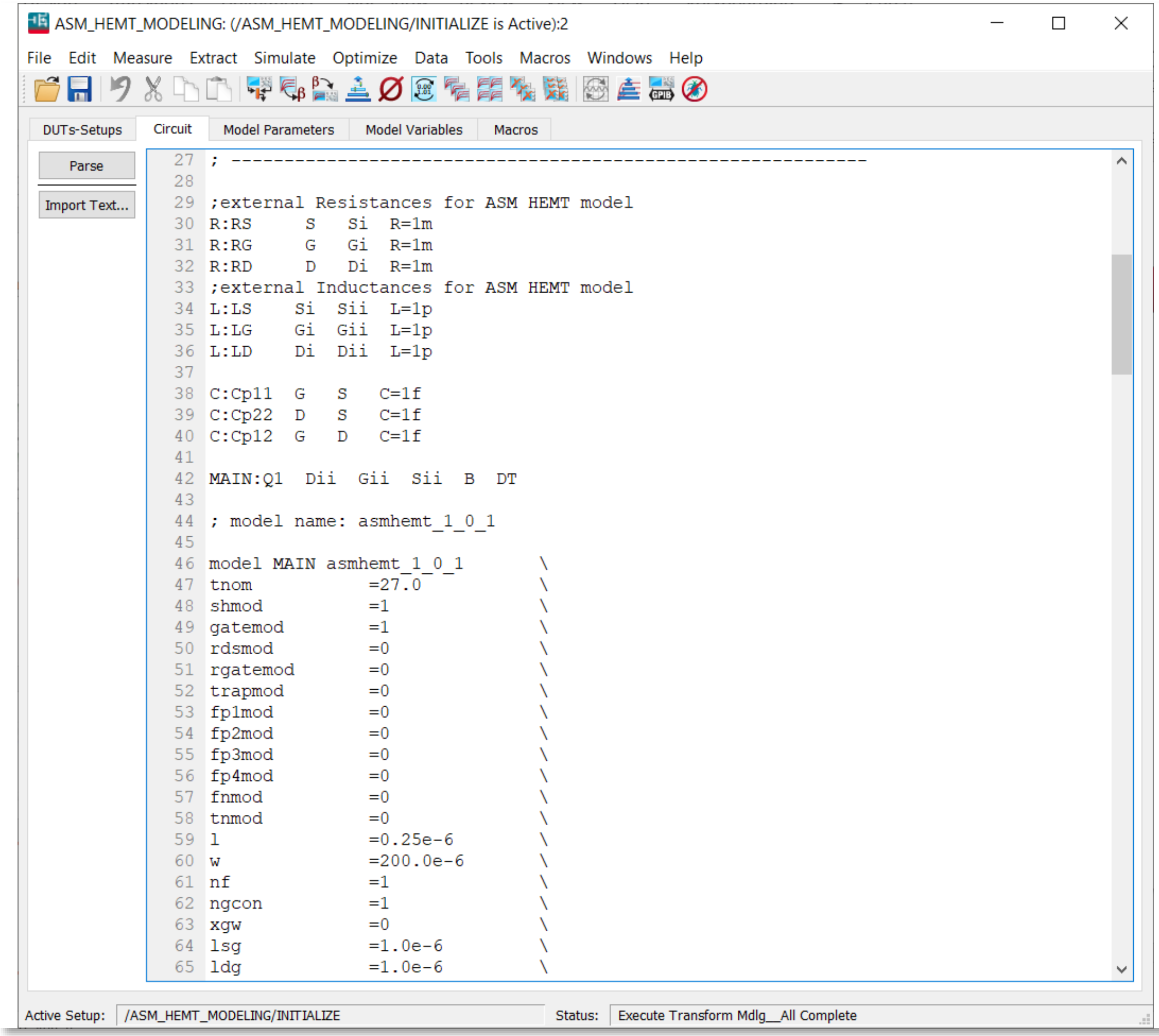
ASM-HEMT

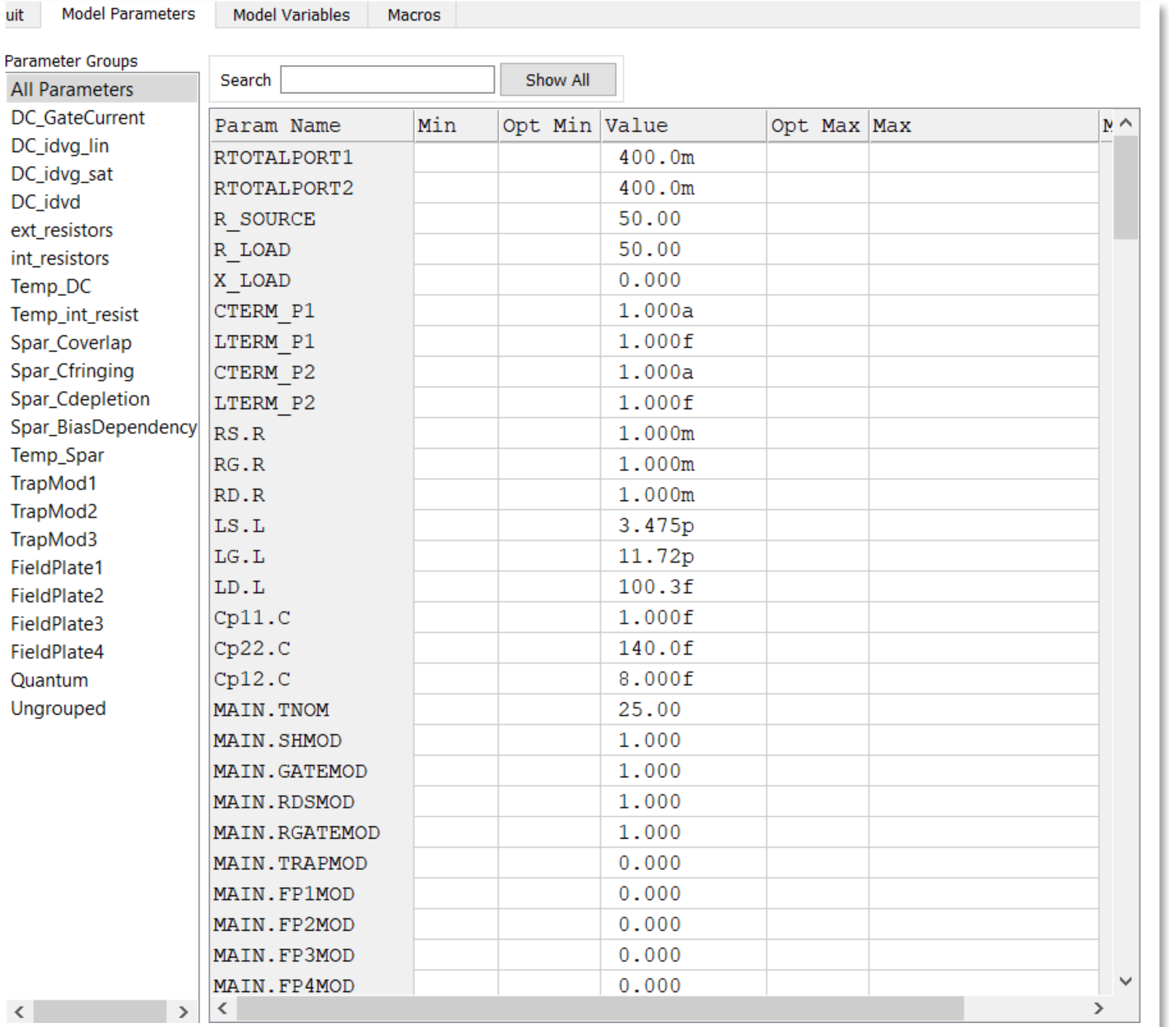




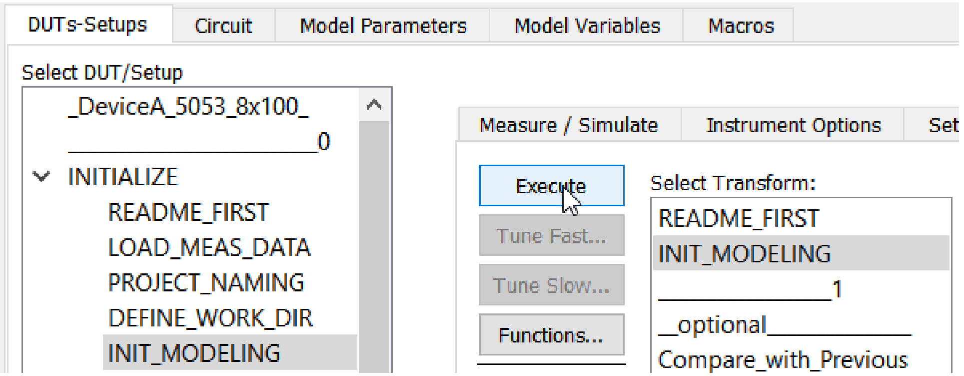


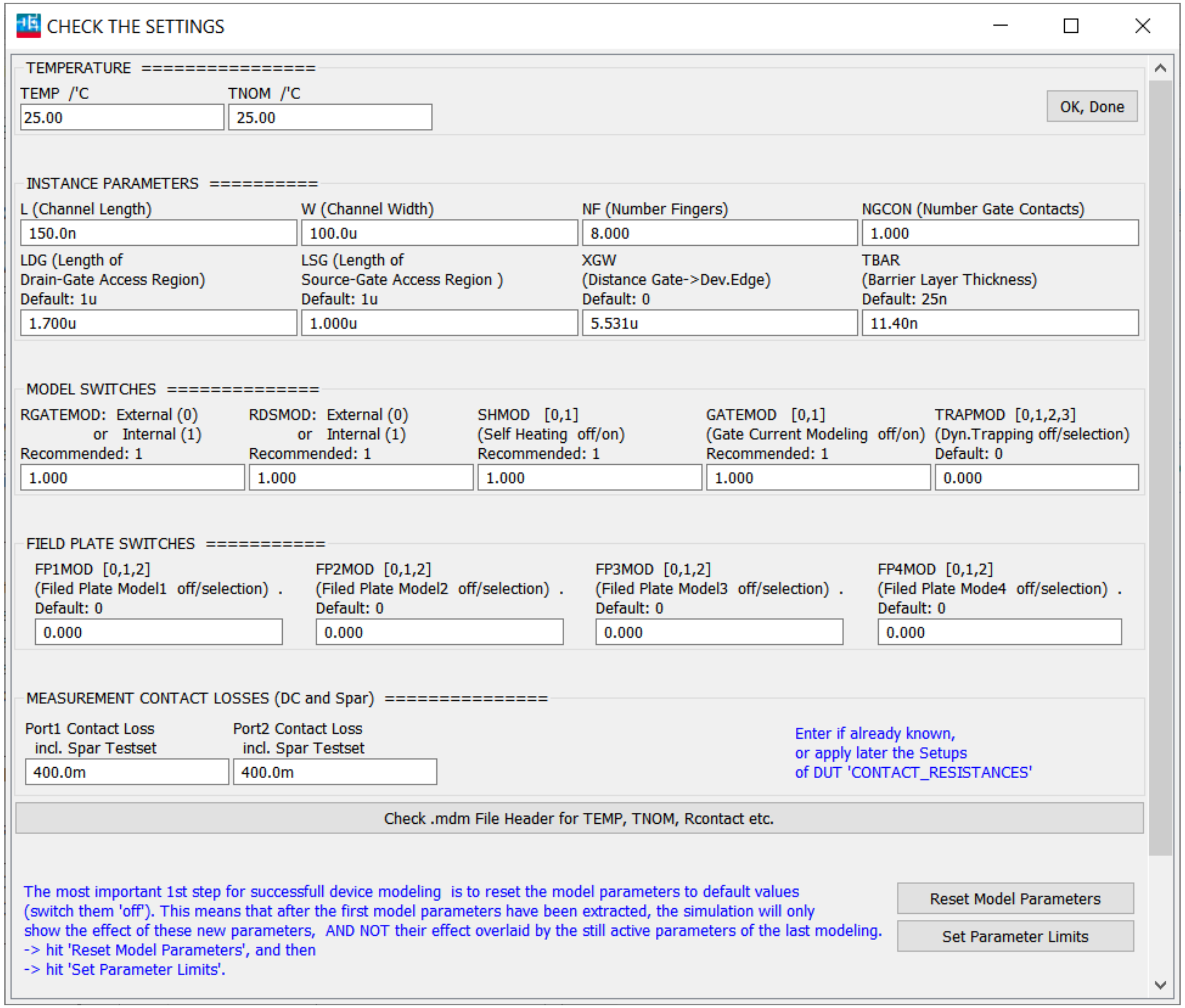
Model Circuit and Parameters



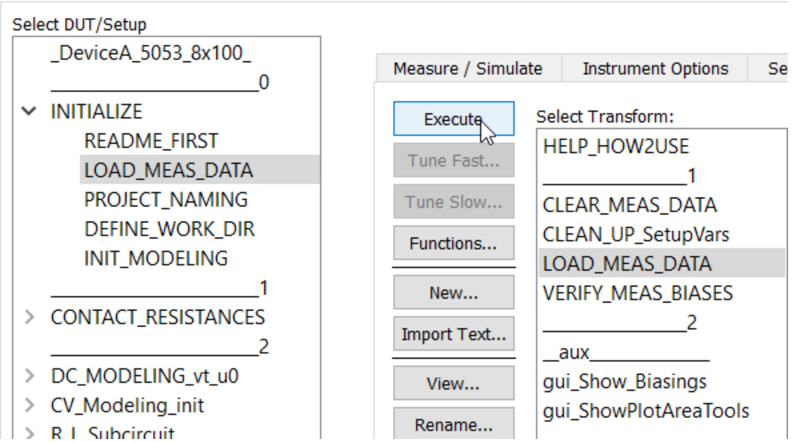


Initialize Modeling



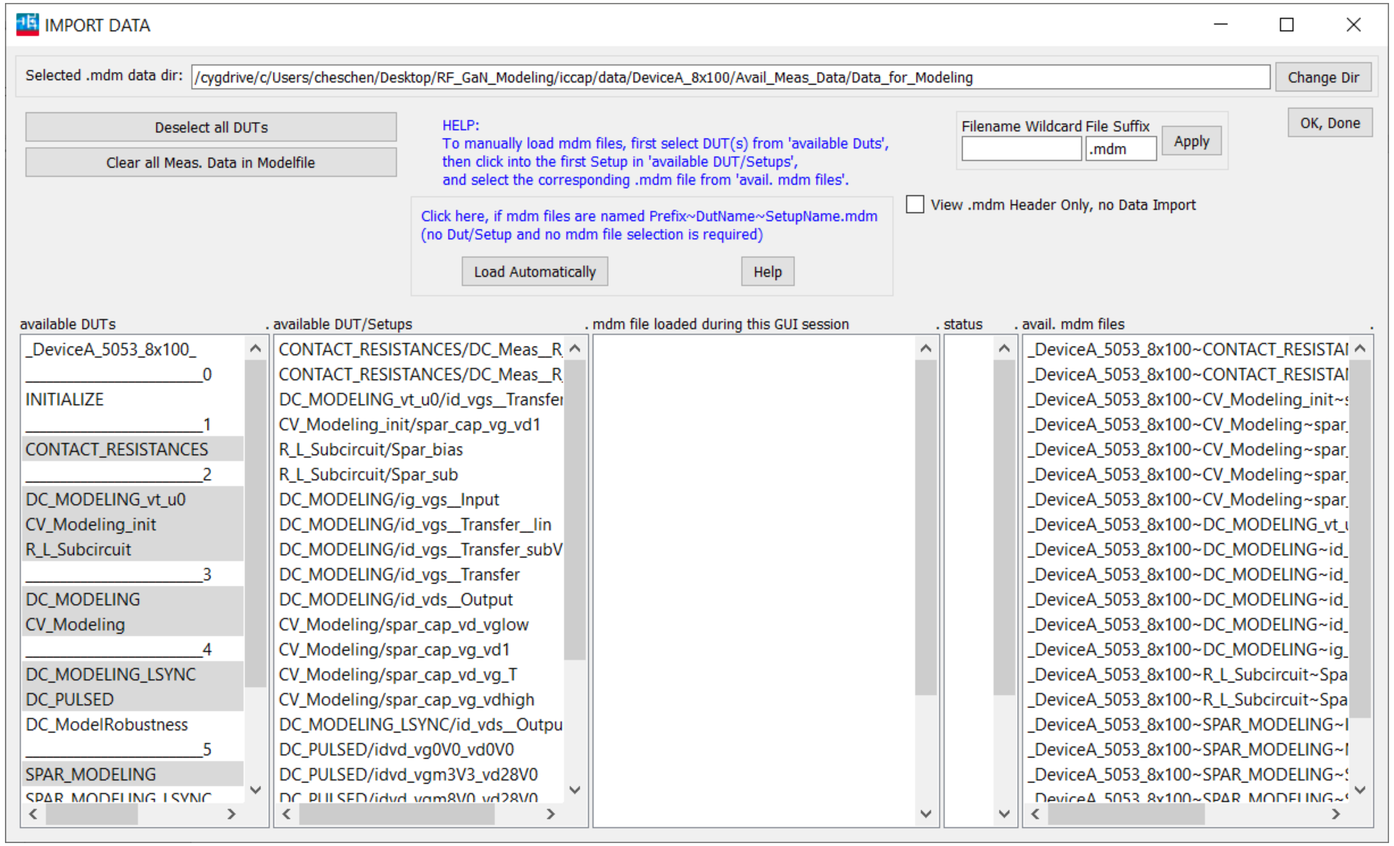


Load Data for Modeling

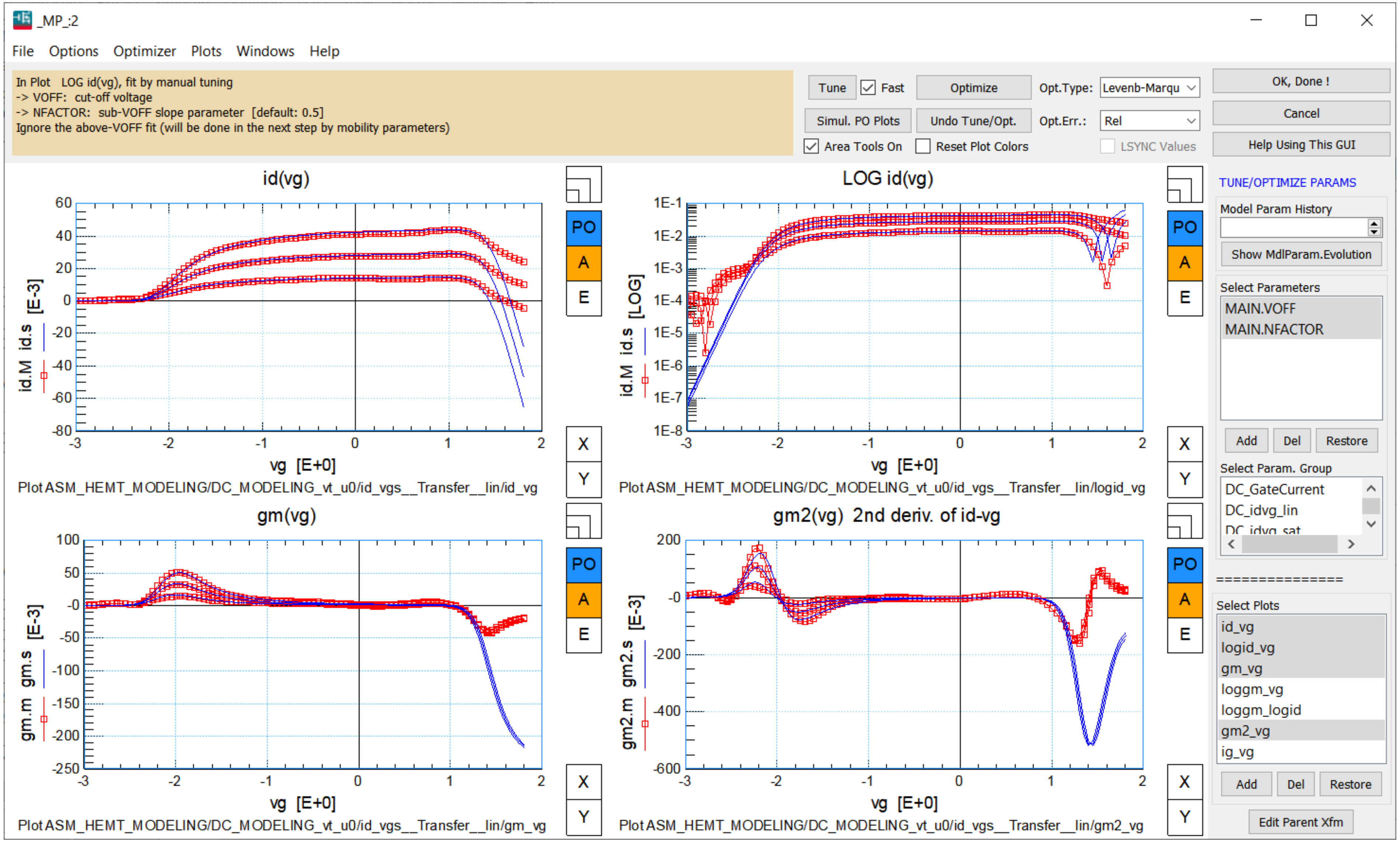


prefix Dut name Setup name

_DeviceA_5053_8x100~DC_MODELING~ig_vgs__Input

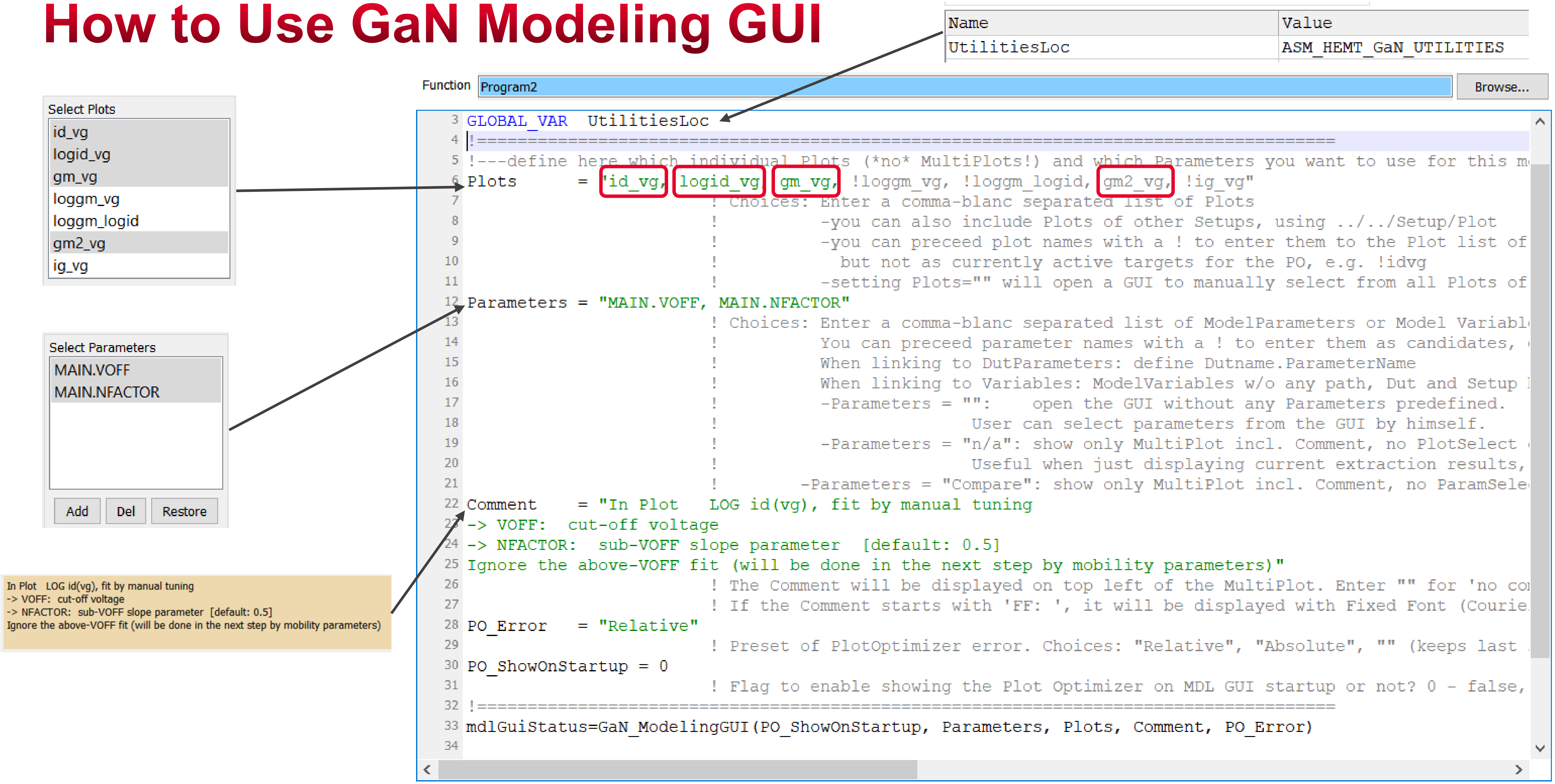


GaN Modeling GUI

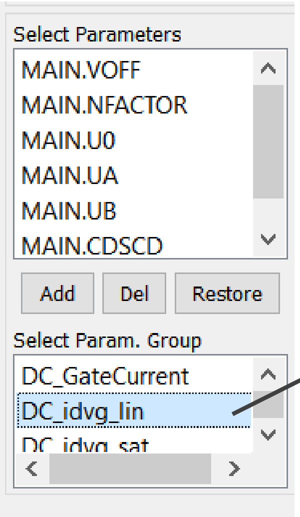


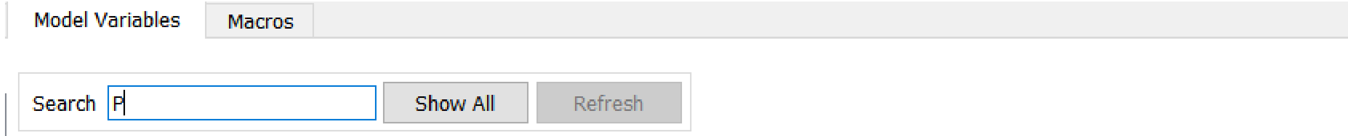
KEYSIGHT TECHNOLOGIES

How to Use GaN Modeling GUI



How to Define Parameter Groups





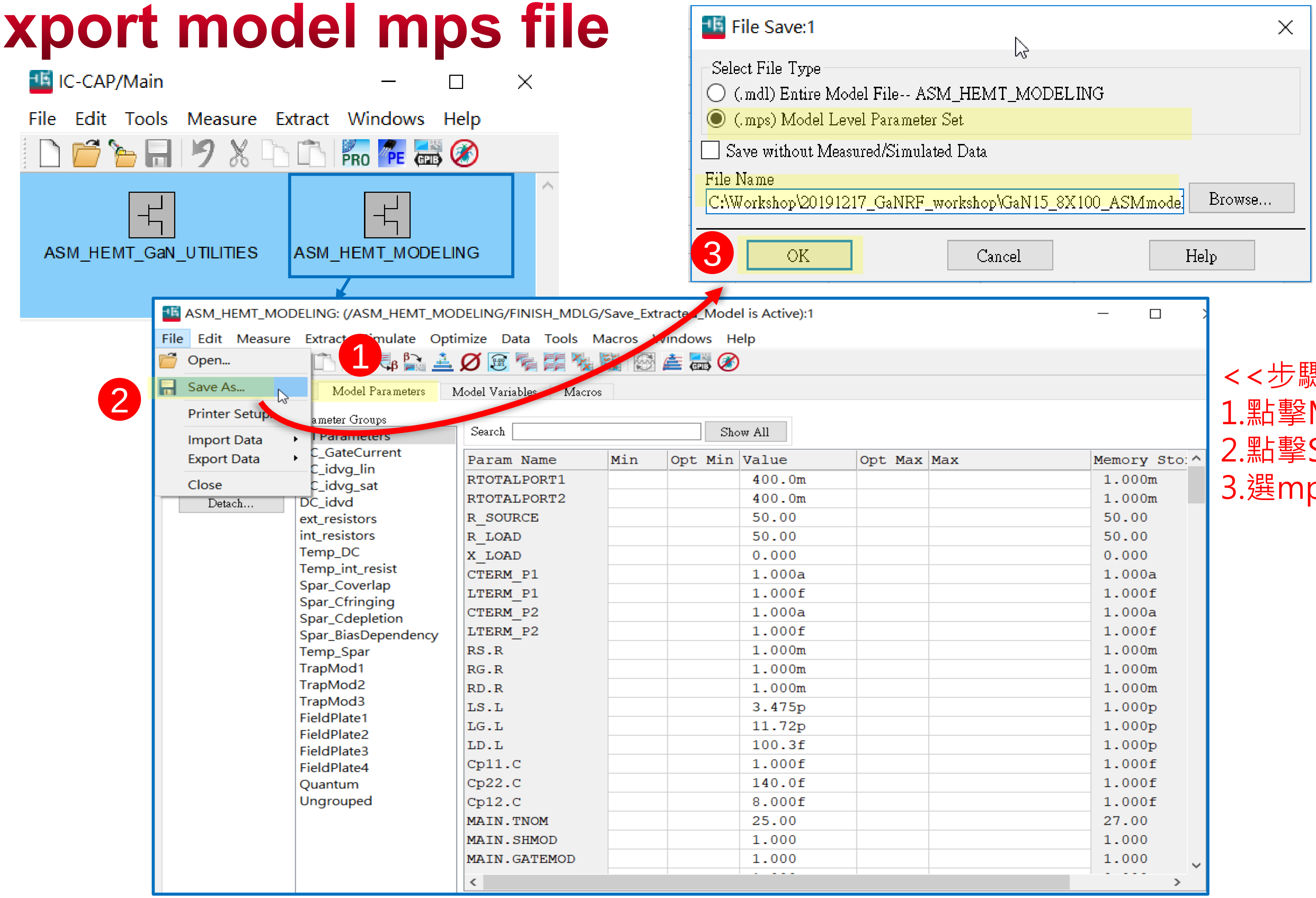
Name	Value
PARAMGROUP_DC_GateCurrent	MAIN.IGSDIO,MAIN.NJGS
PARAMGROUP_DC_idvg_lin	MAIN.VOFF,MAIN.NFACTOR,MAIN.U0,MAIN.UA,MAIN.UB,M…
PARAMGROUP_DC_idvg_sat	MAIN.ETA0,MAIN.VDSCALE,MAIN.RTH0
PARAMGROUP_DC_idvd	MAIN.LAMBDA,MAIN.VSAT,MAIN.DELTA,MAIN.THESAT
PARAMGROUP_ext_resistors	MAIN.RDSMOD,MAIN.RGATEMOD,RG.R,RS.R,RD.R
PARAMGROUP_int_resistors	MAIN.RDSMOD,MAIN.RGATEMOD,MAIN.RSHG,MAIN.RSC,MAI…
PARAMGROUP_Temp_DC	MAIN.UTE,MAIN.KT1,MAIN.AT,MAIN.KTGS
PARAMGROUP_Temp_int_resist	MAIN.KNS0,MAIN.ATS,MAIN.UTES,MAIN.UTED,MAIN.KRSC…
PARAMGROUP_Spar_Coverlap	MAIN.CGSO,MAIN.CGDO,MAIN.CDSO,MAIN.CBDO,MAIN.CBSO
PARAMGROUP_Spar_Cfringing	MAIN.CFG,MAIN.CFD,MAIN.CFGD,MAIN.CFGD0,MAIN.CFGD…
PARAMGROUP_Spar_Cdepletion	MAIN.CJ0,MAIN.VBI,MAIN.MZ,MAIN.AJ,MAIN.DJ
PARAMGROUP_Spar_BiasDependency	MAIN.VDSATCV,MAIN.CGDL
PARAMGROUP_Temp_Spar	MAIN.KTVBI,MAIN.KTCFG,MAIN.KTCFGD
PARAMGROUP_TrapMod1	MAIN.TRAPMOD,MAIN.CDLAG,MAIN.RDLAG,MAIN.IDIO,MAI…
PARAMGROUP_TrapMod2	MAIN.TRAPMOD,MAIN.CTRAP1,MAIN.RTRAP1,MAIN.CTRAP2…
PARAMGROUP_TrapMod3	MAIN.TRAPMOD,MAIN.CTRAP3,MAIN.RTRAP3,MAIN.VATRAP…
PARAMGROUP_FieldPlate1	MAIN.FP1MOD,MAIN.LFP1,MAIN.DFP1,MAIN.IMINFP1,MAI…
PARAMGROUP_FieldPlate2	MAIN.FP2MOD,MAIN.LFP2,MAIN.DFP2,MAIN.IMINFP2,MAI…
PARAMGROUP_FieldPlate3	MAIN.FP3MOD,MAIN.LFP3,MAIN.DFP3,MAIN.IMINFP3,MAI…
PARAMGROUP_FieldPlate4	MAIN.FP4MOD,MAIN.LFP4,MAIN.DFP4,MAIN.IMINFP4,MAI…
PARAMGROUP_Quantum	MAIN.ADOSI,MAIN.BDOSI, MAIN.QM0I

Live Demo for GaN Modeling GUI

Export Model to ADS for Load-Pull Simulation

KEYSIGHT TECHNOLOGIES

Export model mps file



Param Name	Min	Opt Min	Value	Opt Max	Max	Memory Sto:
RTOTALPORT1			400.0m			1.000m
RTOTALPORT2			400.0m			1.000m
R_SOURCE			50.00			50.00
R_LOAD			50.00			50.00
X_LOAD			0.000			0.000
CTERM_P1			1.000a			1.000a
LTERM_P1			1.000f			1.000f
CTERM_P2			1.000a			1.000a
LTERM_P2			1.000f			1.000f
RS.R			1.000m			1.000m
RG.R			1.000m			1.000m
RD.R			1.000m			1.000m
LS.L			3.475p			1.000p
LG.L			11.72p			1.000p
LD.L			100.3f			1.000p
Cp11.C			1.000f			1.000f
Cp22.C			140.0f			1.000f
Cp12.C			8.000f			1.000f
MAIN.TNOM			25.00			27.00
MAIN.SHMOD			1.000			1.000
MAIN.GATEMOD			1.000			1.000

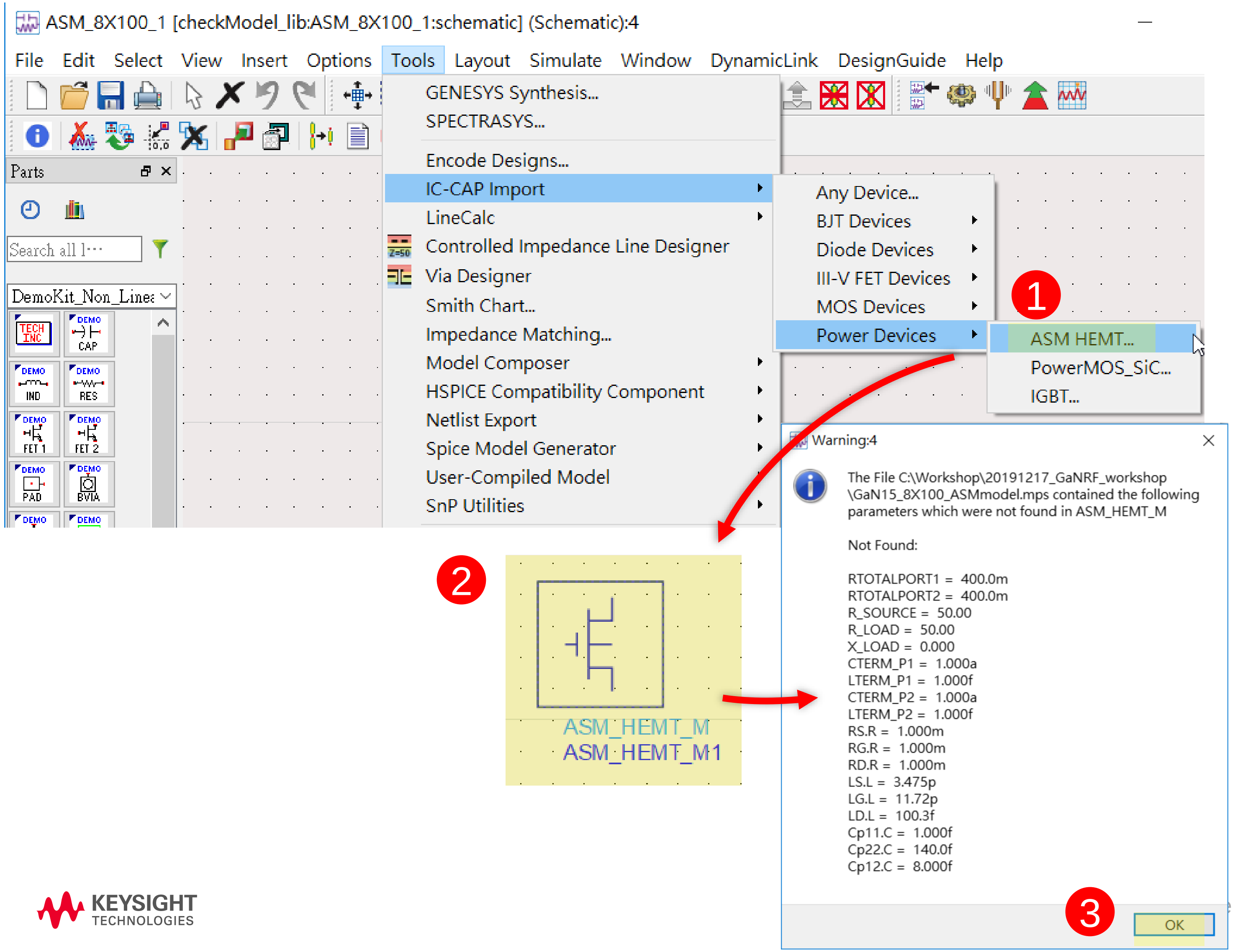
<<步驟>>

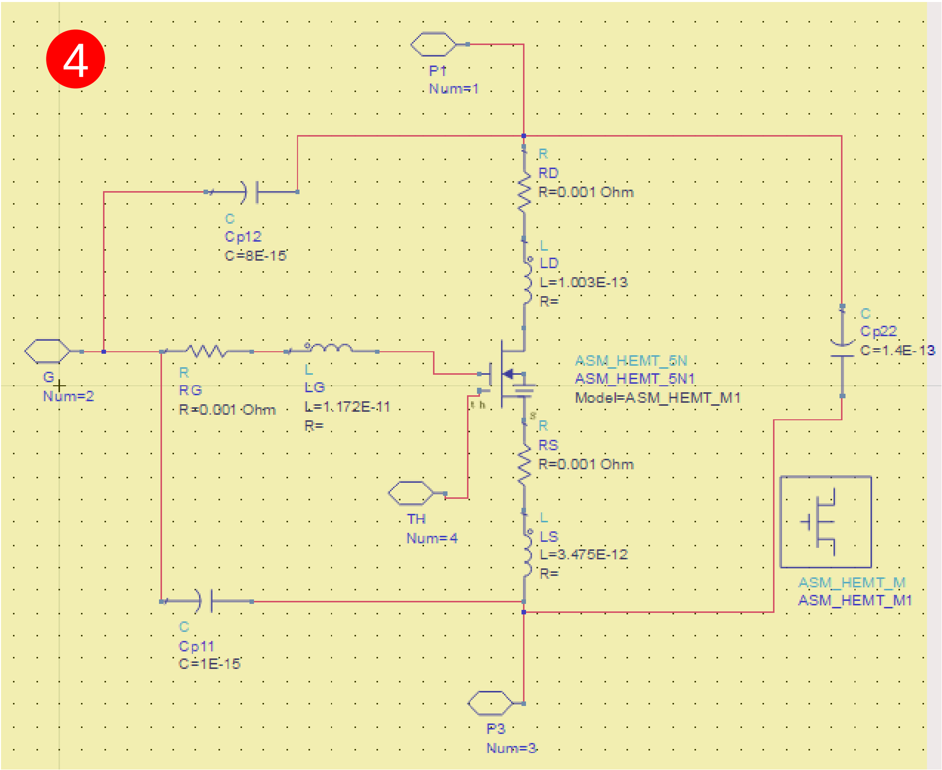
1.點擊Model Parameters頁面

2.點擊Save As

3.選mps & 設置路徑 ➔ 取得mps file

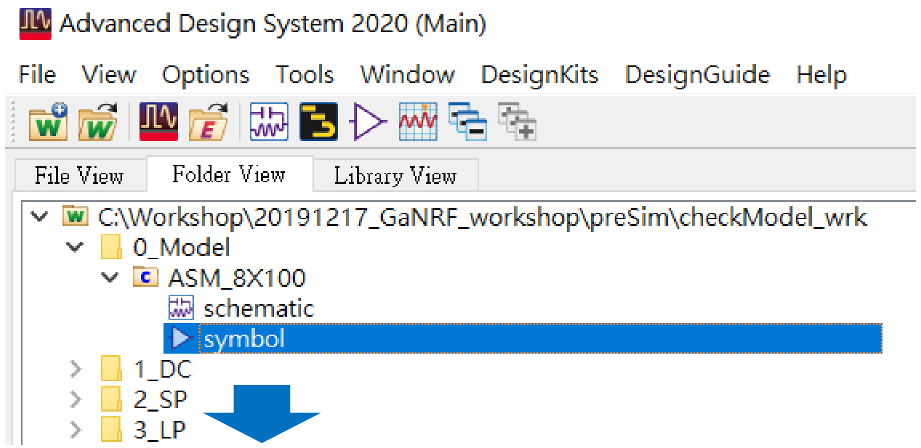
將Model導入ADS

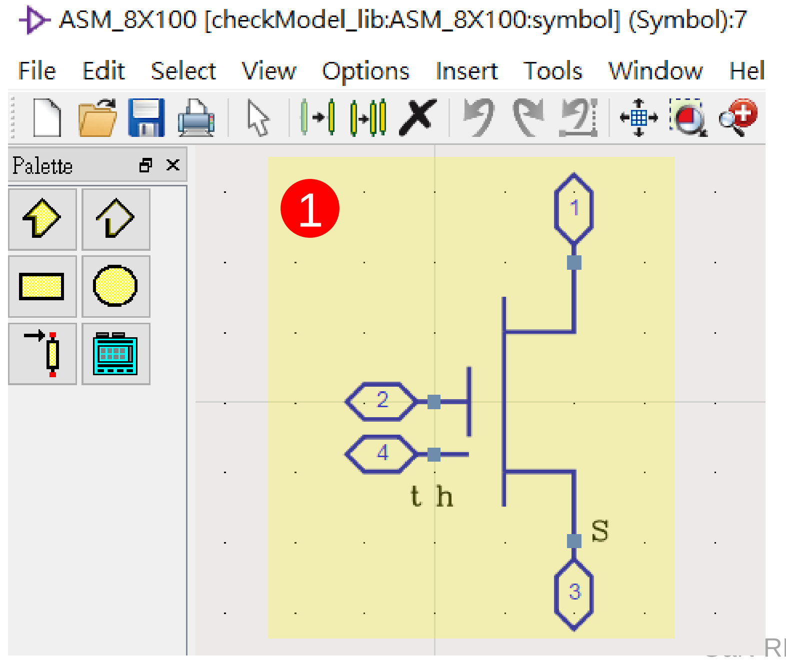


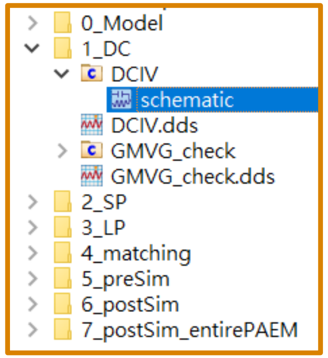


<<步驟>>
1.創建schematic後,使用tools進行參數導入
2.自動帶出 ASM_HEMT_M model card
3.由于有外部參數,因此有Warning(需自行建構)
4.自行建構外部參數與ASM_HEMT_5N連接

建立Symbol & 檢測基本電性





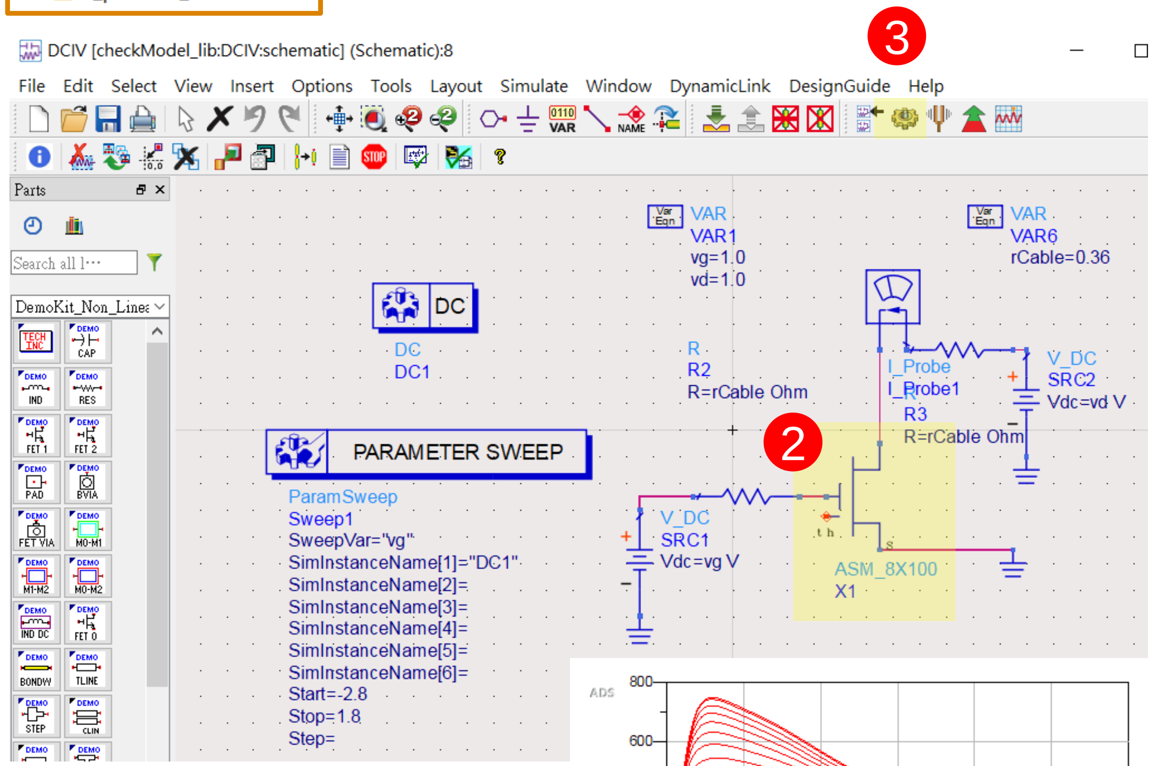


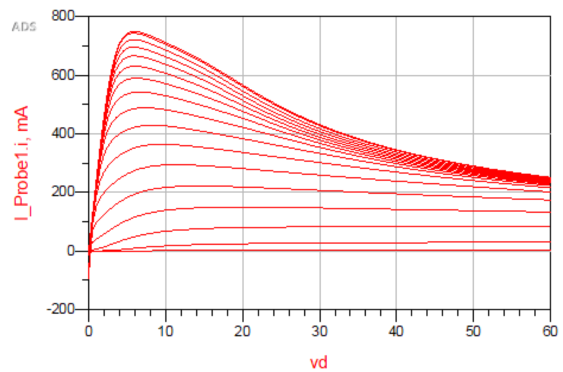
<<步驟>>

1.建立4T symbol

2.放入schematic

3.點擊simulation



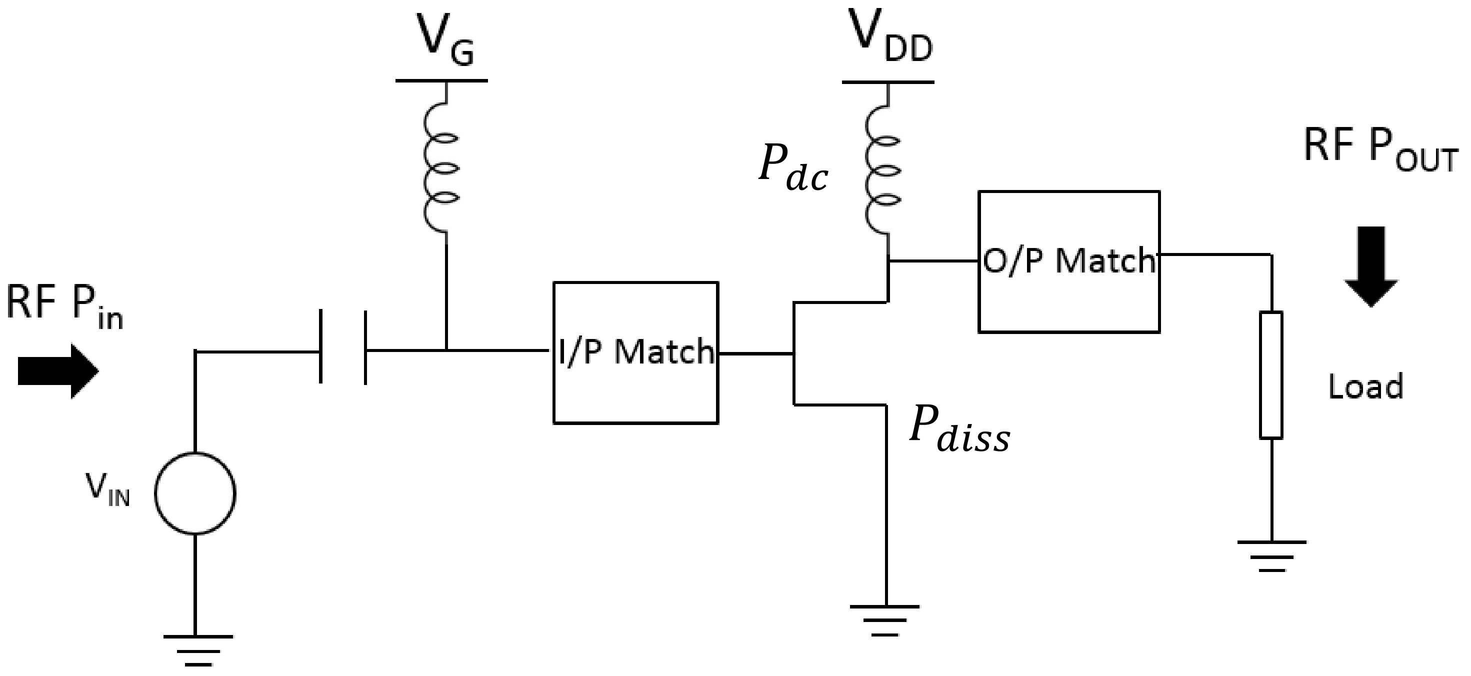


Power Amplifier Design Goals

$$Gain = \frac{P_{out}}{P_{in}}$$

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}}$$

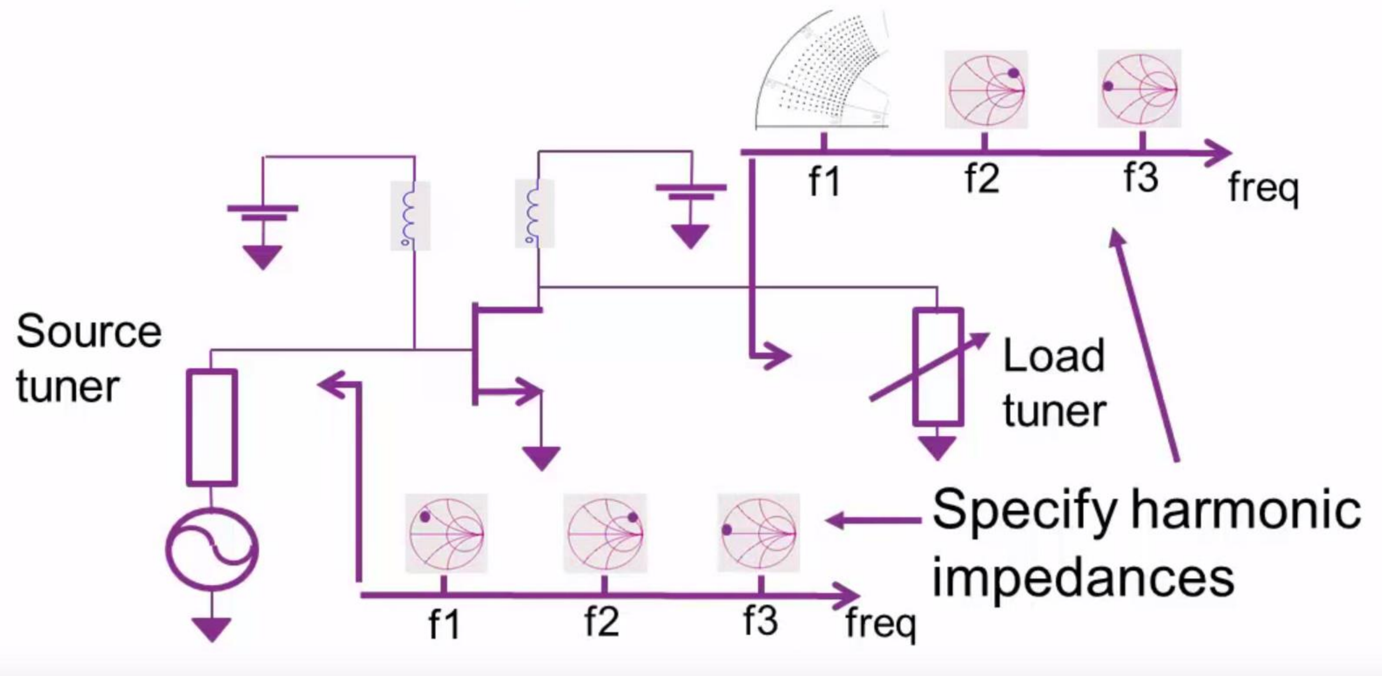
$$Drain\ Efficiency = \frac{P_{out}}{P_{dc}}$$

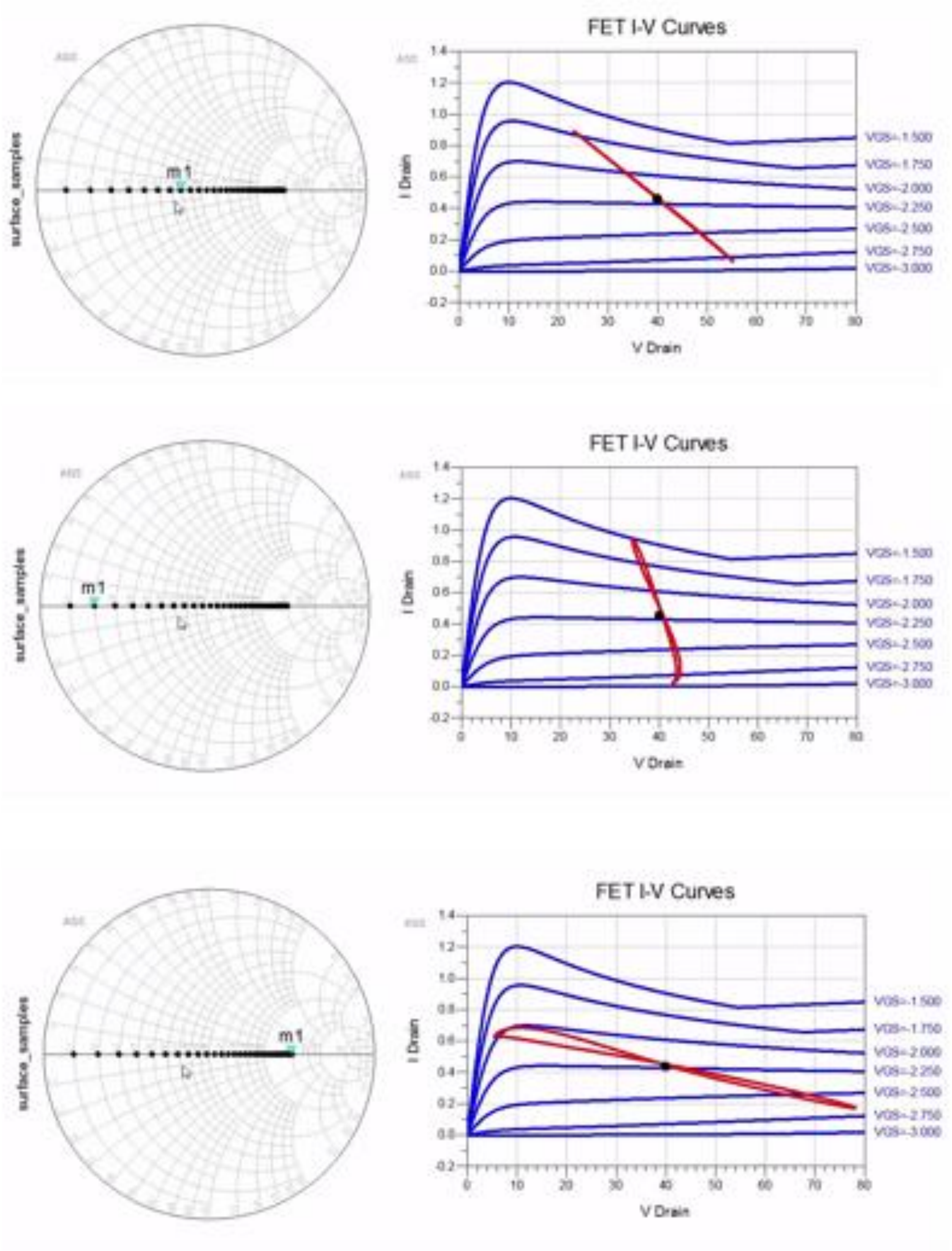


Source: Prof. Yogesh Chauhan

Load Pull Technique

- Determine Optimum load impedance for maximum Pout and PAE performance
- Specify matching networks
- Understand tradeoffs!

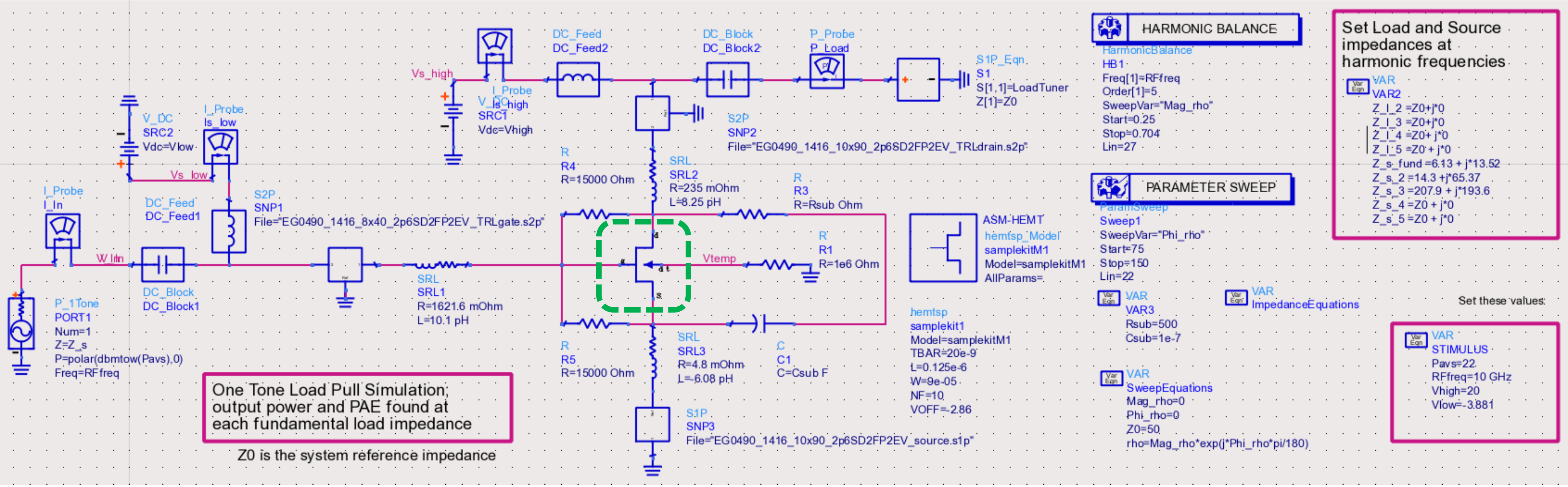




[M. S. Hashmi *et. al*, *IEEE Instrum. Meas. Mag.*, **16 (2)**, Feb., (2013)]

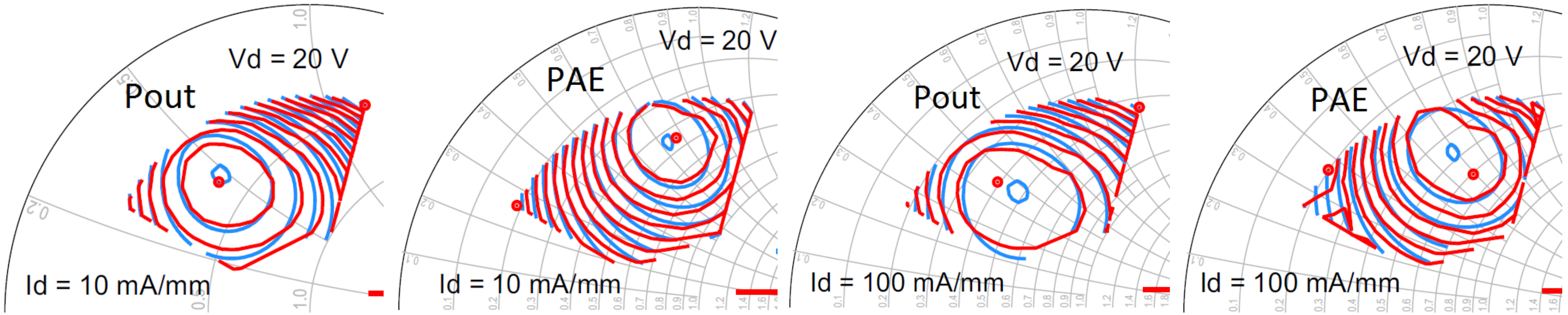
Source: Prof. Yogesh Chauhan

Large-Signal Model Validation



ADS Schematic for simulation of load-pull contours

22 dBm signal @ 10 GHz



Pout & PAE load pull contours for 10 mA/mm

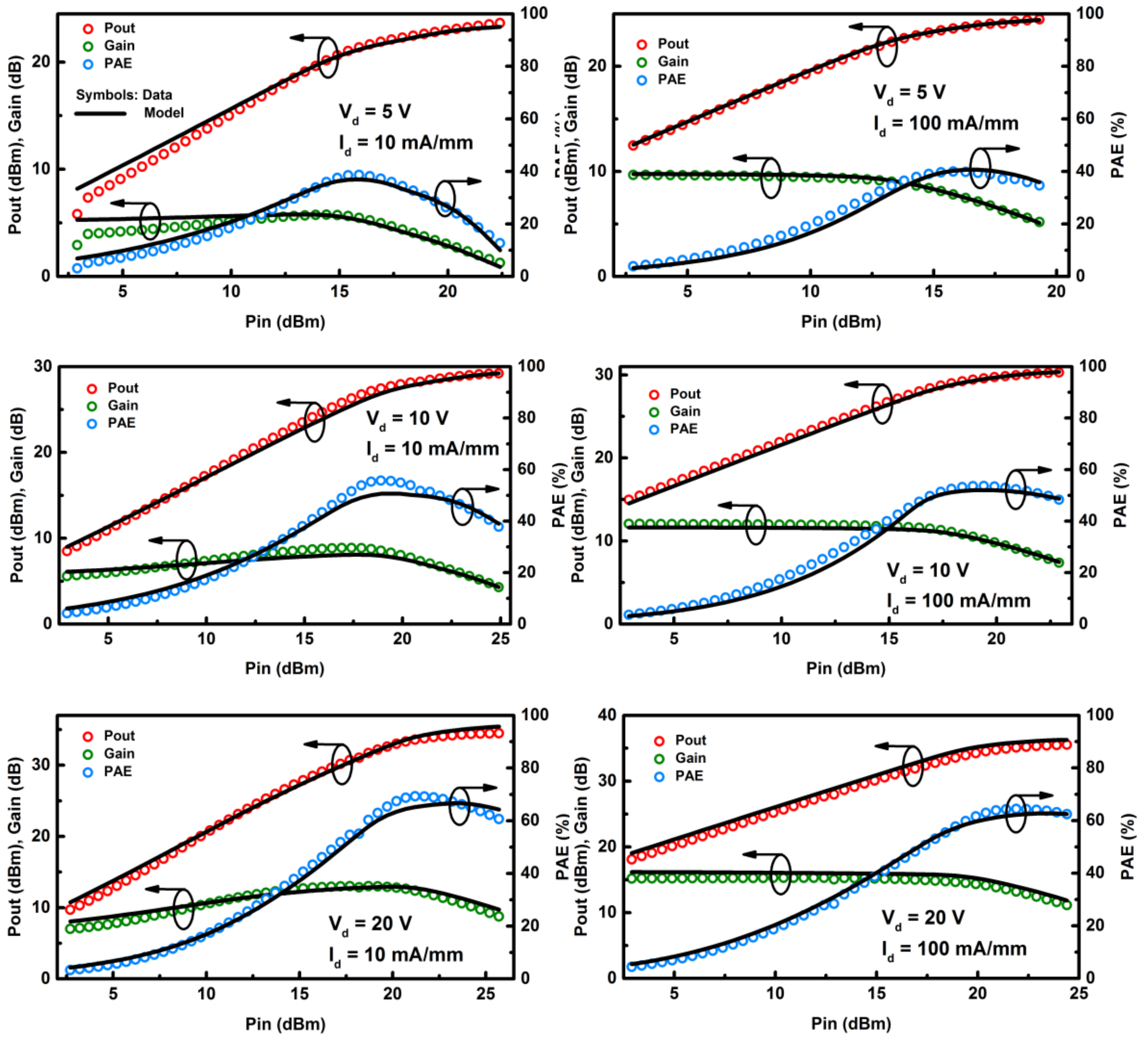
Pout & PAE load pull contours for 100 mA/mm

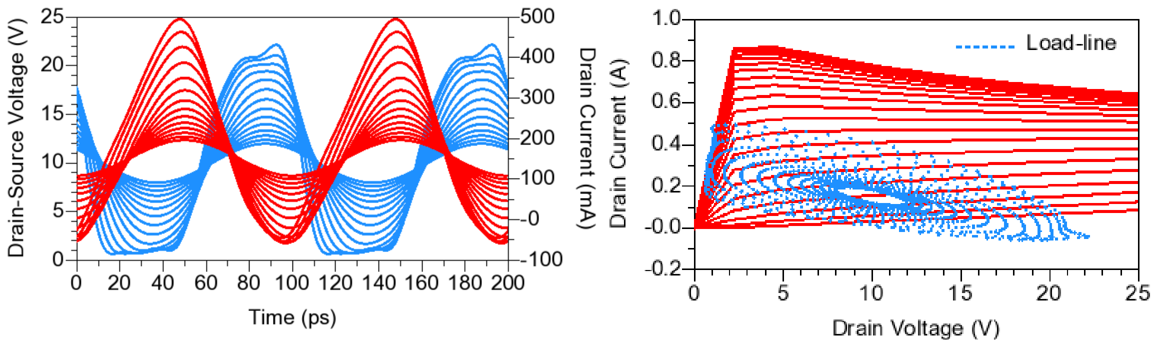
[1] S. A. Ahsan *et al.*, *IEEE J. Electron Devices Society*, Sep., [2017]

Source: Prof. Yogesh Chauhan

Validation – Drive-up (HB)

Harmonic balance drive-up characteristics showing Pout, PAE & Gain





Time domain waveforms of drain voltage & current.
Load line contours spanning the IV plane

	Frequency	10 mA/mm	100 mA/mm
Max. PAE	f_0	$22.46 + j38.54$	$30.53 + j34.35$
	f_1	$40.61 - j93.39$	$37.32 - j73.44$
	f_2	$11.39 - j0.07$	$14.77 + j10.83$
Max. P_{OUT}	f_0	$19.57 + j22.83$	$19.57 + j22.83$
	f_1	$253.48 - j65.72$	$253.48 - j65.72$
	f_2	$15.66 - j31.21$	$15.66 - j31.21$

[1] S. A. Ahsan *et al.*, *IEEE J. Electron Devices Society*, Sep., [2017]

Source: Prof. Yogesh Chauhan

Live Demo for Load-Pull Simulation

Summary

- RF GaN modeling is challenging but extremely important.
- IC-CAP provides an easy-to-use kit for CMC GaN modeling.
- The tuned parameters can be easily imported to ADS for design and verification.

Let's work together to enable first pass design success!

問卷填寫與抽獎

台灣繁體問卷:

- 請點選會議訊息欄中的連結，或掃描右方QR Code，以進行問卷填寫。
- 相關欄位請確實填寫，以確保抽獎資格。
- 我們將從有效問卷中抽出10位，寄送小禮物。請留有效地址。
- 若您還有其他技術問題，請寄信至亞太區客戶服務中心:
  eesof-asia_support@keysight.com

大陆简体问卷:

- **感謝您的參與!**