

Keysight PCIe Gen5 Application solution

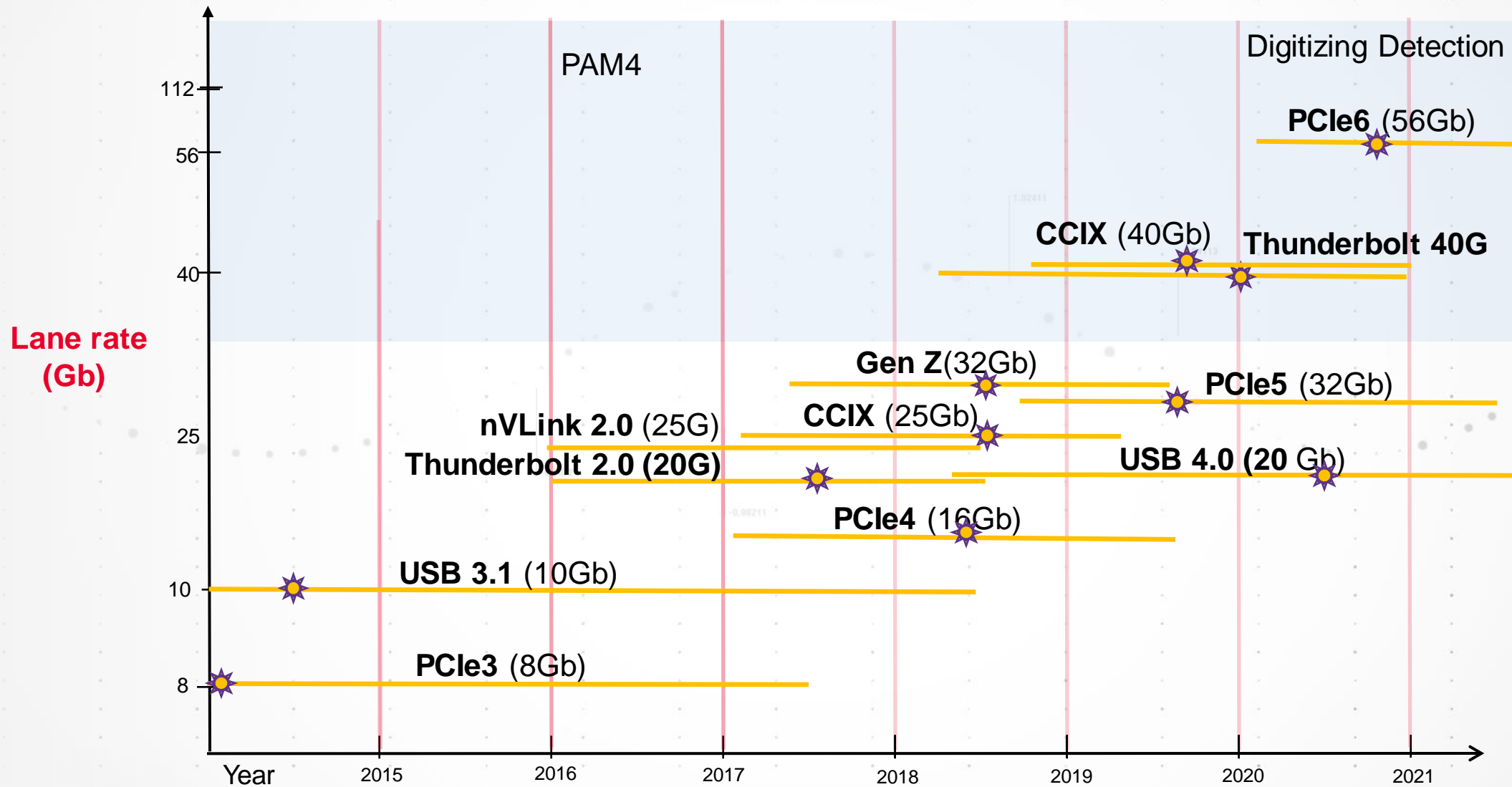
Jacky Yu

2020.MARCH

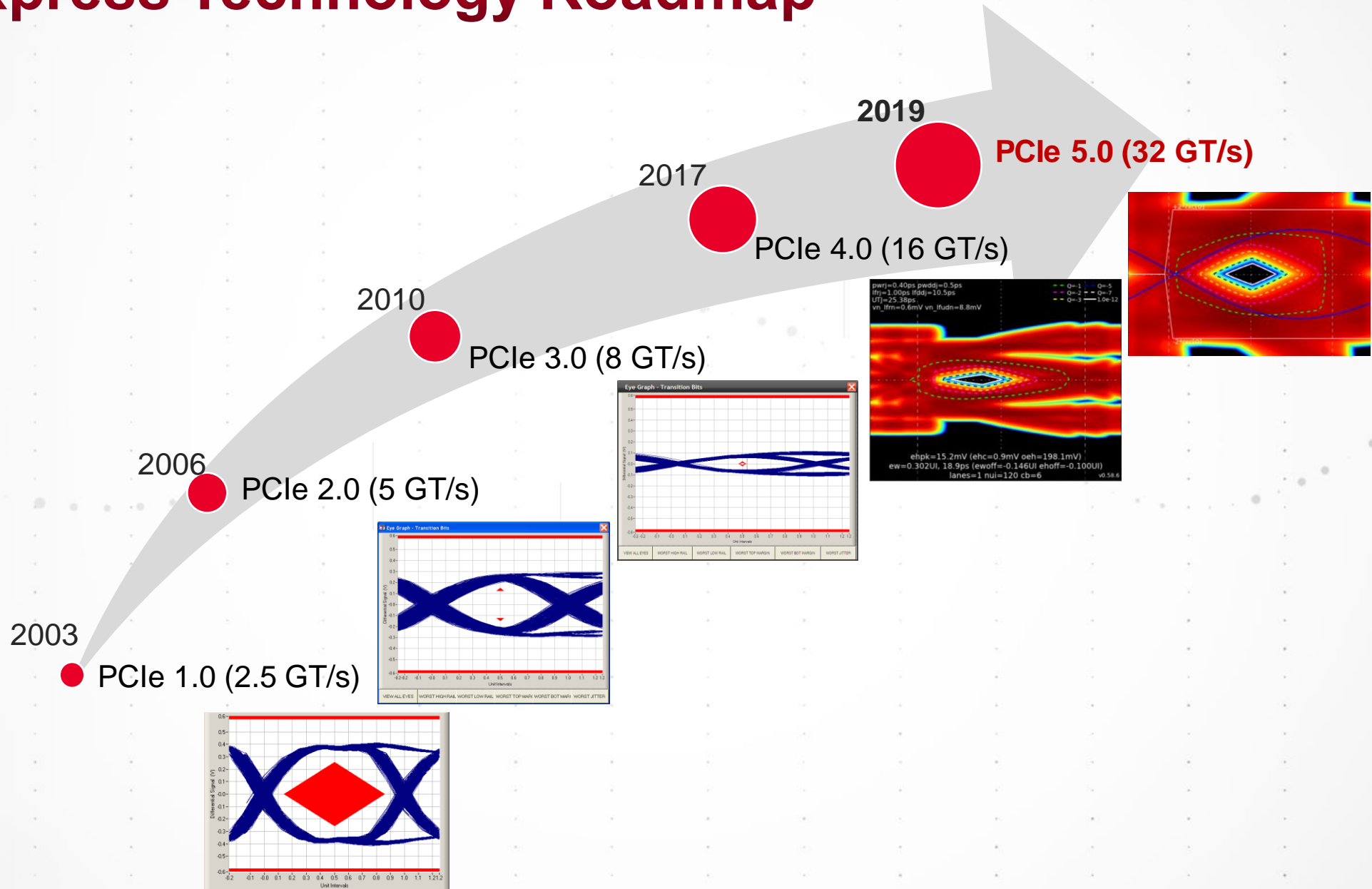
Keysight Taiwan Technologies



High-Speed Computing Roadmap



PCI Express Technology Roadmap



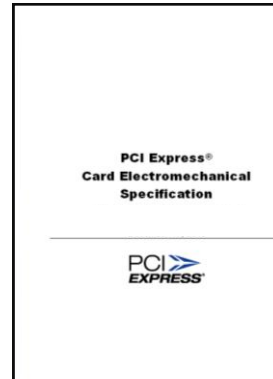
PCI Express Specifications and Scope

SELECT THE SPECIFICATIONS THAT RELATE TO YOUR SPECIFIC NEED

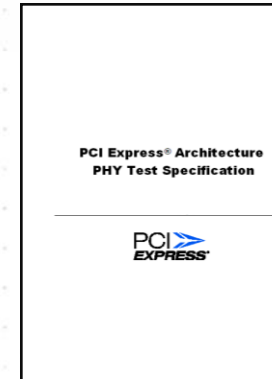


- Base Specification
- Contains all the system knowledge
 - Can directly be applied to Chip Test

1.0 final in May 2019



- Card Electromechanical (CEM) Spec
- Applies to Add-In Cards and Mother Boards
 - Mitigates card manufacturer's need to study the base specification
 - Increases reproducibility through PCI-SIG supplied test tools CBB and CLB (compliance base and load board)



- Phy Test Specification
- Defines compliance tests of CEM spec in detail

The screenshot shows a file management interface with a sidebar on the left and a main content area on the right. The sidebar is titled "Documents" and contains a search bar and a list of folders: "PCI Express - ElectroMechanical", "Administrative Documents", "Calendar Documents", "Meeting Documents", "PCIe 5.0 CEM", "PCIe 5.0 CEM Edge Finger SI", and "Standards". The main content area is titled "PCIe 5.0 CEM" and features an "Upload Document" button, a "Download Selected as ZIP" button, and a dashed box with the text "Drop to Upload or Click to Browse" and "Maximum File Size: 1024 MB". Below this is a table with columns for "Title", "Modified Date", and "Modified By". The table contains one entry: "CEM_5_0_Ver_0_5_draft_08_08_2019.pdf" with a "Download" link (575.27 KB) and a "Preview" link. The modified date is "Aug 9, 2019" and the modified by is "Manisha Nilange Intel Corporation".

Title	Modified Date	Modified By
CEM_5_0_Ver_0_5_draft_08_08_2019.pdf	Aug 9, 2019	Manisha Nilange Intel Corporation

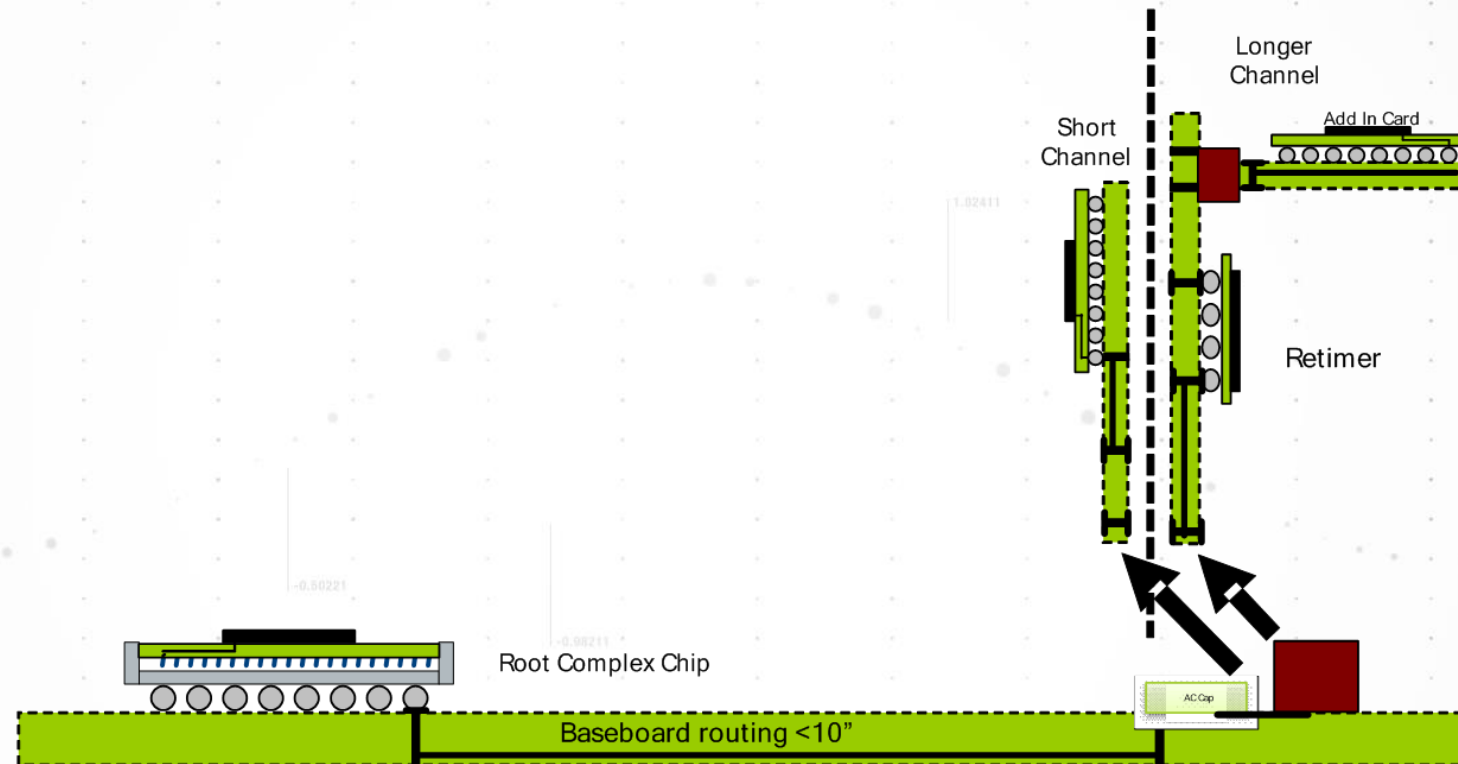
PCIe Gen5

GOALS

- BER target is $10e-12$
- TX Presets P0-P10 to remain the same
- Backward compatibility with previous PCIe Gen1/2/3/4
- Same approach for TX and RX testing used for Gen4
 - Similar method for TX testing via de-embedding of breakout board traces
 - Similar method for calibrating the eye width and eye height as used with PCIe 4.0 (ISI based, fixed RJ)
- Same TX Voltage and Jitter parameters as Gen4

PCI Express 5.0 Channel Topology

RETIMER REQUIRED WHEN LOSS EXCEEDS -36DB OR >1 CONNECTOR



- Estimated allowable loss: $\approx -36\text{dB}$ @ 16GHz
- Root complex pkg loss allowance $\approx -9\text{dB}$ @ 16GHz
- Add-in Card pkg loss allowance $\approx -4\text{dB}$ @ 16 GHz
- Total AIC loss budget estimate = $\approx 9\text{dB}$ @ 16GHz
- PCIe 5.0 CEM Connector loss budget $\approx 1.5\text{dB}$ @ 16 GHz

PCIe 5.0 Reference Clock and PLL Bandwidth Requirements

HIGHER SPEEDS = TIGHTER PHASE JITTER LIMITS

Data Rate	CC Jitter Limit
2.5GT/s	86ps (pk-pk)
5GT/s	3.1ps (RMS)
8GT/s	1.0ps (RMS)
16GT/s	0.5ps (RMS)
32GT/s	0.15ps (RMS)

- PCIe 5.0 specifies a short channel and a 50 ohm termination (100 ohm differential termination) for reference clock phase jitter measurements only.
- Lower PLL bandwidth limit for 8.0 and 16.0 GT/s reduced to 0.5 MHz
 - Revised model CDR at 16GT/s for backward compatibility
 - Reduced TX UTJ limit at 8GT/s for backward compatibility

PLL #1, PLL #2	0.01 dB peaking	2.0 dB peaking	32.0 GT/s CC	CDR
BW _{PLL} (min) = 0.5 MHz	$\omega_{n1} = .112$ Mrad/s $\zeta_1 = 14$	$\omega_{n1} = 1.51$ Mrad/s $\zeta_1 = 0.73$		
BW _{PLL} (max) = 1.8 MHz	$\omega_{n1} = .403$ Mrad/s $\zeta_1 = 14$	$\omega_{n1} = 5.42$ Mrad/s $\zeta_1 = 0.73$		

16 combinations

32.0 GT/s



PCI Express 5.0 TX Testing

KEYSIGHT TOOLS FOR TRANSMITTER VALIDATION

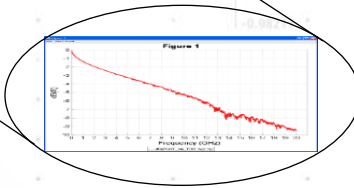
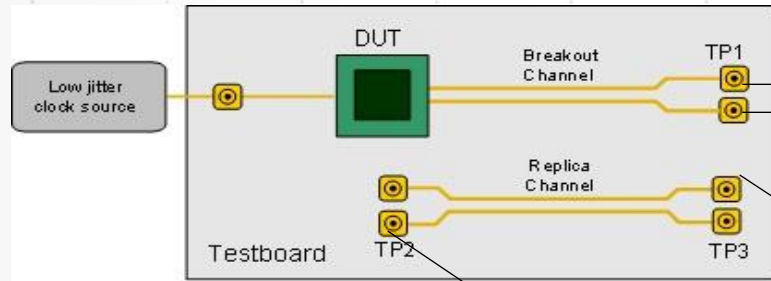
PCIe 5.0 32GT/s TX Testing

BREAK OUT CHANNEL FOR ASIC REQUIRED

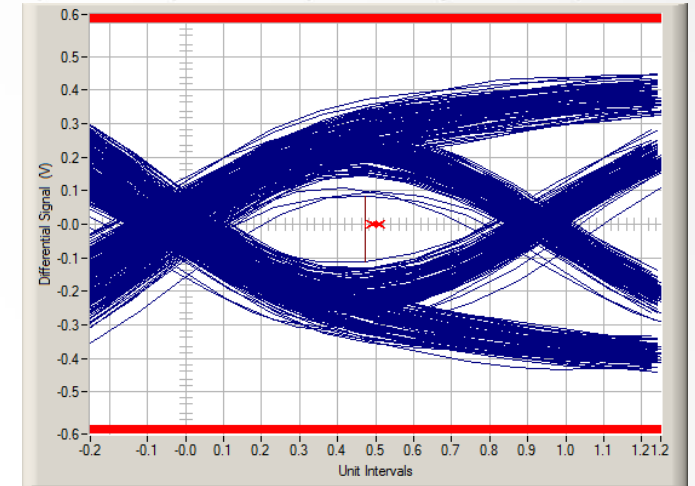
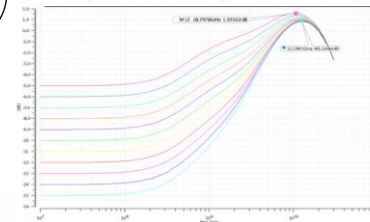
Keysight UXR-Series Real Time Oscilloscope



PCIe 5.0 ASIC/IC Custom Breakout Board



S-Parameters of Replica Ch. Used to de-embed to pin or Ref CTLE can be used (12dB).



Base Test Results - Test_File_Gen5_P4.bin

Base Test Result *Pass!*

VOLTAGE STATS		MISC STATS	
EIEOS Min Voltage (mV)	V Tx no. eq (mV)	# of samples	1500000
Pattern not in waveform	1092.76367	sample int (ps)	3.91
AC CM 4GHz (mV pp)	AC CM 30KHz-500MHz (mV pp)	waveform length (us)	58.59
Not single ended data	Not single ended data	# of UI	1875000
		Pattern repeat count	28

JITTER STATS		
Uncorrelated TIE TJ @ E-12 (ps)	Uncorrelated TIE Di dd (ps)	TIE RJ (RMS)
2.64581	0.08567	0.18209
Uncorrelated PWJ TJ @ E-12 (ps)	Uncorrelated PWJ Di dd (ps)	PWJ RJ (RMS)
2.90266	0.23565	0.18969
DDi (ps)	PS21 Ratio (dB)	FZ Jitter (ps)
1.56790	Pattern not in waveform	0.35840

[View HTML Report](#)

D9050PCIC New Features

MASTER YOUR BEST DESIGN

- Supports PCIe 5.0 BASE TX Testing at 32GT/s as well as 2.5G, 5G, 8G and 16GT/s (v0.9 BASE)
- Supports PCIe 5.0 Reference Clock tests (2.5G, 5G, 8G, 16G)
- Will Support CEM tests for endpoints and root complexes (2.5G, 5G, 8G, 16G, 32G).
- Integrated De-embedding of break-out channel with optional InfiniiSim
- Automated DUT control using an 81150/60A Pulse Generator ARB.
- Enhanced Switch Matrix supporting arbitrary lane mapping
- Minimum oscilloscope BW: 50GHz

Keysight D9050PCIC PCIe 5 (Gen5) TX Test Application

50GHZ SCOPE BANDWIDTH REQUIRED

The screenshot shows the 'PCI-Express Gen5 Test Application -- New Device1' window. The interface includes a menu bar (File, View, Tools, Help) and a toolbar (Set Up, Select Tests, Configure, Connect, Run, Automate, Results, HTML Report). The main area is divided into several sections:

- Capture and Analysis Mode:** Three radio buttons: 'Capture mode: Acquire and store waveforms only', 'Analyze mode: Analyze captured waveforms', and 'Capture and analyze stored waveforms' (selected).
- Test Point:** A list of radio buttons: 'Base - Transmitter Tests' (selected), 'CEM - Add In Card Tests', 'CEM - System Tests', 'Base - Reference Clock Tests', and 'Equalization Preset Tests' (checkbox).
- Set Up:** Two buttons: 'Device Definition' and 'Connection Setup'.
- Device Under Test (DUT):** A section for 'Device Name' with a 'New Device' button.
- Data Speed:** A list of checkboxes for data rates: 2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s (checked).
- Signal Quality Preset:** Three dropdown menus for 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s, all set to 'P4'. A '5.0 GT/s De-emphasis' button is also present.
- Misc:** Three checkboxes: 'Collective Preset Data Acquisition', 'DUT Automation', and 'Workshop Compliance Mode' (checked).
- Test Report:** A section for 'User comments'.
- Messages:** A log showing system messages, with the latest entry '2019-01-09 10:06:08:277 PM Ready' highlighted.

Callouts and annotations:

- 'Operate on "live" or saved data waveforms' points to the 'Capture and Analysis Mode' section.
- 'Choose Test Reference Point' points to the 'Test Point' section.
- 'Define Test Setup' points to the 'Set Up' buttons.
- 'Select Speeds of Gen5 Device to Test' points to the 'Data Speed' section.

Keysight D9050PCIC PCIe 5 (Gen5) TX Test Application

5.0 BASE SPEC TESTS

PCI-Express Gen5 Test Application -- New Device1

File View Tools Help

Set Up **Select Tests** Configure Connect Run Automate Results HTML Report

- All PCI Express Gen 5 Tests
 - 32.0 GT/s Tests
 - Transmitter (Tx) Tests
 - Signal Quality
 - Unit Interval
 - Full swing Tx voltage with no TxEQ
 - Uncorrelated total jitter
 - Uncorrelated deterministic jitter
 - Total uncorrelated PWJ
 - Deterministic DjDD uncorrelated PWJ
 - Pseudo package loss
 - Data dependent jitter
 - Random jitter
 - Min swing during EIEOS for full swing
 - Common Mode Voltage
 - Tx, DC common mode voltage
 - Tx, AC common mode voltage
 - Tx, Absolute delta of DC common mode voltage

(Click a test's name to see its description)

Messages

Summaries (click for details) Details

2019-01-09 10:06:00:460 PM Connected to Infiniium

2019-01-09 10:06:02:142 PM Refreshing HTML Report

2019-01-09 10:06:02:186 PM HTML Report Refreshed

2019-01-09 10:06:08:277 PM Ready

Application initialized and ready for use.

Test Report

Overall Result: **PASS**

Test Configuration Details	
Device Description	
Data Channel +	ChannelR-1
Data Channel -	ChannelR-3
Device Name	New Device1
Test Session Details	
Infiniium SW Version	06.30.00701
Infiniium Model Number	DSAZ634A
Infiniium Serial Number	MY57220110
Application SW Version	0.99.9029.0
Debug Mode Used	No
Compliance Limits	PCI-Express Gen5 Test Application (official)
Last Test Date	2019-01-12 22:03:19 UTC -06:00

Keysight D9050PCIC PCIe 5 (Gen5) TX Test Application

ORDERING INFORMATION

Oscilloscope Bandwidth Requirements

Data Rate	TX Bandwidth Required	Minimum Sample Rate	Minimum Bandwidth required for RX Calibration
2.5 GT/s	6 GHz	20 GSa/s	12 GHz
5 GT/s	12 GHz	40 GSa/s	12 GHz
8 GT/s	12 GHz	40 GSa/s	25 GHz
16 GT/s	25 GHz	80 GSa/s	25 GHz
32 GT/s	50 GHz	160 GSa/s	50 GHz

Recommended Test Accessories

40 GHz Electrical (2.92 mm) (K connector) [mates with 3.5 mm]	
Part Number	Description
N2812B	50-ohm cable, 2.92 mm (m-m) 1 meter
N2823A	50-ohm cable, 2.92 mm (m-m) matched pair 1 meter
N5448B	50-ohm cable, 2.92 mm (m-m) matched pair 25 cm

50 GHz Electrical (2.4 mm)	
Part Number	Description
N4910A	50-ohm cable, 2.4 mm (m-m), matched pair

Breakthrough Technology

ENABLES 1-TERABIT/S MEASUREMENTS

Introducing UXR-Series Ultra-High Performance Infiniium Oscilloscopes

110 GHz maximum bandwidth with **extremely high signal integrity**

- 13, 16, 20, 25, 33/40, 50, 70, 80, 100, and 110 GHz models (on all channels)
- 128/256 GSa/s on all channels
- 2G max memory per channel
- 10-bit ADC and superior ENOB with extremely low noise
- Vertical sensitivity from 10 mV to 500 mV per division
- 2 or 4 channels
- Full self-calibration



The Industry's Best Signal Integrity

- **Lowest noise**
< 1.0 mV rms*
- **Lowest intrinsic jitter**
< 25 fs rms*
- **Lowest inter-channel jitter**
< 35 fs rms*
- **Highest ENOB**
> 4.5 bits @ 110 GHz*
> 5 bits @ 100 GHz*
- **Flattest frequency response**
(magnitude and phase)

*Typical performance measured on prototype units

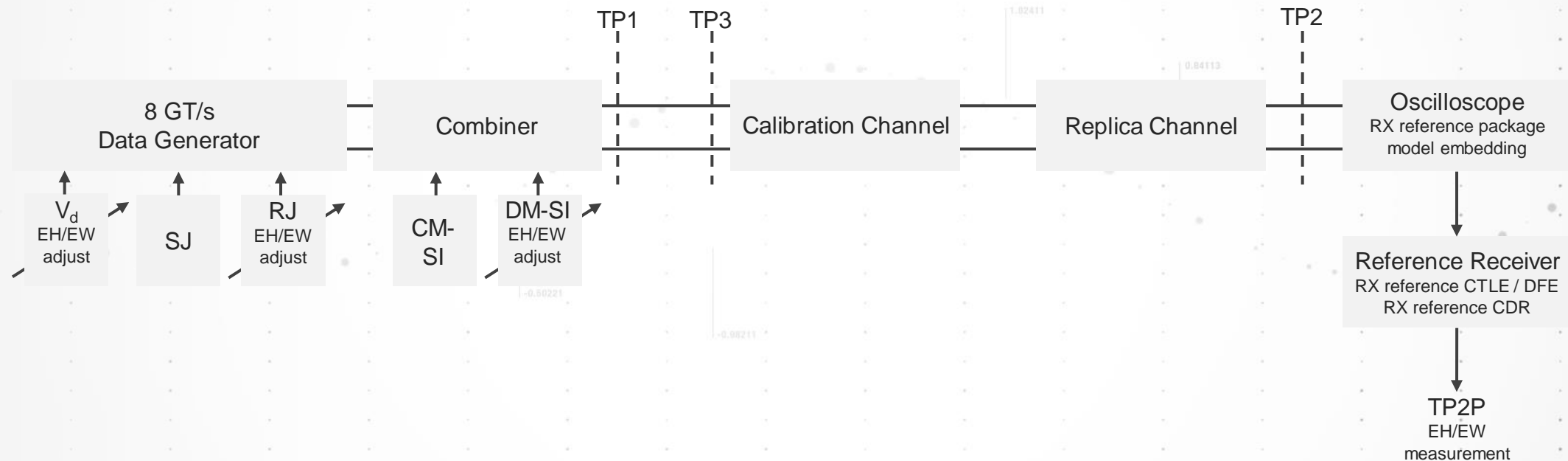




PCIe Gen5 Rx testing

PCI Express 5.0 – Base Specification

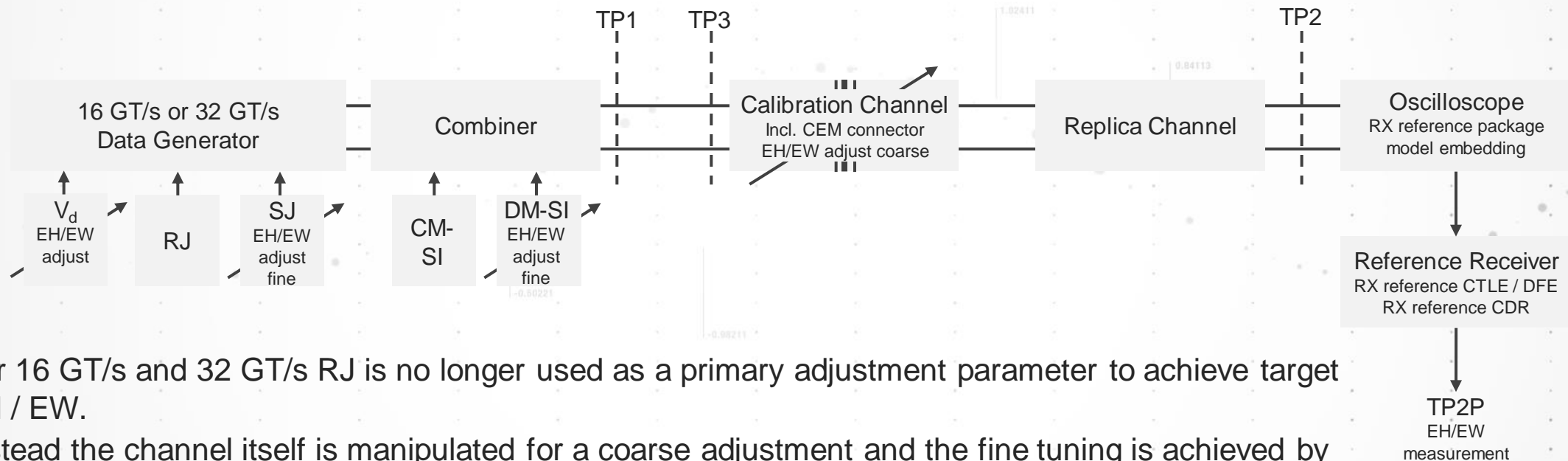
RX STRESS SIGNAL CALIBRATION SETUP FOR 8 GT/s



- In case SIGTEST is used the RX reference package model embedding is not done on the oscilloscope but by SIGTEST. This applies to 8 GT/s only

PCI Express 5.0 – Base Specification

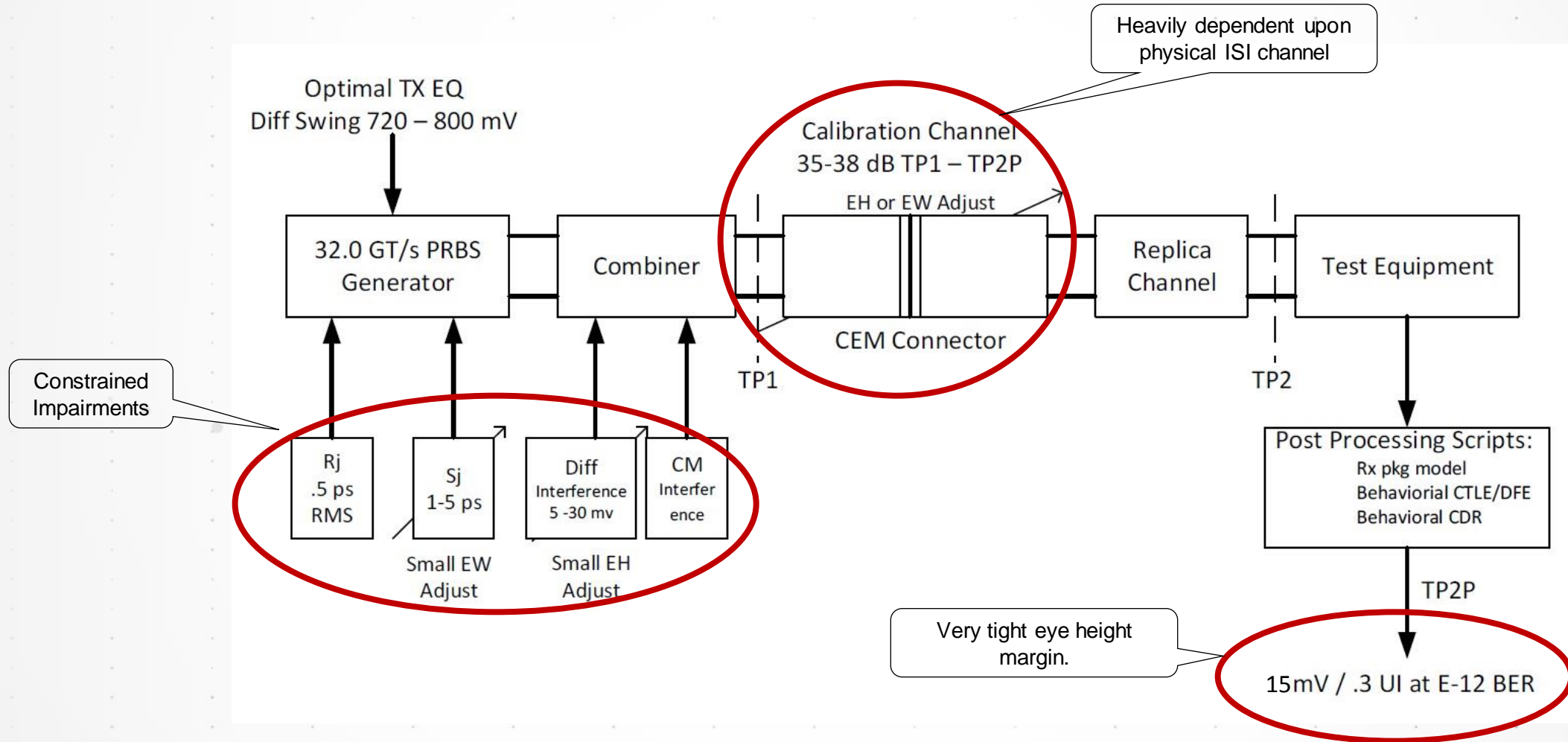
RX STRESS SIGNAL CALIBRATION SETUP FOR 16 GT/s & 32 GT/s



- For 16 GT/s and 32 GT/s RJ is no longer used as a primary adjustment parameter to achieve target EH / EW.
- Instead the channel itself is manipulated for a coarse adjustment and the fine tuning is achieved by manipulating SJ and DM-SI
- The intention was to achieve a more realistic stress signal
- RX reference package model embedding is no longer done in SIGTEST for 16 GT/s and 32 GT/s but on the scope itself

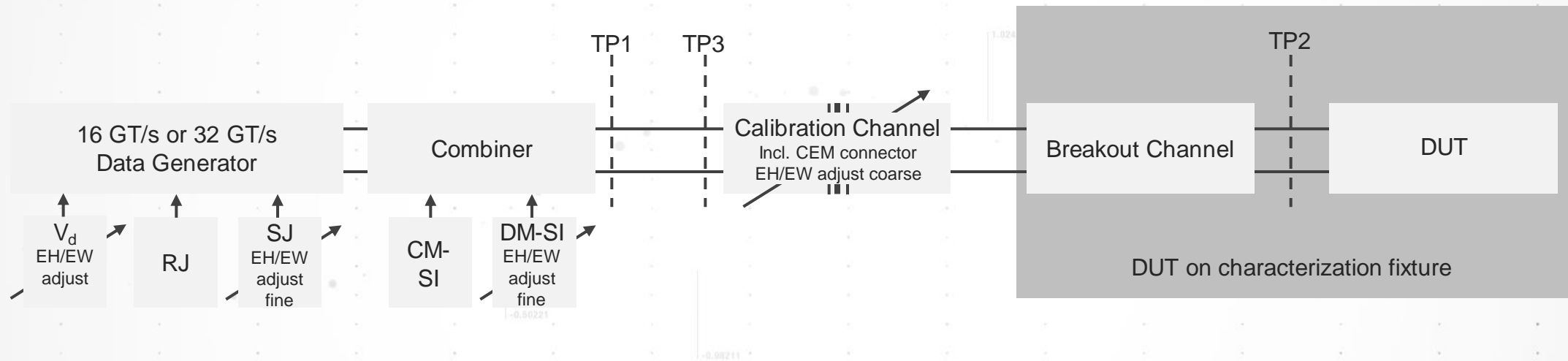
PCIe 5.0 32GT/s RX Calibration (BASE)

15MV EYE HEIGHT POST EQ (0.3UI EYE WIDTH) TARGET



PCI Express 5.0 – Base Specification

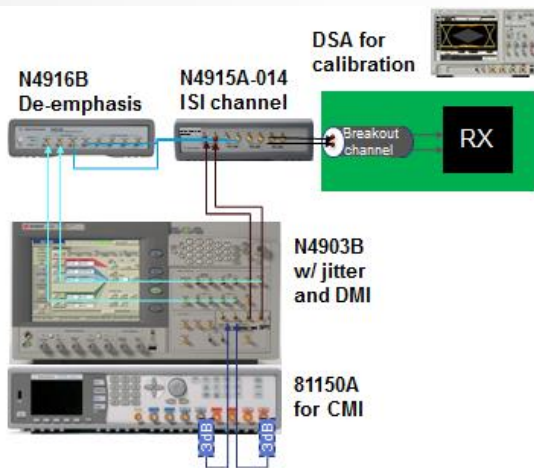
RX TEST SETUP FOR 16 GT/s & 32 GT/s



Keysight's PCI Express Receiver Test Solutions

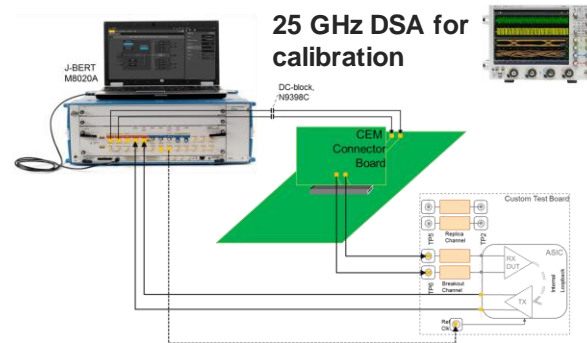
2012

PCIe 3.0 8G Base Specification
Calibration and Test Setup for ASICs



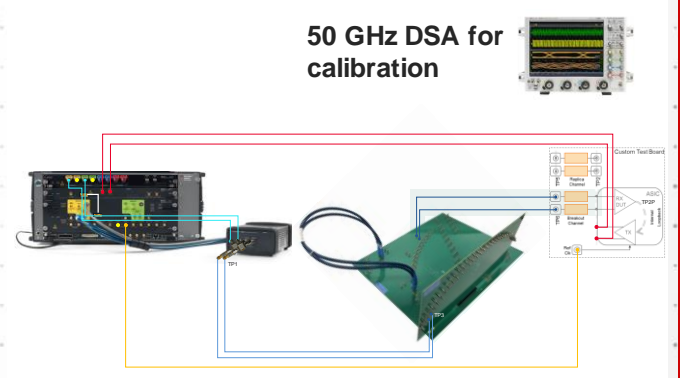
2016

PCIe 4.0 8G / 16G Base Specification
Calibration and Test Setup for ASICs



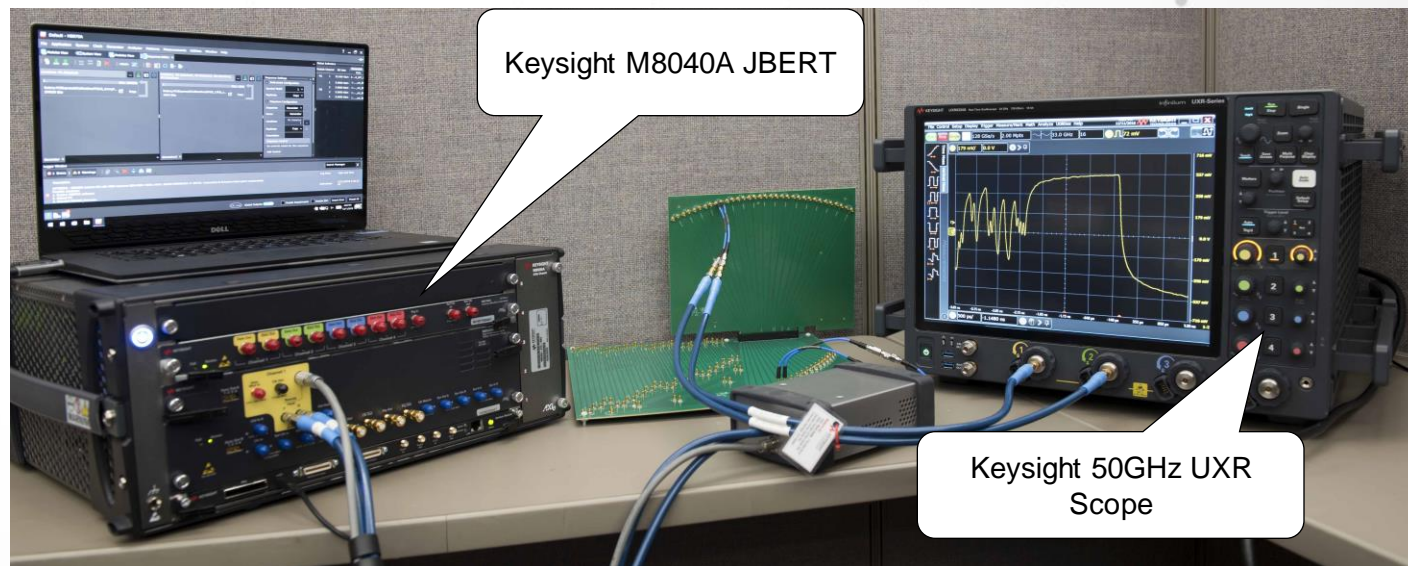
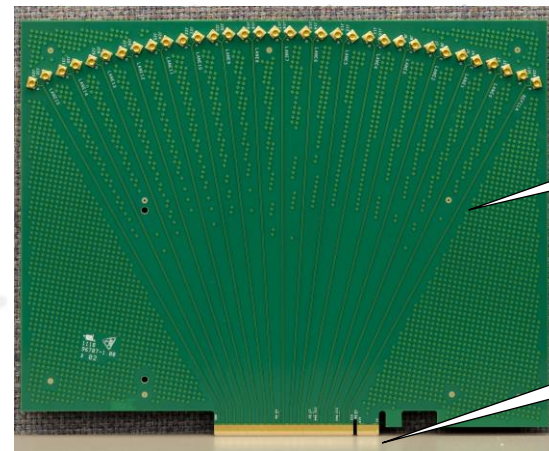
2019

PCIe 5.0 8G/16G/32G Base Specification
Calibration and Test Setup for ASICs



PCIe 5.0 32GT/s RX Calibration (BASE) Example

TARGET TEST CHANNEL BOARD W/ NEW CEM SMT CONNECTOR



TxEQ Coefficient Matrix Scan



- Show all results
- Show only selected

Print

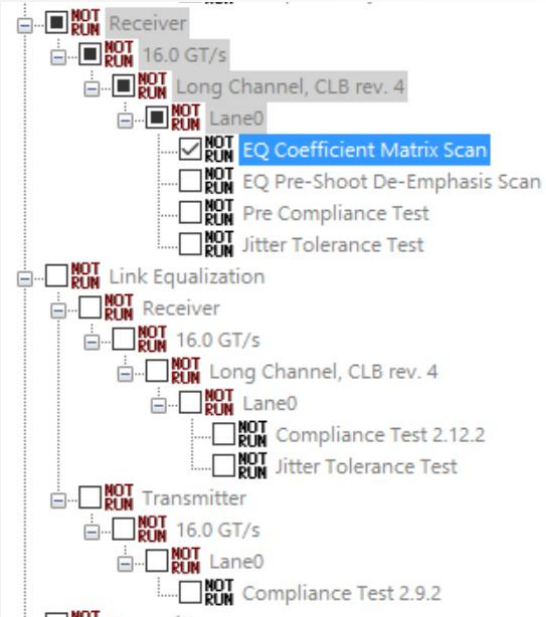
Summary

Product Number: PCIe PCIe Station Unknown User 12/02/2019 12:10:53

L0_Rx_16GTps_EQtable

for PCIe 4.0 System

Offline	False
CLB var. ISI pair	0
Total Channel Loss	-29.931 dB
Random Jitter	1 ps
Sinusoidal Jitter	7.1 ps
Sinusoidal Jitter Frequency	100 MHz
Common Mode Sinusoidal Interference	150 mV
Differential Mode Sinusoidal Interference	18.7 mV
Generator Launch Voltage	795 mV
Target BER	30E-12
Confidence Level	95 %
Force Retraining at each BER measurement	False



C-1 C+1	0/24	1/24	2/24	3/24	4/24	5/24	6/24	
0/24	BER: 0 Errors PS: 0.0dB DE: 0.0dB Boost: 0.0dB	BER: 0 Errors PS: 0.0dB DE: -0.8dB Boost: 0.8dB	BER: 0 Errors PS: 0.0dB DE: -1.6dB Boost: 1.6dB	BER: 0 Errors PS: 0.0dB DE: -2.5dB Boost: 2.5dB	BER: 0 Errors PS: 0.0dB DE: -3.5dB Boost: 3.5dB	BER: 0 Errors PS: 0.0dB DE: -4.7dB Boost: 4.7dB	BER: 0 Errors PS: 0.0dB DE: -6.0dB Boost: 6.0dB	
1/24	BER: 0 Errors PS: 0.8dB DE: 0.0dB Boost: 0.8dB	BER: 0 Errors PS: 0.8dB DE: -0.8dB Boost: 1.6dB	BER: 0 Errors PS: 0.9dB DE: -1.7dB Boost: 2.5dB	BER: 0 Errors PS: 1.0dB DE: -2.8dB Boost: 3.5dB	BER: 0 Errors PS: 1.2dB DE: -3.9dB Boost: 4.7dB	BER: 0 Errors PS: 1.3dB DE: -5.3dB Boost: 6.0dB		
2/24	BER: 0 Errors PS: 1.6dB DE: 0.0dB Boost: 1.6dB	BER: 0 Errors PS: 1.7dB DE: -0.9dB Boost: 2.5dB	BER: 0 Errors PS: 1.9dB DE: -1.9dB Boost: 3.5dB	BER: 0 Errors PS: 2.2dB DE: -3.1dB Boost: 4.7dB	BER: 0 Errors PS: 2.5dB DE: -4.4dB Boost: 6.0dB			
3/24	BER: 0 Errors PS: 2.5dB DE: 0.0dB Boost: 2.5dB	BER: 0 Errors PS: 2.8dB DE: -1.0dB Boost: 3.5dB	BER: 0 Errors PS: 3.1dB DE: -2.2dB Boost: 4.7dB	BER: 0 Errors PS: 3.5dB DE: -3.5dB Boost: 6.0dB				
4/24	BER: 0 Errors PS: 3.5dB DE: 0.0dB Boost: 3.5dB	BER: 0 Errors PS: 3.9dB DE: -1.2dB Boost: 4.7dB	BER: 0 Errors PS: 4.4dB DE: -2.5dB Boost: 6.0dB					
5/24	BER: no sync PS: 4.7dB DE: 0.0dB Boost: 4.7dB	BER: no sync PS: 5.3dB DE: -1.3dB Boost: 6.0dB						
6/24	BER: no sync PS: 6.0dB DE: 0.0dB Boost: 6.0dB							

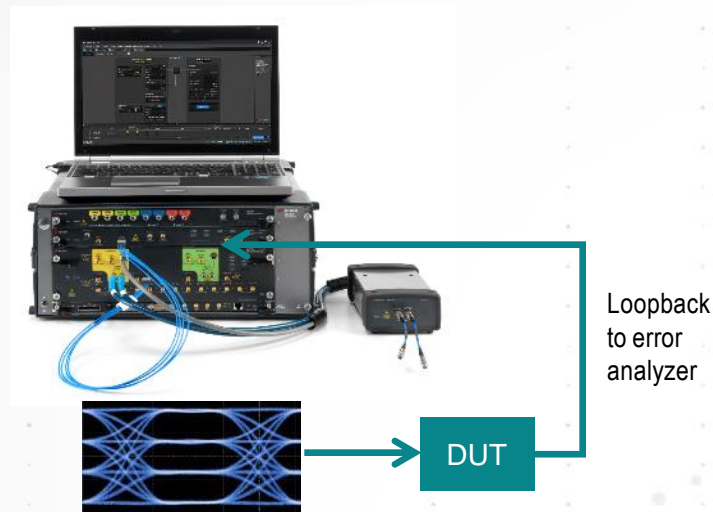
M8040A 64 GBaud High-performance BERT



Master your next generation PCIe design

- Highly integrated for simplified RX test setup for 400G and PCIe5
- Upgrade paths towards 64 Gbaud PAM4/ NRZ
- Most complete solution with test automation
- PCI-SIG gold-suite approved vendor

M8040A 64 Gbaud High-performance BERT



PAM4 and NRZ
1 and 2 channel pattern generator
with remote heads, de-emphasis, jitter
injection and FEC

Where used:

- 400GbE, 200GbE, CEI-56G
- New: PCI Express 5.0, TBT 3
- Input (RX) characterization and compliance test
- For PAM4 and NRZ signals up to 64 Gbaud

Key Capabilities:

- Highly integrated BERT, AXIe based
- Accurate physical layer characterization and compliance test of next generation digital high-speed I/Os with NRZ and PAM4 data formats
- Control via M8070B system software for M8000

Pattern Generator (M8045A)

- Single or dual 32/64 Gbaud NRZ/PAM4
- Built-in de-emphasis (5 taps)
- Clean and jittered data patterns and clocks
- Remote head M8057B: 1.8 Vpp diff. and close connection to DUT
- NRZ and PAM4 is switchable by software
- FEC encoding on 1 lane
- ISI channels and interference source

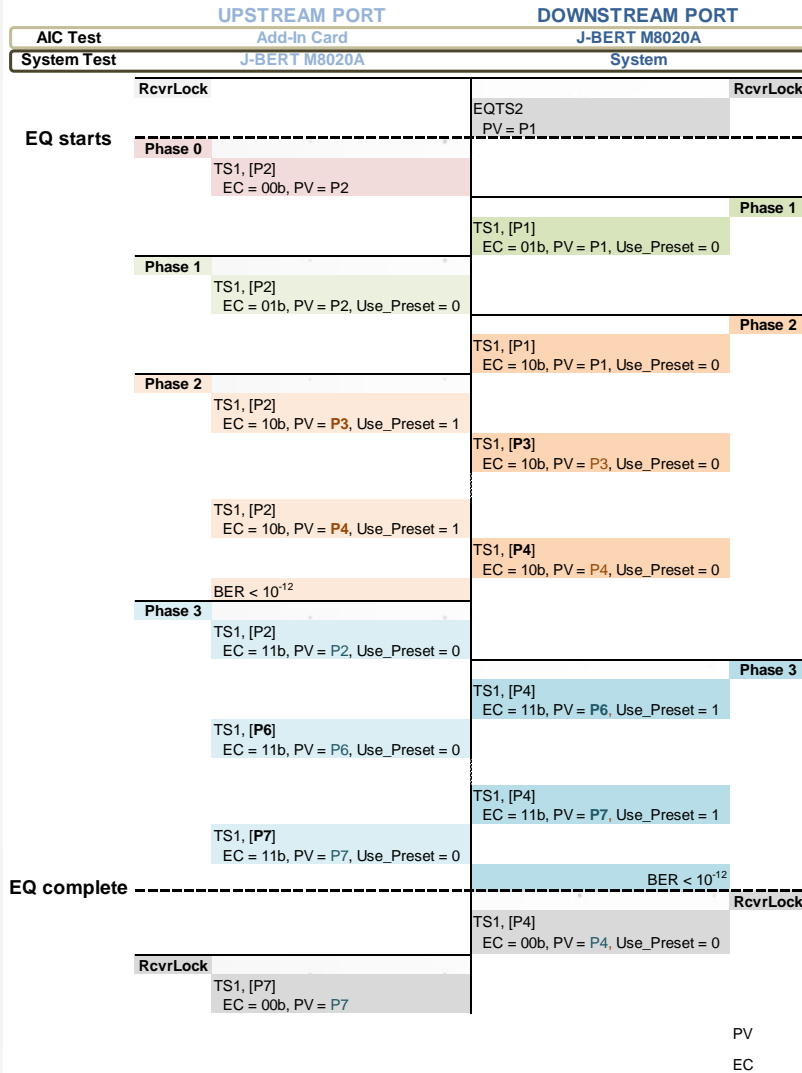
Error Analyzer (M8046A)

- 32/58Gbaud error detector for PAM4* and NRZ
- Built-in equalization
- Built-in clock recovery
- Supports up to 64Gb/s NRZ, 30GBd PAM4
- Burst error distribution and FLR extrapolation
- Filtering of SKP OS symbols
- Interactive link training 8&16/32 GT/s PCIe

* PAM4 58G

Dynamic Link Equalization Handshake 32 GT/s

THE FOUR PHASES OF THE LINK EQUALIZATION PROTOCOL



Phase 0:

- 2.5 Gb/s
- Downstream port tells upstream port which initial preset to use after the speed change will have been done.

Phase 1:

- 8 Gb/s
- Link partners settle on 8 GT/s speed.
- Exchange FS/LF values.

Phase 2:

- 8 Gb/s
- Add-in Card sets up the de-emphasis of the System Board's transmitter.

Phase 3:

- 8 Gb/s
- System Board sets up the de-emphasis of the Add-in Card's transmitter.

IF SUCCESSFUL

Phase 0:

- 8 Gb/s
- Downstream port tells upstream port which initial preset to use after the speed change will have been done.

Phase 1:

- 16 Gb/s
- Link partners settle on 16 GT/s speed.
- Exchange FS/LF values.

Phase 2:

- 16 Gb/s
- Add-in Card sets up the de-emphasis of the System Board's transmitter.

Phase 3:

- 16 Gb/s
- System Board sets up the de-emphasis of the Add-in Card's transmitter.

IF SUCCESSFUL

Phase 0:

- 16 Gb/s
- Downstream port tells upstream port which initial preset to use after the speed change will have been done.

Phase 1:

- 32 Gb/s
- Link partners settle on 16 GT/s speed.
- Exchange FS/LF values.

Phase 2:

- 32 Gb/s
- Add-in Card sets up the de-emphasis of the System Board's transmitter.

Phase 3:

- 32 Gb/s
- System Board sets up the de-emphasis of the Add-in Card's transmitter.

New: PCI Express Interactive Link Training 8/16/32 GT/s

M8046A-0S1 INTERACTIVE LINK TRAINING FOR PCIE 32G/16G/8G

The screenshot displays the Keysight M8070B software interface for configuring PCI Express Interactive Link Training. The main window is titled "Default - M8070B" and features a menu bar (File, Application, System, Clock, Generator, Analyzer, Patterns) and a toolbar. The interface is divided into several panels:

- Locations:** A list of test locations for M1.DataOut1, including "1. Link_Down", "2. Link_Idle", "3. Link_Up", and "4. RX_Test_Pattern".
- Sequence Settings:** A central configuration panel for "M1.DataOut1" with the following settings:
 - PHY Protocol: PCIe5
 - Replicate: Copy
 - Description: **Link Training PCIe :** (highlighted with a red circle)
 - DUT: Add In Card
 - Clock Architecture: Common
 - Loopback through: L0-Recovery
 - Trigger State: Recovery Equali
 - Lane: 0
 - Link: 0
 - Compliance Receiv...: Deasserted
 - Link Equalization: Bypass
 - Start Preset: P4
 - DUT Preset Hint: Reserved
 - DUT Initial Preset: P0
 - DUT Target Preset: P0
 - Select Start Preset...: User Defined
 - Start Preset Gen 4: P4
- Parameters:** Two panels on the right showing detailed settings for "M2.DataIn":
 - Clock:** Source: CDR, Follow SYS CLK: On, Symbol Rate: 32.000 GBd.
 - Equalization:** Equalizer Level: 0.
 - Line Coding:** Coding: NRZ.
 - Comparator:** Compare mode: Differential, Threshold: 0 mV, Polarity: Non-Inverted, Input Range: 500 mV.
 - CDR:** Control: Sequence, Transition Density: 50 %, Loop Order: 2nd, Loop Bandwidth: 20.000 MHz, Loop Selection: Loop3, Peaking: 1.8 dB.
- Amplifier:** Output State: On, Coupling: AC, Polarity: Non-Inverted, Amplitude: 500 mV, Offset: 0 mV, High: 250 mV, Low: -250 mV, Clk/2 Jitter State: Off, Clk/2 Jitter: 0.0 ps.
- Deemphasis:** PCIe LTSSM Presets: Full Swing (selected), Pre-Cursor: 0, Post-Cursor: 0.
- Output Timing:** LF Jitter, HF Jitter, Error Insertion, FEC Error Insertion.

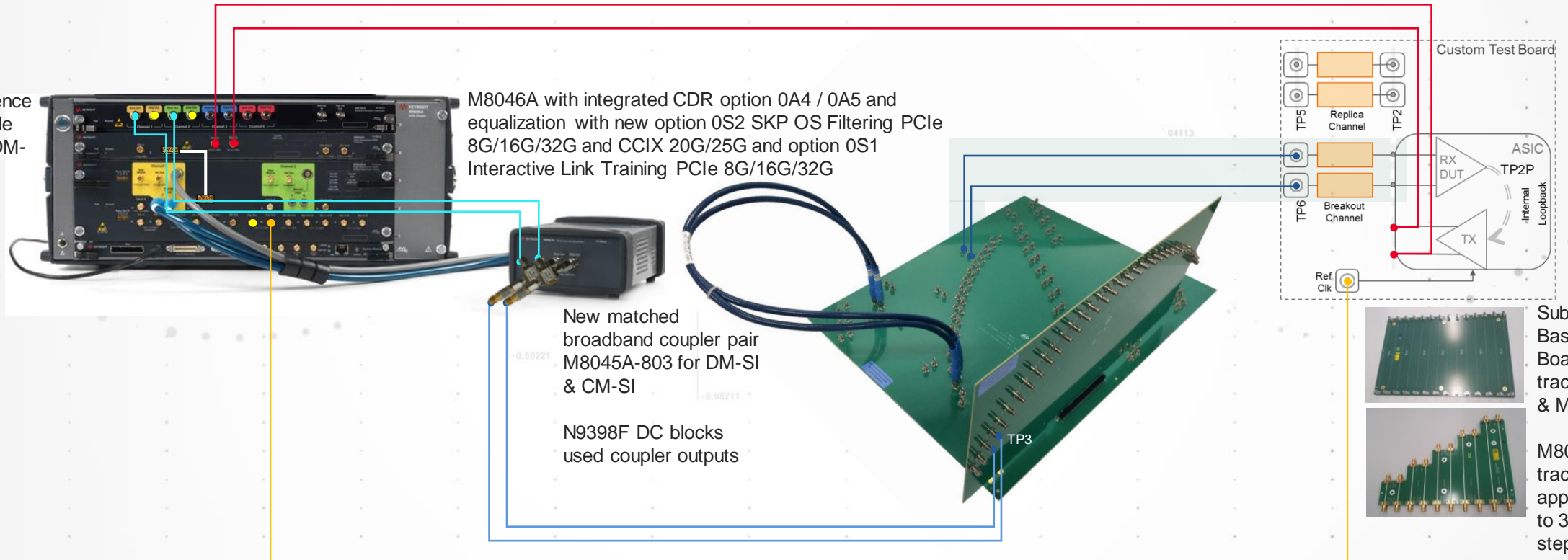
- Status Indicators:** A table at the bottom showing the status of the generator and analyzer modules.

Module	Channel	Bit Rate	Data	Output	Jitter	SSC
M1	1	32.000 Gb/s	1:...training			
	2	32.000 Gb/s	1:static 0			
M2	1	32.000 Gb/s				

PCIe 32G/16G/8G RX Test Setup

SETUP USING M8040A 64G HIGH-PERFORMANCE BERT

New Interference Source module M8054A for DM-SI & CM-SI



M8046A with integrated CDR option 0A4 / 0A5 and equalization with new option 0S2 SKP OS Filtering PCIe 8G/16G/32G and CCIX 20G/25G and option 0S1 Interactive Link Training PCIe 8G/16G/32G

New matched broadband coupler pair M8045A-803 for DM-SI & CM-SI

N9398F DC blocks used coupler outputs

Substitute PCIe 5 Base Channel Boards by new ISI traces M8049A-003 & M8049A-001

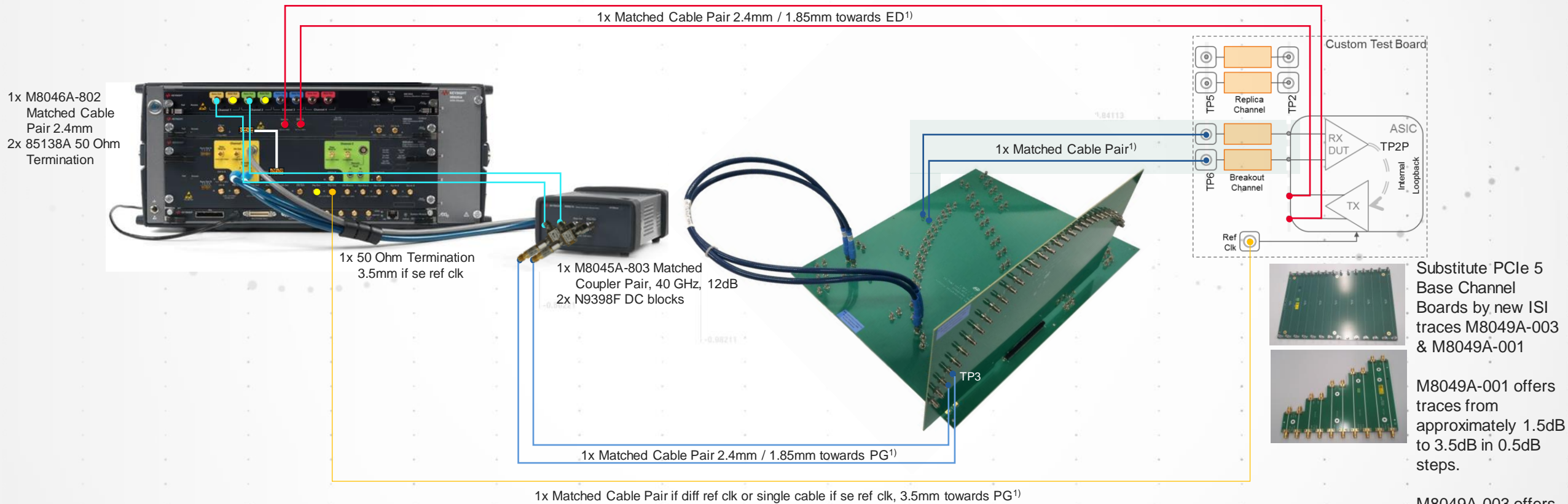
M8049A-001 offers traces from approximately 1.5dB to 3.5dB in 0.5dB steps.

M8049A-003 offers traces from 10dB to 22dB in 2dB steps.

IL @ 16GHz

PCIe 32G/16G/8G RX Test Setup

SETUP USING M8040A 64G HIGH-PERFORMANCE BERT



Substitute PCIe 5 Base Channel Boards by new ISI traces M8049A-003 & M8049A-001

M8049A-001 offers traces from approximately 1.5dB to 3.5dB in 0.5dB steps.

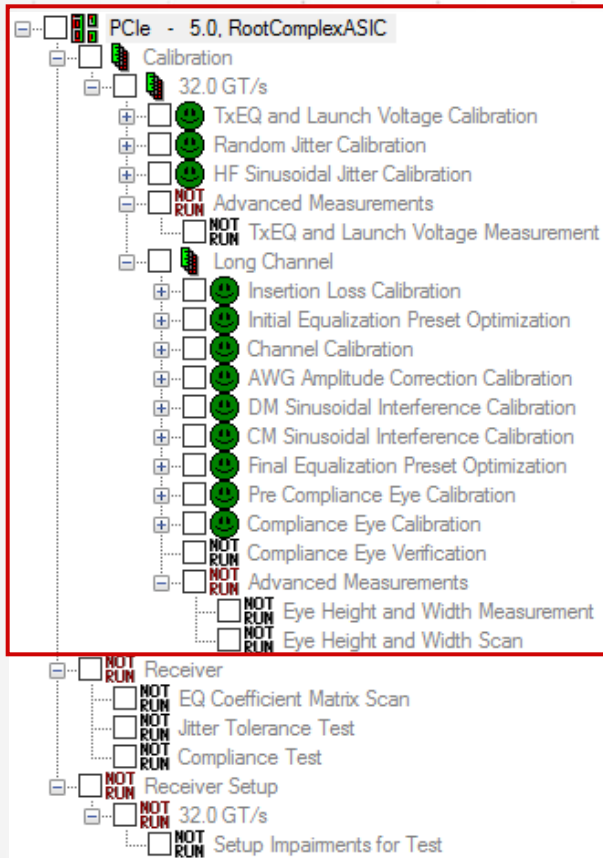
M8049A-003 offers traces from 10dB to 22dB in 2dB steps.

IL @ 16GHz

¹⁾ Type of cable depends on connectors of ISI fixtures and test boards

PCI Express 5.0 – Base Specification

CALIBRATION STEPS 32 GT/s RX STRESS SIGNAL



TP3 Calibration Steps

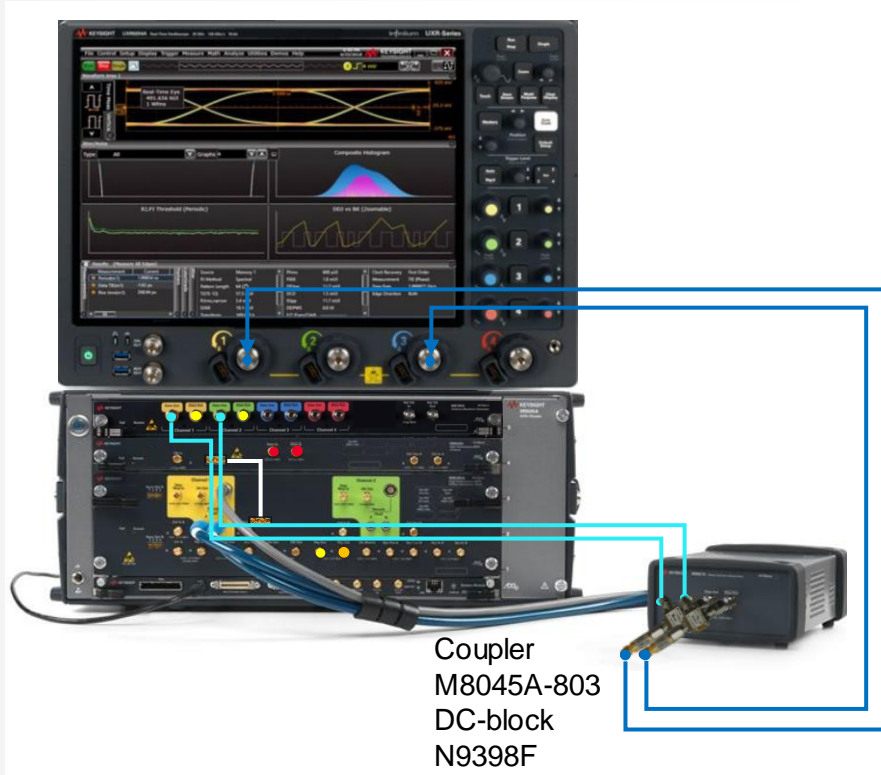
- Launch voltage, preshoot and de-emphasis
- RJ
 - using EZJIT
- SJ
 - using EZJIT

TP2P Calibration Steps

- Insertion loss calibration
 - VNA
- Initial optimal preset selection
 - using SEASIM
- Test channel loss selection
 - using SEASIM
- DM-SI calibration for selected channel
- CM-SI calibration for selected channel
- Final optimal preset selection
 - using SEASIM
- Compliance eye calibration
 - using SEASIM

PCI Express 5.0 32 GT/s – M8040A

BASE SPECIFICATION – TP3 CALIBRATION SETUP



TP3 Calibration Steps

- Launch voltage, preshoot and de-emphasis
- RJ
 - using EZJIT
- SJ
 - using EZJIT

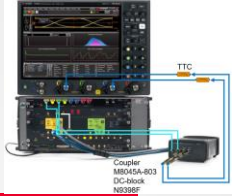
Connection

- BERT Data Output → Power Couplers → DC Blocks → high quality matched pair 2.4 mm cables → scope
- Comment: The actual cabling after the DC blocks and the scope is dependent on the connectors used for the ISI traces

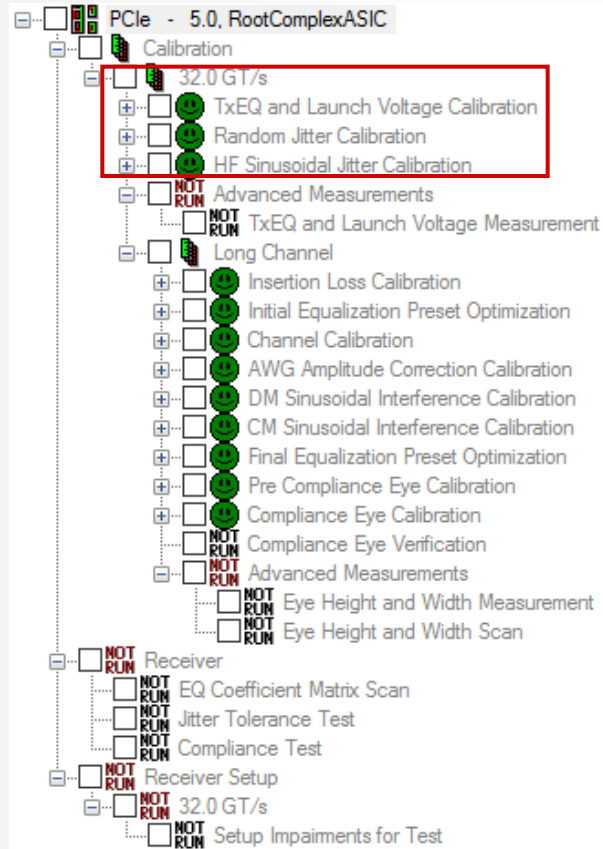
Scope BW

- At least 50 GHz of scope BW are required

PCI Express 5.0 – Base Specification



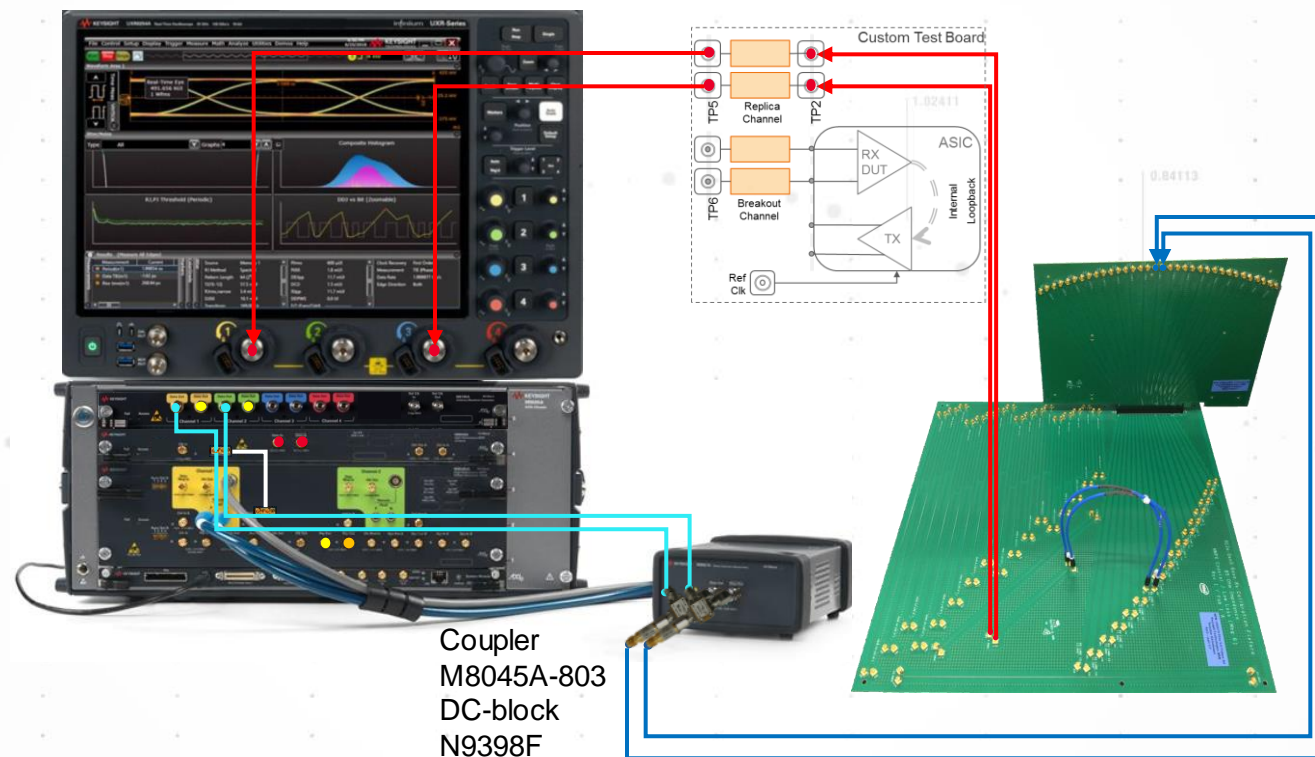
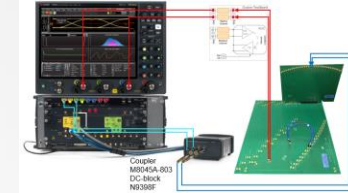
CALIBRATION 32 GT/s RX STRESS SIGNAL – TP3 CALIBRATION SETTINGS



Parameter	Min	Max	Unit	Oscilloscope Settings	
				Q-Series / Z-Series	UXR
Launch Amplitude 800 mV	796	804	mV _{pp}	BW: 50 GHz M8040A Sampling rate: 160 GSa/s Memory depth: 4.096 kpts Averaging: 128	BW: 50 GHz M8040A Sampling rate: 256 GSa/s Memory depth: 6.554 kpts Averaging: 256
Launch Amplitude 720 mV	716	724	mV _{pp}		
Preshoot and de-emphasis for P0 through P9 P5 and P6 are the only presets used for the calibration of the stress signal				BW: 50 GHz M8040A Sampling rate: 160 GSa/s Memory depth: 4.096 kpts Averaging: 128	BW: 50 GHz M8040A Sampling rate: 256 GSa/s Memory depth: 6.554 kpts Averaging: 256
RJ	0.5	0.6	ps _{rms}	BW: 33 GHz Sampling rate: 160 GSa/s Memory depth: 10 Mpts Averaging: off	BW: 33 GHz Sampling rate: 256 GSa/s Memory depth: 16 Mpts Averaging: off
SJ @ 100 MHz 1 ps	0.8	1.0	ps _{pp}	BW: 33 GHz Sampling rate: 160 GSa/s Memory depth: 10 Mpts Averaging: off	BW: 33 GHz Sampling rate: 256 GSa/s Memory depth: 16 Mpts Averaging: off
SJ @ 100 MHz 5 ps	5.0	5.5	ps _{pp}		

PCI Express 5.0 32 GT/s – M8040A

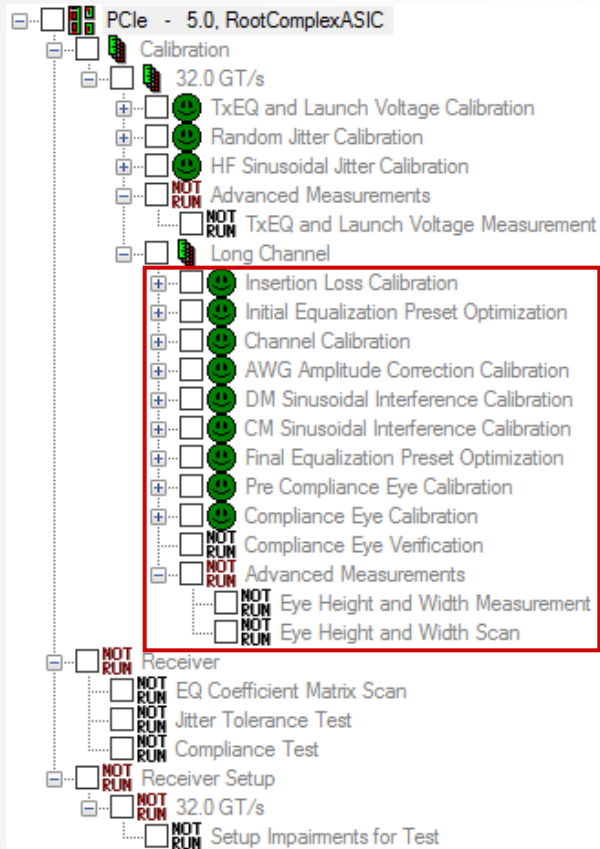
BASE SPECIFICATION TP2P CALIBRATION SETUP



PCI Express 5.0 – Base Specification



CALIBRATION 32 GT/s RX STRESS SIGNAL – TP2P CALIBRATION SETTINGS



Parameter	Min	Max	Unit	Oscilloscope Settings	
				X-Series / Q-Series V-Series / Z-Series	UXR
Insertion Loss @ 16 GHz	-37	-34	dB	VNA measurements; root and end point reference package models need to be taken into account	
DM-SI @ 2.1 GHz 25 mV	28	30	mV _{pp}	BW: 5 GHz Sampling rate: 160 GSa/s Memory depth: 2 Mpts Averaging: off Reference package model embedding required	BW: 5 GHz Sampling rate: ? GSa/s Memory depth: ? Mpts Averaging: off Reference package model embedding required
DM-SI @ 2.1 GHz 14 mV	8	10	mV _{pp}		
CM-SI @ 120 MHz	148	150	mV _{pp}	BW: 5 GHz Sampling rate: 160 GSa/s Memory depth: 2 Mpts Averaging: off Reference package model embedding required	BW: 5 GHz Sampling rate: ? GSa/s Memory depth: ? kpts Averaging: off Reference package model embedding required
TxEQ Preset selection	Largest eye height * eye width		mVps	BW: 33 GHz Sampling rate: 160 GSa/s Memory depth: 2.05 kpts Averaging: 1024 Reference package model embedding required	BW: 33 GHz Sampling rate: 256 GSa/s Memory depth: 3.278 kpts Averaging: 1024 Reference package model embedding required
V_{RX-EW-8G} Eye Height	AIC & System: 13.5 to 15.5		mV	BW: 33 GHz Sampling rate: 160 GSa/s Memory depth: 2.05 kpts	BW: 33 GHz Sampling rate: 256 GSa/s Memory depth: 3.278 kpts
T_{RX-EW-8G} Eye Width	AIC & System: 18.25 to 19.25		ps	Averaging: 1024 Reference package model embedding required	Averaging: 1024 Reference package model embedding required

PCIe 5.0 RX Tests

32 GT/s BASE SPECIFICATION – RX TESTS

The screenshot displays the PCIe N5991 Test Automation software interface. The main window is titled "PCIe N5991 Test Automation (Version: 2.00.20190426Beta1)". The interface is divided into several sections:

- Toolbar:** Includes icons for NEW, LOAD, SAVE, EXPORT, RESET, START, ABORT, PAUSE, and ABOUT.
- Tree View:** A hierarchical tree on the left shows the test configuration. The "Receiver" section is highlighted with a red box, containing:
 - Receiver
 - 32.0 GT/s
 - 32G Rx EQ Coefficient Matrix Scan
 - 32G Rx Jitter Tolerance Test
 - 32G Rx Pre-Compliance Test
- 32G Rx Impairments Setup:** A detailed configuration panel on the right, including:
 - Offline: True
 - Repeat Setup: False
 - Generator:**
 - Pre-Shoot: 1.9 dB
 - De-Emphasis: 0 dB
 - Differential Voltage: 790 mV
 - Common Mode Interference: 150 mV
 - Differential Mode Interference: 25.3 mV
 - Random Jitter: 500 fs
 - Sinusoidal Jitter: 3.125 ps
 - Sinusoidal Jitter Frequency: 210 MHz
 - 2nd Tone Sinusoidal Jitter: 1.77 ps
 - 2nd Tone Sinusoidal Jitter: 210 MHz
 - Sequencer:**
 - Procedure Error Case Behavior: Abort Sequence
 - Procedure Failed Case Behavior: Proceed With Next Procedure
 - Repetitions: 0
- Repetitions:** A section at the bottom of the configuration panel.
- Log:** A table at the bottom showing test progress:

Severity	Message	Date
Info	32G Rx Impairments Setup started	6/11/2019 1:02:35 PM
Progress	32G Rx Impairments Setup: Step 0	6/11/2019 1:03:23 PM

• EQ Coefficient Matrix Scan

- Measures the BER per cell of the coefficient matrix dependent on

- User can definably coefficient resolution
- User limits for the matrix search
- User setting for target BER

• Jitter Tolerance Test

- Measures the jitter tolerance of the DUT and compares against Swept SJ mask

- User setting for target ber
- User definable start / stop frequencies and frequency steps
- Selection of search algorithms

• Compliance Test

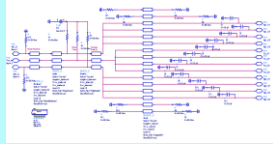
- Performs RX compliance test with 100 MHz SJ frequency point

• Receiver Setup Impairments

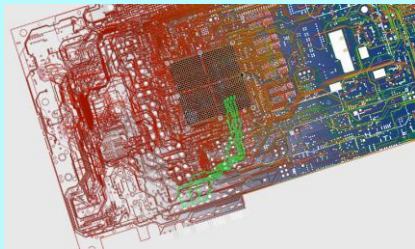
- Setup of M8000 BERT systems to user defined impairments by using the calibration tables of the test automation

PCI Express® 5.0 – Keysight Total Solution

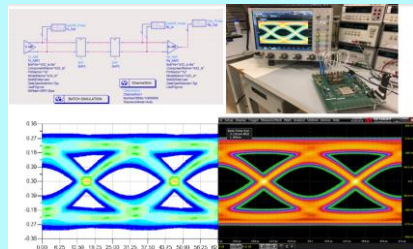
Physical Layer – System Simulation



ADS Design Software



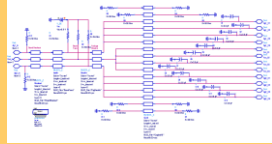
SIPro/PIPro



Simulation to Measurement Correlation

Complete System Simulation
From Pre-layout analysis to Post-layout extraction

Physical layer – interconnect design



ADS design software



86100D DCA-X/TDR



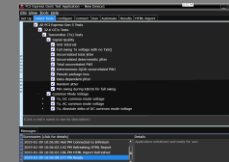
N5227B PNA w/ PLTS

Verify PCIe 5.0 Compliant Channels
Verify Return Loss Compliance
Capture break-out channel S-Params

Physical layer-transmitter test



UXR-Series, Z-Series Real-Time Oscilloscopes



D9050PCIC PCI Express 5.0 TX Electrical compliance software



86100CU-400 PLL and Jitter Spectrum Measurement SW

DSA UXR-Series & Z-Series Real-Time Oscilloscopes

Physical layer-receiver test

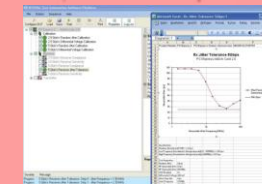


M8046A J-BERT High Performance BERT w/ integrated CDR + M80454A Interference Source

M8049A-1 Substitute PCIe 5 BASE Channel board



N5991PB5A PCIe 5.0 32GT/s RX Test software



Automated RX Test software
- Accurate, Efficient
- Comprehensive RX Testing

Questions?

