

# From Simulation to Test

## Be Ready for PCIe Gen5 Design Challenge

TU Nash

2019.3.12

Application Engineer



# Outline

- PCIe Gen5 Testing Solution and Challenge
- Lab1: ADS Channel Simulator Overview
- Lab2: PCIE Gen5 Overview
  - CTLE
  - DFE
  - Channel Tolerance
  - Jitter
  - EYE
- Lab3: PCIe Gen5 Testbench
- Lab4: Repeater (Retimer/ Redriver) Usage
- Lab5: PCIe Gen5 Testbench with Retimer
- Summary

# Hot Keys – Schematic

## Edit Commands

Following table lists the hot keys for the Edit menu options.

Menu Name	Default
Edit > Copy	Ctrl+C
Edit > Copy/Paste > Copy Using Reference	C
Edit > Cut	Ctrl+X
Edit > Delete	Del
Edit > End Command	Esc
Edit > Mirror About X	Shift+X
Edit > Mirror About Y	Shift+Y
Edit > Move > Move Component Text	F5
Edit > Move > Move Edge	
Edit > Move > Move Using Reference	M
Edit > Move > Move Wire Endpoint	Ctrl+Shift+M
Edit > Paste	Ctrl+V
Edit > Redo	Ctrl+Y
Edit > Rotate	Ctrl+R
Edit > Undo	Ctrl+Z

## View Commands

Following table lists the hot keys for the View menu options.

Menu Name	Default
View > Clear Highlighting	F8
View > Command Quick Help	Shift+F1
View > Grid Display	Ctrl+G
View > Origin Crosshair	Shift+O
View > Pan View	Tab
View > Pop Out Of Hierarchy	B
View > Push Into Hierarchy	Shift+E
View > Restore Last View	Ctrl+L
View > View All	F
View > Zoom > Zoom Area	
View > Zoom > Zoom By Factor > Zoom In x2	+
View > Zoom > Zoom By Factor > Zoom Out x2	-
View > Zoom > Zoom To Selected	Z

## Insert Commands

Following table lists the hot keys for the Insert menu options.

Menu Name	Default
Insert > Change Entry Layer To	Ctrl+Shift+C
Insert > Component > Component Library...	I
Insert > Measure...	Ctrl+M
Insert > Shape > Polygon	Shift+P
Insert > Shape > Rectangle	R
Insert > Shape > Undo Vertex	Backspace
Insert > Text	Ctrl+T
Insert > Wire	Ctrl+W

## Window and Miscellaneous Cor

Following table lists the hot keys for the Window and Miscellaneous

Menu Name	Default
Window > Close	Ctrl+F4
Window > Layout	Ctrl+Shift+L
Window > Open Another Schematic Window	Ctrl+Shift+S
Help > Topics and Index	F1
Options > Snap Enabled	Ctrl+E
Select > Select All	Ctrl+A
Simulate > Simulate	F7

- Help > F1

# Hot Keys – Data Display

## File Command

Following table lists the File menu commands

Menu Name	Default
File > New	Ctrl+N
File > Open...	Ctrl+O
File > Print...	Ctrl+P
File > Save	Ctrl+S

## Edit Commands

Following table lists the Edit menu commands

Menu Name	Default
Edit > Copy	Ctrl+C
Edit > Cut	Ctrl+X
Edit > Delete	Del
Edit > End Command	Esc
Edit > Paste	Ctrl+V
Edit > Redo	Ctrl+Y
Edit > Select All	Ctrl+A
Edit > Undo	Ctrl+Z

## View Commands

Following table lists the View menu commands

Menu Name	Default
View > Grid Display	Ctrl+G
View > Restore Last View	Ctrl+L
View > View All	F
View > Zoom > Zoom Area	
View > Zoom > Zoom In x2	+
View > Zoom > Zoom Out x2	-

## Miscellaneous Commands

Following table lists the various other menu commands such as

Menu Name	Default
Help > Topics and Index	F1
Marker > New...	Ctrl+M
Options > Hide ADS Logo on all plots	Alt+L
Options > Snap Enabled	Ctrl+E
Window > Close	Ctrl+F4
Window > New	Ctrl+Shift+D

- Help > F1

# ADS Tips Forum (ADS小秘訣) [www.keysight.com/find/ADS\\_tips](http://www.keysight.com/find/ADS_tips)

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标题	作者	最近的活跃	检视	0	0	2	0
2019 大学学术论文 (shared in Keysight EESof Design Forum)	Jiarui Wu	2019年11月12日 下午 07:36:58	529	0	0	2	0
Keysight EDA 软件免费学习资源汇总-2019.11	Jiarui Wu	2019年11月7日 下午 06:13:28	5368	2	2	0	0
新入职工程师必看视频 - ADS Basic (YOUKU)	XUYue	2019年10月14日 上午 12:44:51	1706	0	0	0	0
新入职工程师必看视频 - SystemVue Basic - Communication (YouTube)	Jiarui Wu	2019年10月1日 下午 05:32:54	238	0	0	0	0
新入职工程师必读课程 - 微波单片集成电路设计 (MMIC)	xindong	2019年9月17日 下午 11:38:28	1671	0	0	0	0
新入职工程师必读课程 - 射频匹配 (RF Matching)	XUYue	2019年9月17日 下午 10:00:23	5922	0	0	4	0
新入职工程师必看视频 - ADS Basic (YouTube)	SharonChen	2019年9月15日 下午 11:37:13	319	0	0	0	0
新入职工程师必读课程 - 三维电磁仿真 (EMPro)	zeyu.yi@keysight.com	2019年9月9日 下午 08:28:01	2830	0	1	2	0
新入职工程师必读课程 - 通信系统 (SystemVue)	Jiarui Wu	2019年7月23日 上午 05:14:33	5244	2	1	1	0
新入职工程师必读课程 - IBIS AMI 建模 (SystemVue+ADS)	Jiarui Wu	2019年6月11日 上午 02:41:00	1918	0	0	0	0
新入职工程师必读课程 - 半导体器件建模 (Device Modeling)	ShaoliV	2019年6月10日 下午 05:56:42	1282	0	0	0	0
新入职工程师必读课程 - 信号完整性 (Signal Integrity)	Chih Yuan Tu	2019年6月9日 下午 11:18:44	4904	0	2	0	0
SystemVue 通信实验教程 (适用于高校)	Jiarui Wu	2019年2月1日 下午 05:55:09	3584	0	1	0	0
2018 Train The Teacher 培训材料 (通信/SystemVue部分)	Jiarui Wu	2019年2月1日 下午 05:55:05	1097	0	1	0	0

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所有内容 (60) 文件 (2) 讨论区 (0) 问题 (58) 视讯 (0)

依动作筛选: [无] 依分享的内容筛选

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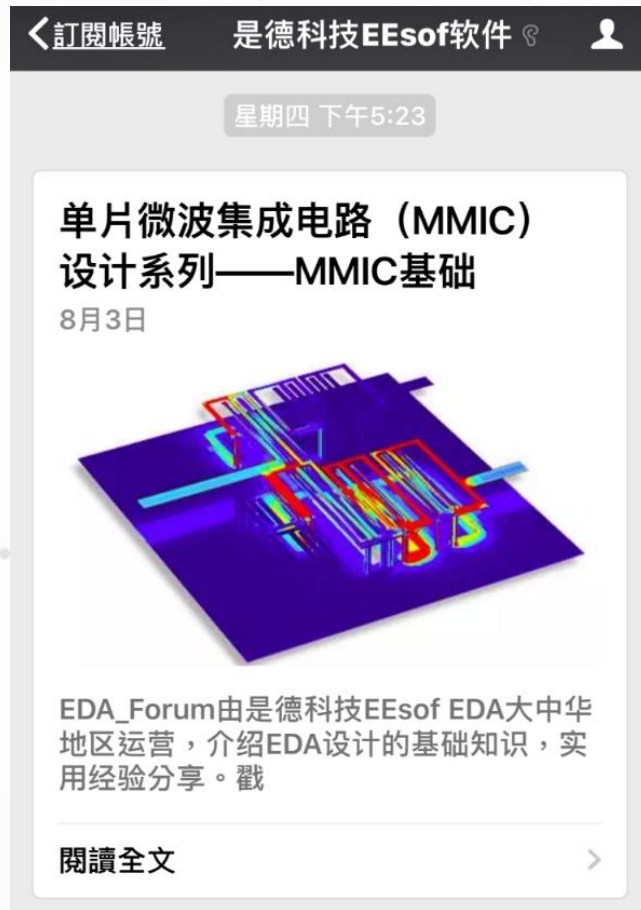
标题	作者	最近的活跃	检视	0	0	2	0
Power Integrity Workshop	Chih Yuan Tu	2019年12月16日 上午 07:20:05	1017	2	0	2	0
2019 大学学术论文 (shared in Keysight EESof Design Forum)	Jiarui Wu	2019年11月12日 下午 07:36:58	529	0	0	2	0
EESof Design Forum 2019 (Hsinchu and Shanghai)	Chih Yuan Tu	2019年10月30日 下午 05:37:05	275	0	0	0	0
[HSD] 2019OCT_FlexDCA&COM Workshop	Chih Yuan Tu	2019年10月14日 下午 05:51:03	175	0	0	0	0
[Workshop] 2019Q4 RF Basic - Efficient Impedance Matching with ADS	SharonChen	2019年9月23日 上午 12:08:34	929	0	0	0	0
FY17Q2 Workshop_ EMI辐射干扰 (RE) 仿真	zeyu.yi@keysight.com	2019年8月27日 下午 04:21:20	663	0	0	0	0
FY19Q2 Workshop: Optical Module SI/EMI Simulation	zeyu.yi@keysight.com	2019年8月25日 上午 12:03:24	579	0	0	4	0
[Workshop] 2019Q4 Understanding PCB Effects in DC-DC Converters	JasonChen	2019年8月23日 下午 05:30:33	252	0	0	0	0
ADS2019 SI/PI Seminar (西安、苏州、南京、深圳和北京)	Xiuguo	2019年8月9日 下午 07:05:50	915	0	0	1	0
2017Q1_SSO Simulation with Power Aware IBIS Model within ADS	Chih Yuan Tu	2019年7月29日 下午 05:54:58	214	1	0	0	0
2016Q1_Advanced SI Simulation Skills	Lin_Ming_Chih	2019年7月22日 下午 11:07:55	2081	0	0	0	0
2019.6.11/13 深圳上海ADS电源完整性仿真与测量训练营资料	zhangtao	2019年6月15日 上午 12:15:19	1040	0	0	3	0
全新射频匹配流程_ADS2019Update1.0	XUYue	2019年5月5日 上午 06:22:38	958	0	0	0	0

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1、分享信号完整性 (SI) 、电源完整性 (PI) 、电磁兼容性和微波射频方面的知识/行业信息及动态； 2、不定期举办线下/上公益活动； 3、帮助大家更好的学习和了解硬件、高速电路、微波射频电路、EMC和高速PCB的设计。 SIPIEMC

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## 輕鬆談電路模擬

2019年12月17日 星期二

### 減少去耦合電容的數量

PCB電源平面上常並聯很多顆去耦合電容，用來抑制電源分配網路的阻抗。這些去耦合電容最早可能是出現在IC設計公司提供的公板。系統廠會依據需求修改公板，但多不會、也不敢拿掉去耦電容。但每一顆電容都關係生產成本，研發能減少一顆電容，就能為公司減少一顆電容的成本。所以，減少PCB上去耦合電容是研發直接貢獻公司利潤的機會。

要減少去耦合電容的數量，先要找出沒有在工作的電容。以是德科技的ADS為例，ADS中的PIPro可以抽取PCB電源平面的S參數。將電源平面的S參數連上去耦合電容，可以算出電源分配網路的阻抗，也能看出每一顆電容有多少電流流過。沒有電流流過，或電流量極小的電容，都是可以去除的目標電容。去掉這些電容，再次檢查電源分配網路的阻抗，如果還能確定符合IC設計公司提供的限制線的要求，那就對了。

於 12月17, 2019 沒有留言:



標籤: Power Integrity

#### 關於我自己



[tonychen.tau](#)

Tony Chen 目前任职于德科技，为EDA软件业务处大中国区应用工程部经理。

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#### 網誌存檔

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[實際案例：傳輸線模擬的結果與測試結果不同](#)

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# PCIe Gen5 Testing Solution and Challenge

# Keysight PCIe Gen5 Application solution

Jacky Yu

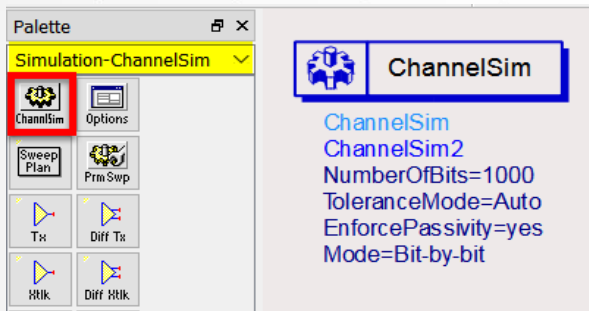
2020.MARCH

Keysight Taiwan Technologies

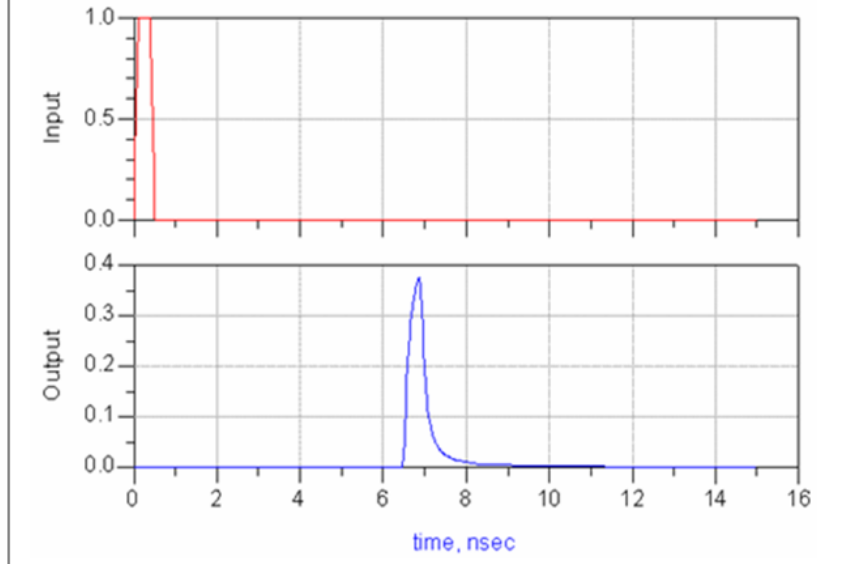


# Lab1 ADS Channel Simulator Overview

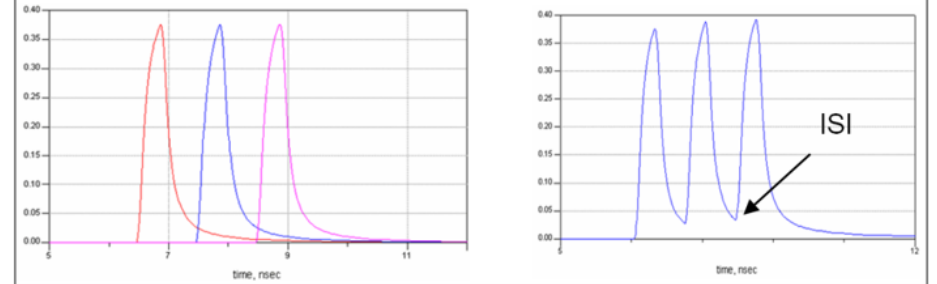
# Channel Simulator Methodology



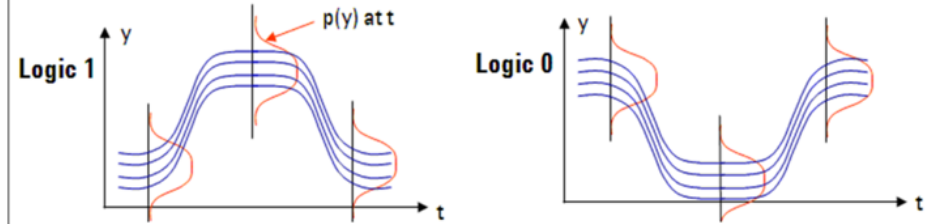
Impulse response is calculated using a short, traditional transient simulation



Bit by bit mode : Superposition of bits



Statistical mode : Statistical techniques



# Comparison of Simulation Techniques

	Netlists & IBIS traditional flow	IBIS AMI flow: Bit-by-bit (“time-domain”) mode	IBIS AMI flow: Statistical mode
Method	Computational expensive: Modified nodal analysis of Kirchoff’s current laws	Bit-by-bit superposition of impulse responses	Statistical calculations based on impulse response
BER floor 1 minute	$\sim 10^{-3}$	$\sim 10^{-6}$	$\sim 10^{-18}$ or lower
Applicability & Restrictions	NLTV analog & channel  NLTV Tx/Rx	LTI analog & channel* <small>*SystemVue and ADS can handle NLTV mid-channel repeaters as specified in IBIS 6.0</small> NLTV Tx/Rx	LTI analog & channel  LTI Tx/Rx



# IBIS-AMI Introduction

- I/O Buffer Information Specification (IBIS)
- Algorithmic Model Interface (AMI)

# Two Kinds of AMI Model

Two Kinds of Tx/Rx Plus a "Dual" or "Hybrid" model		Model's Init_Returns_Impulse flag is:	
		False ("Can't be modeled as LTI")	True ("LTI model via impulse response")
Model's GetWave_Exists flag is	False ("Model is pure LTI")	Empty model: not allowed	Typical case for Tx and simple Rx's (fixed Eq. and no CDR)
	True ("NLTV model via waveform modification")	Typical case for Rx (Adaptive Eq., CDR)	Buyer beware: LTI approximation of NLTV device if used in stat mode

Table 1. Two kinds of AMI model, plus a "hybrid"

# Statistical Mode

		Tx model's Init_Returns_Impulse flag is	
		False ("Tx cannot be modeled nor approximated as LTI")	True ("Tx can be modeled as LTI using AMI_Init()")
Rx model's Init_Returns_Impulse flag is	False ("Rx cannot be modeled nor approximated as LTI")	Not recommended. ChanSim issues warning	Not recommended. ChanSim issues warning
	True ("Rx can be modeled as LTI using AMI_Init()")	Not recommended. ChanSim issues warning.	"Case 1"

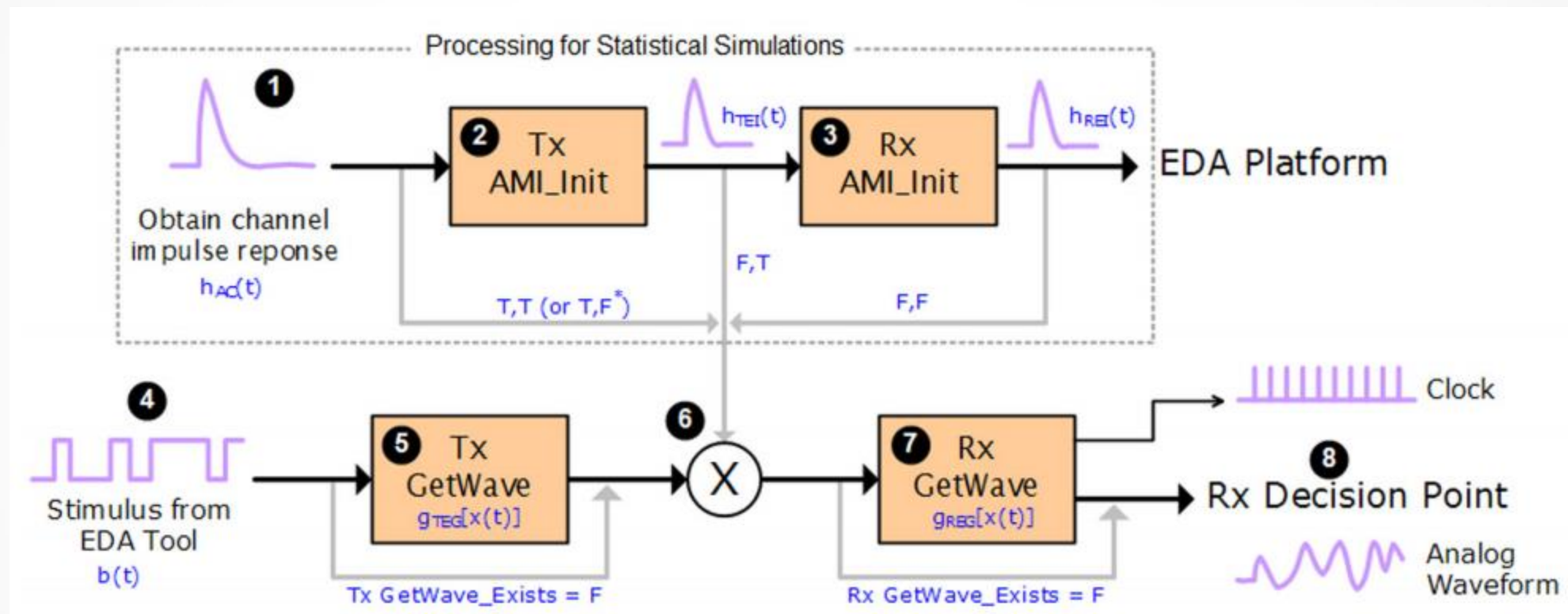
*Table 2a. Channel Simulator set to statistical mode*

# Bit-By-Bit Mode

		Tx model's GetWave_Exists flag is	
		False ("Tx does not have AMI_GetWave()")	True ("Tx has AMI_GetWave()")
Rx model's GetWave_Exists flag is	False ("Rx does not have AMI_GetWave()")	"Case 2"	"Case 5" (Practically never used)
	True ("Rx has AMI_GetWave()")	"Case 3" (Most common case)	"Case 4"

*Table 2b. Channel simulator set to bit-by-bit mode. (Note: In IBIS 5.0, there was a third flag ("Use\_Init\_Output") besides the present Init\_Returns\_Impulse and GetWave\_Exists flags. However, this flag caused much confusion and so Use\_Init\_Output is deprecated in IBIS 5.1.)*

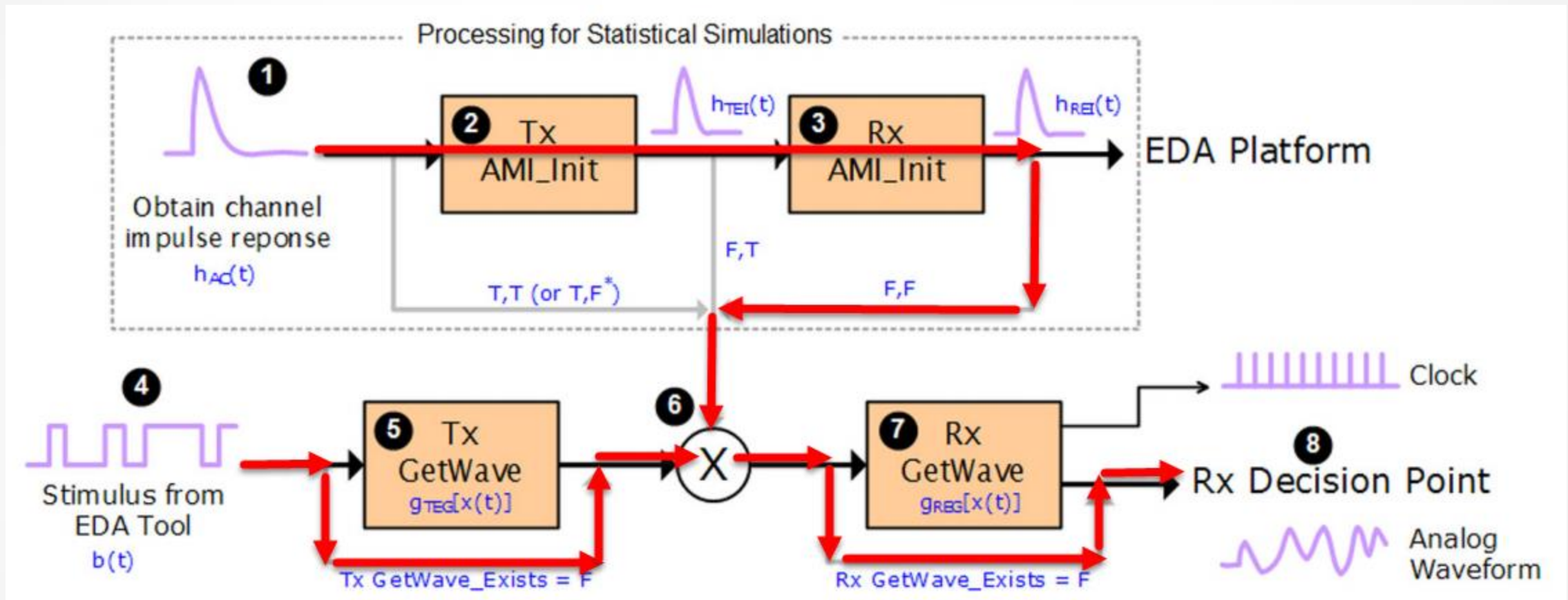
# AMI Simulation Flow



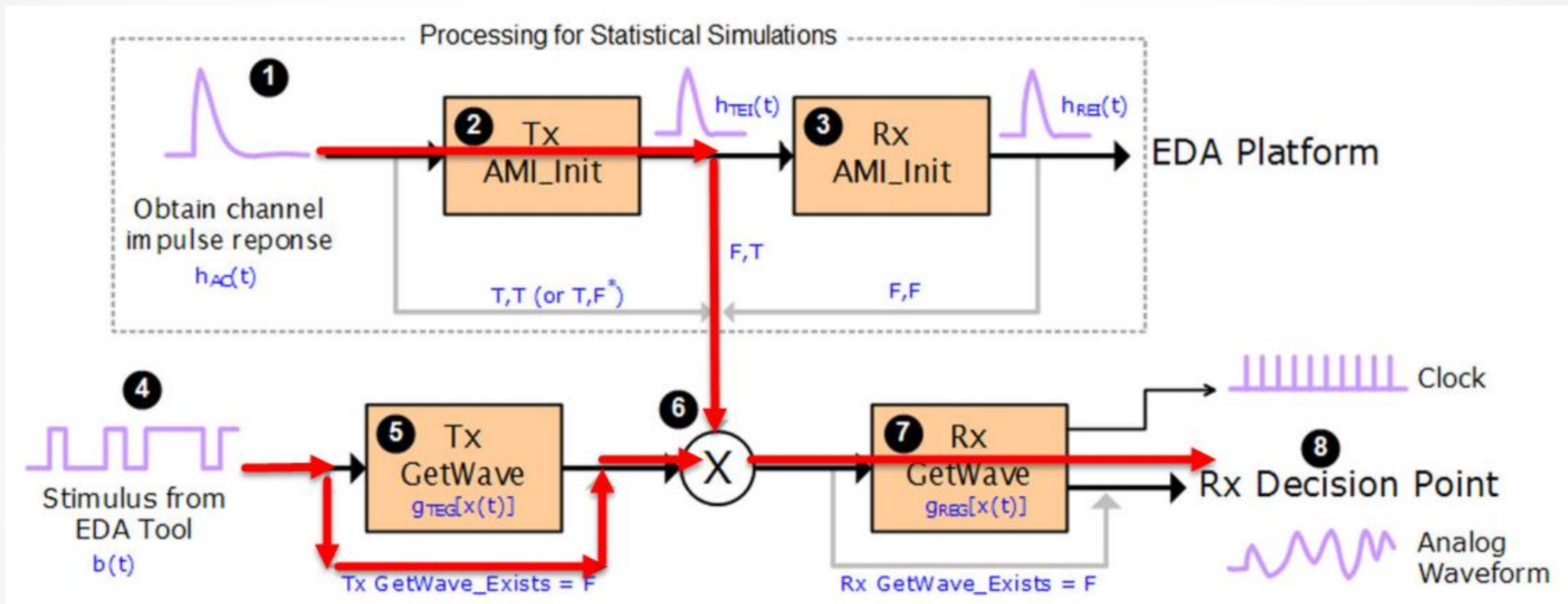
<https://www.keysight.com/sg/en/assets/7018-03143/application-notes/5990-9111.pdf?success=true>



# Statistical (TX Init, RX Init)



# Bit-by-bit (TX Init, RX GetWave)

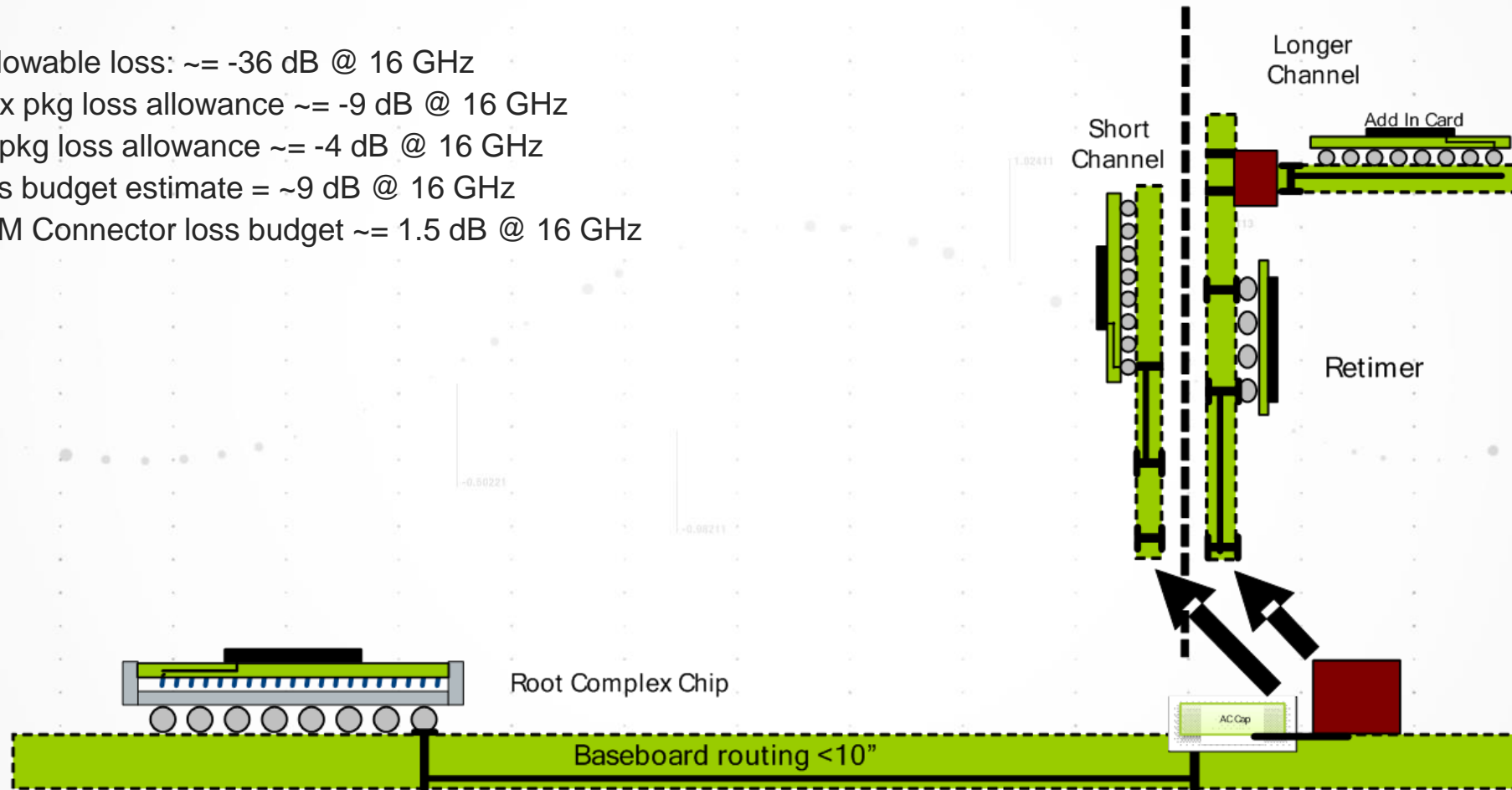


# Lab2 PCIe Gen5 Overview

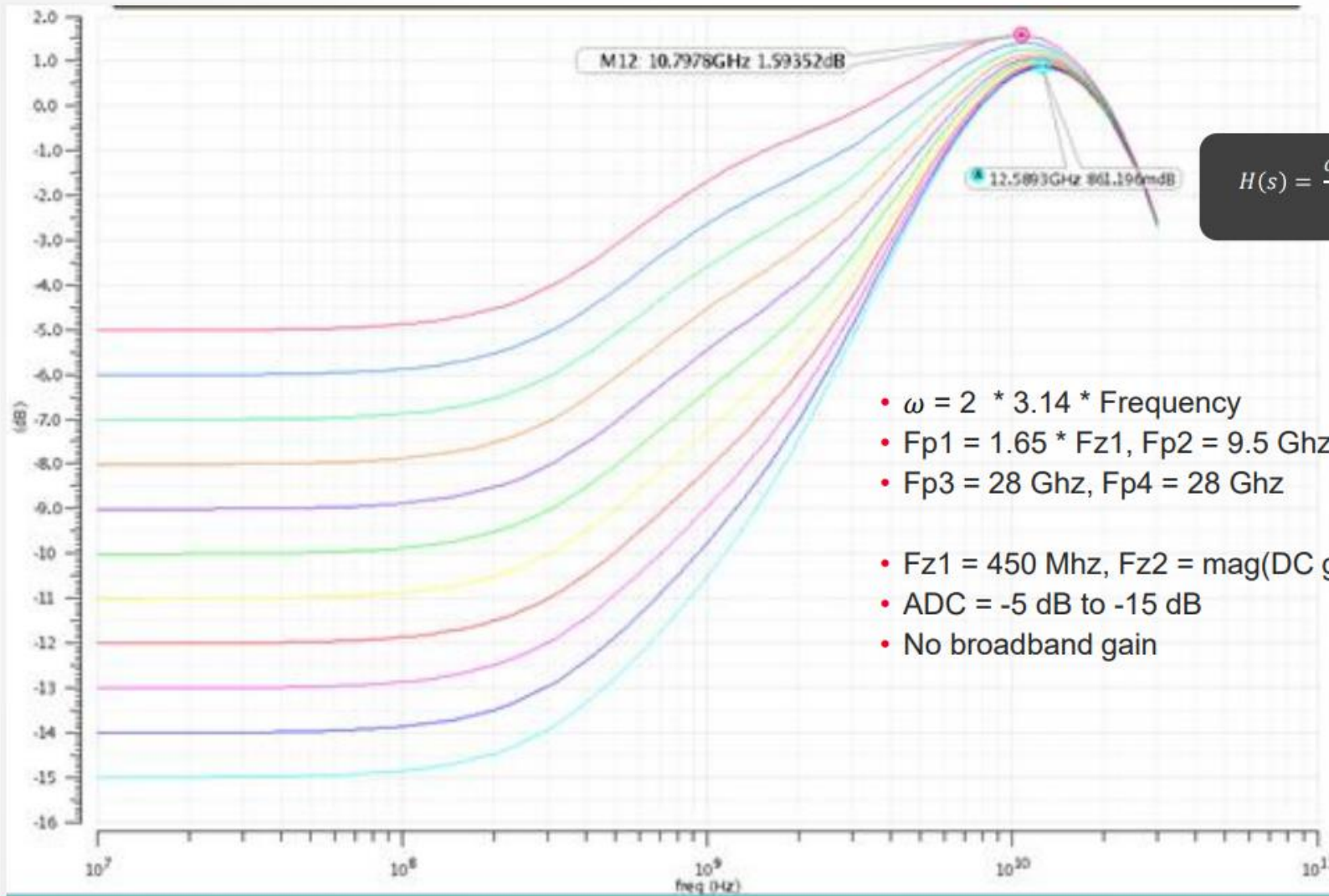
# PCI Express 5.0 Channel Topology

RETIMER REQUIRED WHEN LOSS EXCEEDS -36 DB OR >1 CONNECTOR

- Estimated allowable loss:  $\approx -36$  dB @ 16 GHz
- Root complex pkg loss allowance  $\approx -9$  dB @ 16 GHz
- Add-in Card pkg loss allowance  $\approx -4$  dB @ 16 GHz
- Total AIC loss budget estimate =  $\approx 9$  dB @ 16 GHz
- PCIe 5.0 CEM Connector loss budget  $\approx 1.5$  dB @ 16 GHz



# CTLE (-5 to -15dB)



$$H(s) = \frac{\omega_{p1} * \omega_{p3} * \omega_{p4}}{\omega_{z1}} * \frac{(s + \omega_{z1})(s + \omega_{p2} * A_{DC})}{(s + \omega_{p1})(s + \omega_{p2})(s + \omega_{p3})(s + \omega_{p4})}$$

- $\omega = 2 * 3.14 * \text{Frequency}$
- $F_{p1} = 1.65 * F_{z1}$ ,  $F_{p2} = 9.5 \text{ GHz}$ ,
- $F_{p3} = 28 \text{ GHz}$ ,  $F_{p4} = 28 \text{ GHz}$
- $F_{z1} = 450 \text{ Mhz}$ ,  $F_{z2} = \text{mag}(\text{DC gain}) * F_{p2}$
- $A_{DC} = -5 \text{ dB to } -15 \text{ dB}$
- No broadband gain



# CTLE (-15dB)

Edit CTLE Parameters:1

Preset  Custom

$$H(s) = A_{pre} \frac{(s - \omega_{z1})(s - \omega_{z2}) \cdots}{(s - \omega_{p1})(s - \omega_{p2})(s - \omega_{p3}) \cdots}$$

Added zeros in rad/s:   
(z2[int(CTLE)+1])\*(2\*pi)

Zero:  rad/s

Added poles in rad/s:   
(-9.5)\*(2\*pi)\*1e9  
(-28)\*(2\*pi)\*1e9  
(-28.0001)\*(2\*pi)\*1e9

Pole:  rad/s

Prefactor:

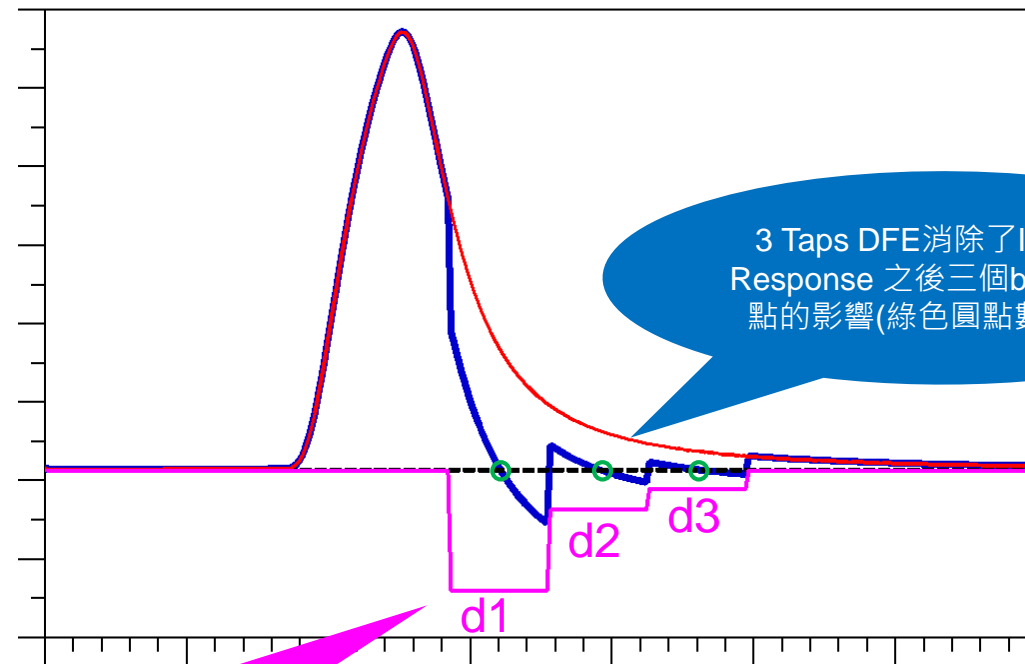
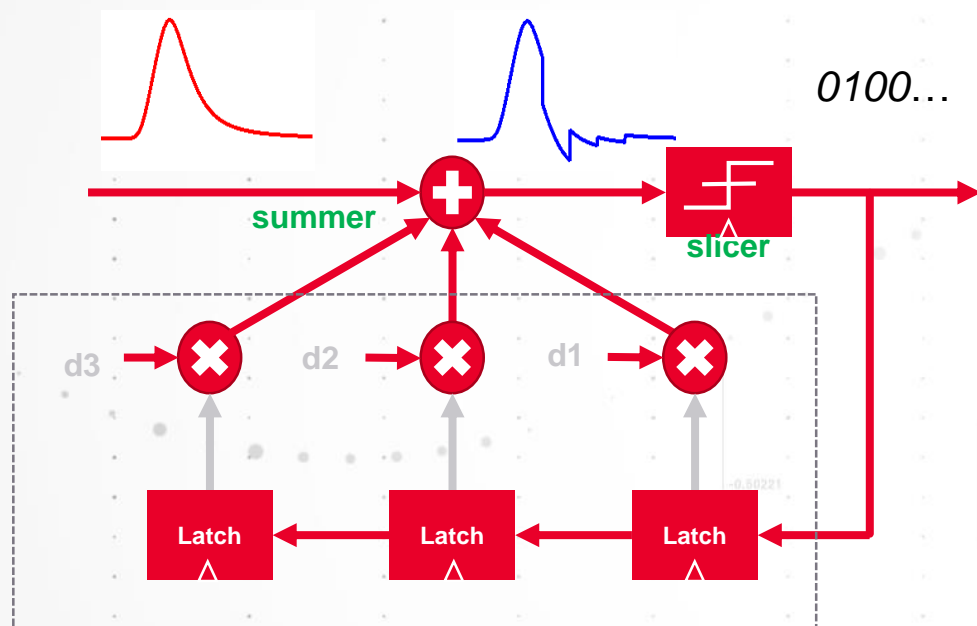
Message  
Zero 1: -0.45 GHz; Zero 2: -1.69 GHz.  
Pole 1: -0.743 GHz; Pole 2: -9.5 GHz; Pole 3: -28 GHz; Pole 4: -28.0001 GHz.

Log Scale  Linear Scale

Frequency Response

OK Apply Cancel Help

# DFE (Decision Feed-back Equalizer)



粉紅色曲線是補償訊號，與輸入訊號(紅色曲線)相加之後得到輸出訊號(藍色曲線)

# DFE

- $d1 = \left(\frac{h1}{h0}\right) \leq 0.8$
- $|d2, d3| \leq 20mV$

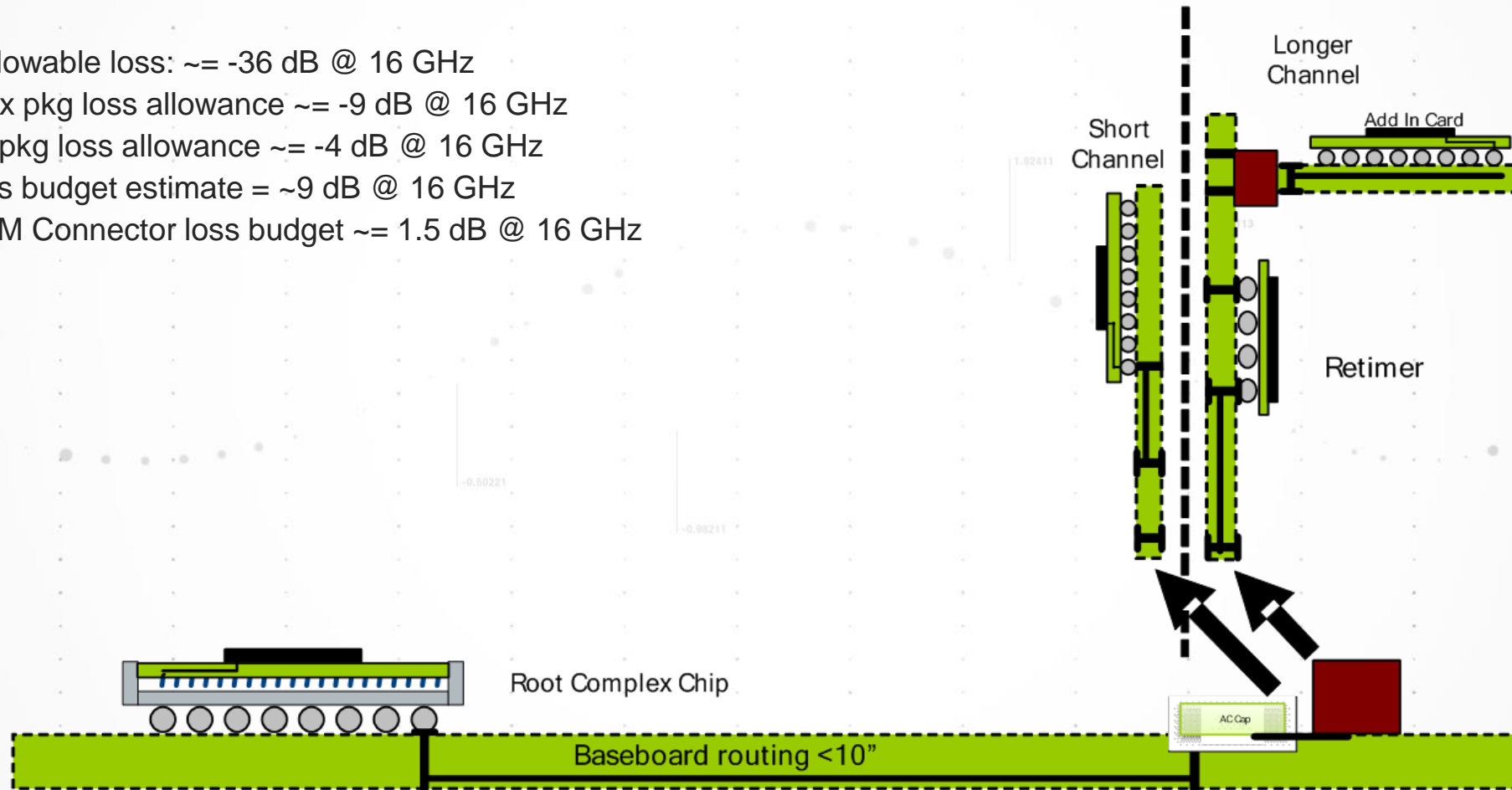
Note:

h1: tap magnitude

h0: cursor strength

# Channel Tolerance

- Estimated allowable loss:  $\approx -36$  dB @ 16 GHz
- Root complex pkg loss allowance  $\approx -9$  dB @ 16 GHz
- Add-in Card pkg loss allowance  $\approx -4$  dB @ 16 GHz
- Total AIC loss budget estimate =  $\approx 9$  dB @ 16 GHz
- PCIe 5.0 CEM Connector loss budget  $\approx 1.5$  dB @ 16 GHz



# Jitter

$T_{TX-CH-URJ-32G}$	Tx uncorrelated Rj	0.276	ps RMS
$T_{TX-CH-UDJDD-32G}$	Tx uncorrelated DjDD	1.875	ps PP
$T_{TX-CH-UPW-RJ-32G}$	Uncorrelated PW Rj	0.27	ps RMS
$T_{TX-CH-UPW-DJ-32G}$	PW DDj	2.5	ps PP

Label	Jitter Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units
jit_hfrj_nui	Tx Rj (HF+LF) edge	0.000	1.422	1.105	0.394	0.222	ps
T-TX UDJDD	Tx Dj (HF+LF) edge	100.000	30.000	12.000	6.250	3.125	ps
TTX-CH-URJ	Tx Rj (LF) + Clk Rj edge	3.450	3.450	1.314	0.710	0.276	ps
TTX-CH-UDJDD	Tx Dj (LF) edge	20.000	20.000	7.000	3.750	1.875	ps
TTX-CH-UPW-RJ	Tx Rj (HF) PW	1.420	1.420	0.995	0.533	0.267	ps
TTX-CH-UPW-DJ	Tx Dj (HF) PW	80.000	40.000	10.000	5.000	2.500	ps
Total Jitter	T-TX UTJ + Clk Rj		93.614	41.619	21.648	9.767	

Label	Jitter Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units
Tx_Rj	Tx Rj (HF) edge			0.704	0.377	0.188	ps
Tx_Dj	Tx Dj (HF) edge			5.000	2.500	1.250	ps
Tx_DCD							
Rx_Rj	Tx Rj (LF) + Clk Rj edge			1.314	0.710	0.276	ps
Rx_Dj	Tx Dj (LF) edge			7.000	3.750	1.875	ps
Rx_DCD							
Rx_Noise							
Tx Total Jitter	Tx Dj + Tx Rj			14.90	7.80	3.90	ps
Rx Total Jitter	Rx Dj + Rx Rj			25.49	13.73	5.76	ps
Total Jitter	Tx + Rx			40.39	21.54	9.66	ps
T_TX_UTJ + T_REFCLK_RMS	Total Jitter check (over-est)			41.62	21.65	9.77	ps

- Deterministic **edge** jitter = (1/2) Deterministic **pulse width** jitter
- Random **edge** jitter = (1/sqrt(2)) Random **pulse width** jitter



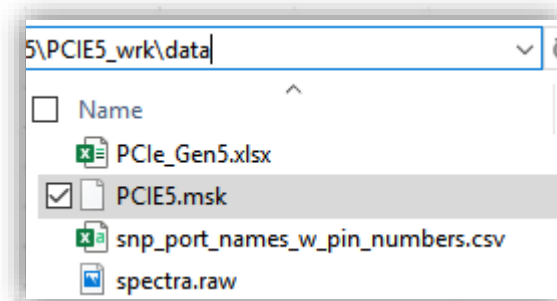
# Total RJ Verification

Label	Jitter Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units
Rj check 1	Tx Rj + Rx Rj			1.491	0.804	0.334	ps
Rj check 2	Tx Rj (HF+LF) + Clk Rj			1.491	0.804	0.334	ps
Rj check 3	Tx Rj (HF) + Tx Rj (LF) + Clk Rj			1.491	0.804	0.334	ps

Label	Jitter Parameter	Formula
Rj check 1	Tx Rj + Rx Rj	$\sqrt{\text{Tx\_Rj}^2 + \text{Rx\_Rj}^2}$
Rj check 2	Tx Rj (HF+LF) + Clk Rj	$\sqrt{\text{jit\_hfrj\_nui}^2 + \text{T\_REFCLK\_RMS}^2}$
Rj check 3	Tx Rj (HF) + Tx Rj (LF) + Clk Rj	$\sqrt{((\text{TTX\_CH\_UPW\_RJ}/\sqrt{2})^2) + \text{TTX\_CH\_URJ}^2}$

# EYE

- *Eye Height*  $\leq 15mVPP$
- *Eye Width at zero crossing*  $\leq 0.3UI$



```
PCIE5.msk
```

```
1 1 /* This is the first polygon index */
2 4 /* This is the number of vertices */
3 /* UI, V */
4 0.35,0
5 0.5,0.0075
6 0.65,0
7 0.5,-0.0075
```

# Lab3 PCIe Gen5 Testbench

# ADS TX/RX Model

The screenshot displays the ADS 2020 interface for a schematic titled "Testbench\_g5 [PCIE3\_lib:Testbench\_g5:schematic] (Schematic):2".

- File Explorer (Left):** Shows the project structure under "C:\Demo\ADS\Application\\_Workshops\FY20Q2\". The selected folder is "Testbench\_g5", containing "schematic", "Testbench\_g5.dds", "Testbench\_g5\_AMI", "Testbench\_g5\_AMI.dds", "Testbench\_g5\_retimer", and "Testbench\_g5\_retimer.dds".
- Parts List (Right):** Lists simulation components:
  - ChannelSim:** ChannelSim, Number of Bits=1000, Tolerance Mode=Auto, Enforce Passivity=no, Mode=Bit-by-bit.
  - BATCH SIMULATION:** BatchSimController, BatchSim1, Var="CTLE", Start=0, Stop=10, Step=5, Lin, Var="Preset", Start=0, Stop=9, Step=5, Lin, Use Sweep Plan=yes, Analysis[1]=ChannelSim 1, Use Sweep Plan Module=no, Sweep Argument=, Use Separate Processes=yes, Merge Datasets=yes, Remove Datasets=yes.
- Schematic (Center):** Shows a transmitter (Tx) and receiver (Rx) connected to a channel. The Tx is labeled "Tx" with parameters "Tx\_Diff", "Tx\_Dm2", and "BTRate=datarate". The Rx is labeled "Rx" with parameters "Rx\_Diff" and "Rx\_Dm1". The channel is labeled "SnP" with "SnP1" and "-36dB @ 18GHz". Two eye diagrams are shown: "Eye\_Probe beforeRX" and "Eye\_Probe afterRX".
- Simulation Parameters (Bottom Right):**
  - TX EQ:** VAR Preset, pre=[0.0,0.0,0.0,-0.1,-0.125,-0.1,-0.125,-0.167], main=[0.75,0.833,0.8,0.875,1.0,0.9,0.875,0.7,0.75,0.833], post=[-0.25,-0.167,-0.2,-0.125,0.0,0,-0.2,-0.125,0].
  - RX EQ:** VAR CTLE, z=[-5.34e9,-4.76e09,-4.24e9,-3.78e9,-3.37e9,-3.00e9,-2.68e9,-2.39e9,-2.13e9,-1.9e9,-1.69e9].

# ADS TX/RX Model (TX PRBS)

The screenshot displays the ADS software interface with the 'Channel Simulation Tx2' dialog box open. The dialog box has several tabs: PRBS, Encoder, EQ, Electrical, Jitter, and Display. The PRBS tab is active, showing the following settings:

Parameter	Value	Unit
Bit rate	datarate	None
Vhigh	voltageSwing	None
Vlow	-1*voltageSwing	None
Rise/Fall time	risefalltime	None

Below these settings, the Mode is set to 'Maximal Length LFSR'. The Register length is 32. The Taps are set to '\*10001110\*', the Seed is '\*10101010\*', and the Bit sequence is '\*0000000111'. There is a 'Bit File' field with a 'Browse...' button.

A note at the bottom of the dialog box states: "Note: In statistical mode, there is no bit pattern, and thus the bit pattern settings are ignored. Statistical mode is based on the stochastic properties of a conceptually infinite, non-repeating bit pattern."

The schematic diagram in the background shows a TX block connected to a TX EQ block, which is then connected to an RX EQ block. The TX block is labeled 'Tx\_Diff' and 'Tx\_Diff2' with 'BitRate=datarate'. The TX EQ block is labeled 'TX EQ' and 'VAR2' with 'Preset=9' and 'CTLE=0'. The RX EQ block is labeled 'RX EQ' and 'VAR6' with 'datarate=32e9', 'UI=1/datarate', 'voltageSwing=0.8', and 'risefalltime=0.33\*UI'. The Jitter block is labeled 'VAR' and 'Jitter' with 'TXRJ=0.188e-12', 'TXDJ=1.25e-12', 'RXRJ=0.276e-12', and 'RXDJ=1.875e-12'. A red arrow points from the 'Tx\_Diff2' instance name in the dialog box to the TX block in the schematic.

# ADS TX/RX Model (TX Preset)

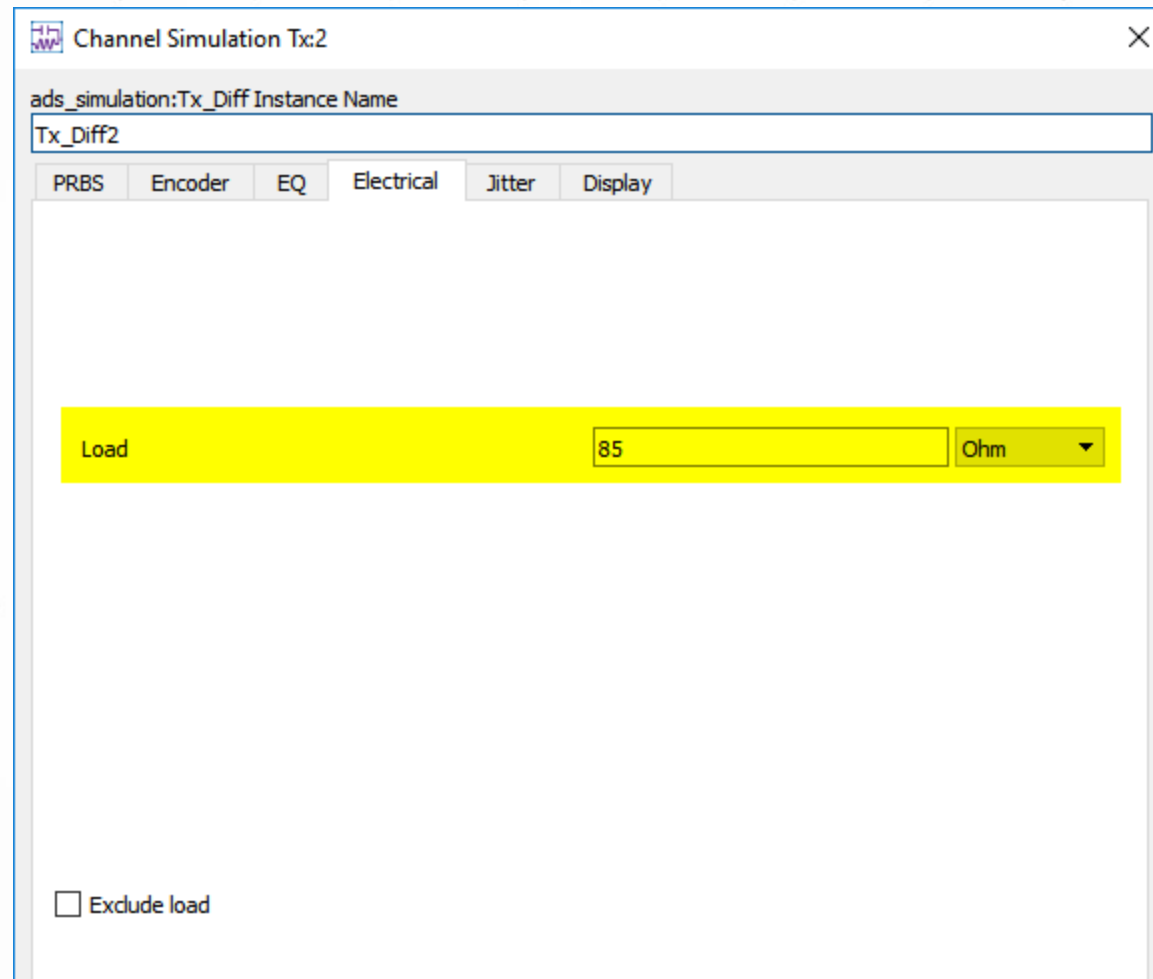
The screenshot displays the ADS software interface. The main window is titled "Testbench\_g5 [PCIE3\_lib:Testbench\_g5:schematic] \* (Schematic):2". A "Channel Simulation Tx:2" dialog box is open, showing the "EQ" tab. The "Choose equalization method" dropdown is set to "Specify FIR taps". The "De-emphasis (dB)" field is empty. The "Pre Cursor" section contains a text box with the formula  $\text{PreCursor}[1] = \text{pre}[\text{int}(\text{Preset}) + 1]$  and a "Name" field. The "Post Cursor" section contains a text box with the formula  $\text{PostCursor}[0] = \text{main}[\text{int}(\text{Preset}) + 1]$  and a "Name" field. The "Tap Interval (UI)" field is set to 1.0. The background schematic shows a transmission line model with components labeled "SnP SnP1", "Rx\_Diff", and "Rx\_Diff1". A yellow highlight in the schematic shows the following values for the "VAR Preset" and "VAR CTLE" parameters:

```
pre={0,0,0,0,0,-0.1,-0.125,-0.1,-0.125,-0.167}
main={0.75,0.833,0.8,0.875,1,0.9,0.875,0.7,0.75,0.833}
post={-0.25,-0.167,-0.2,-0.125,0,0,-0.2,-0.125,0}
```

The "VAR CTLE" parameter is defined as  $z2 = \{-5.34e9, -4.76e09, -4.24e9, -3.78e9, -3.37e9, -3.00e9, -2.6\}$ .



# ADS TX/RX Model (TX Source Impedance)



# ADS TX/RX Model (TX Jitter)

The screenshot displays the ADS software interface. The main window is titled "Testbench\_g5 [PCIE3\_lib:Testbench\_g5:schematic] \* (Schematic):2". A "Channel Simulation Tx:2" dialog box is open, showing the configuration for "ads\_simulation:Tx\_Diff Instance Name" and "Tx\_Diff2". The "Jitter" tab is selected, and the "Specify the jitter PDF:" checkbox is checked. The "DJRJ:" option is selected, with the following parameters: Sigma(UI) = TXRJ/UI, Min(UI) = -1\*TXDJ/UI, and Max(UI) = TXDJ/UI. The "Display" tab is also visible, showing various parameters like DCD (UI), Clock DCD (UI), PJ amplitude, and PJ frequency. The background schematic shows a block diagram with variables like VAR1, VAR2, CTLE=0, TX EQ, VAR6, datarate=32e9, UI=1/datarate, voltageSwing=0.8, risefalltime=0.33\*UI, and Jitter parameters: TXRJ=0.188e-12, TXDJ=1.25e-12, RXRJ=0.276e-12, and RXDJ=1.875e-12.

# ADS TX/RX Model (RX CTLE)

The image shows the ADS Channel Simulation Rx2 interface. A configuration dialog for the RX CTLE is open, with the 'Continuous-time linear equalizer (CTLE)' section highlighted in yellow. The 'Enable' checkbox is checked. The 'Feed-forward equalizer (FFE)' section is also visible, with 'Optimized' selected for initial tap calculation. The 'Decision-feedback equalizer (DFE)' section has 'Enable' checked and 'Optimized' selected for initial tap calculation. The 'Tap file' section shows an output file named 'dfe.txt'. The 'Advanced settings' section has an 'Edit advanced settings' button.

The background circuit diagram shows a receiver model with a CTLE block. A red arrow points from the CTLE configuration dialog to the CTLE block in the circuit. The circuit diagram includes a signal source, a filter, and a receiver block labeled 'Rx\_Diff Rx\_Diff1'. The signal source is labeled '36dB @16GHz'. The receiver block is labeled 'Rx\_Diff Rx\_Diff1'. The CTLE block is labeled 'CTLE'. The CTLE block is highlighted in yellow. The CTLE block is labeled 'z2={-5.34e9,-4.76e09,-4.24e9,-3.78e9,-3.37e9,-3.00e9,-2.68e9,-2.39e9,-2.13e9,-1.9e9,-1.69e9}'. The CTLE block is labeled 'z2={-5.34e9,-4.76e09,-4.24e9,-3.78e9,-3.37e9,-3.00e9,-2.68e9,-2.39e9,-2.13e9,-1.9e9,-1.69e9}'.

```
VAR Preset
pre={0,0,0,0,0,-0.1,-0.125,-0.1,-0.125,-0.167}
matn={0.75,0.833,0.8,0.875,1,0.9,0.875,0.7,0.75,0.833}
post={-0.25,-0.167,-0.2,-0.125,0,0,0,-0.2,-0.125,0}

VAR CTLE
z2={-5.34e9,-4.76e09,-4.24e9,-3.78e9,-3.37e9,-3.00e9,-2.68e9,-2.39e9,-2.13e9,-1.9e9,-1.69e9}
```

# ADS TX/RX Model (RX CTLE)

The image shows the ADS software interface for configuring a TX/RX model. The main window displays parameters for TX EQ and RX EQ. The RX EQ section is highlighted, showing a CTLE (Continuous-time linear equalizer) configuration. A red box highlights the 'Edit...' button in the 'Edit poles and zeros' section. A red arrow points from this button to the 'Edit CTLE Parameters' dialog box.

The 'Edit CTLE Parameters' dialog box shows the transfer function  $H(s) = A_{pre} \frac{(s - \omega_{z1})(s - \omega_{z2}) \dots}{(s - \omega_{p1})(s - \omega_{p2})(s - \omega_{p3}) \dots}$ . The 'Added zeros in rad/s' section contains two entries:  $(-0.45) \cdot (2\pi) \cdot 1e9$  and  $(z2 \cdot \text{int}(CTLE - 1)) \cdot (2\pi)$ . The 'Added poles in rad/s' section contains four entries:  $(-0.743) \cdot (2\pi) \cdot 1e9$ ,  $(-9.5) \cdot (2\pi) \cdot 1e9$ ,  $(-28) \cdot (2\pi) \cdot 1e9$ , and  $(-28.0001) \cdot (2\pi) \cdot 1e9$ . The 'Prefactor' is set to  $5.1e22$ .

The 'Message' section displays the following information: Zero 1: -0.45 GHz; Zero 2: -5.34 GHz; Pole 1: -0.743 GHz; Pole 2: -9.5 GHz; Pole 3: -28 GHz; Pole 4: -28.0001 GHz.

Below the message section, there are two plots: 'Frequency Response' (Magnitude in dB vs Frequency in GHz) and 'Phase degree' (Phase in degree vs Frequency in GHz). Both plots show a blue curve with red markers indicating the locations of the zeros and poles.

# ADS TX/RX Model (RX 3-tap DFE)

The image shows the ADS Channel Simulation Rx2 dialog box overlaid on a schematic diagram. The dialog box is configured for a Decision-Feedback Equalizer (DFE) with 3 taps. The schematic shows a signal path through a multiplexer (SnP1) and a receiver block (Rx) labeled Rx\_Diff1. The receiver block is connected to a signal source (SnP1) and a signal sink (SnP1). The schematic also shows a signal path through a multiplexer (SnP1) and a receiver block (Rx) labeled Rx\_Diff1. The signal path is labeled with a gain of -36dB @16GHz. The schematic also shows a signal path through a multiplexer (SnP1) and a receiver block (Rx) labeled Rx\_Diff1. The signal path is labeled with a gain of -36dB @16GHz. The schematic also shows a signal path through a multiplexer (SnP1) and a receiver block (Rx) labeled Rx\_Diff1. The signal path is labeled with a gain of -36dB @16GHz.

**Channel Simulation Rx2**  
ads\_simulation:Rx\_Diff Instance Name  
Rx\_Diff1

EQ Electrical Jitter Display

Continuous-time linear equalizer (CTLE)  
 Enable Edit poles and zeros Edit...

Feed-forward equalizer (FFE)  
Initial tap calculation  
 Enable Precursor taps 2 Postcursor taps 4 Edit taps Edit...  
 Adaptive equalization  File  Manual

**Decision-feedback equalizer (DFE)**  
Initial tap calculation  
 Enable Taps 3 Edit taps Edit...  
 Adaptive equalization  File  Manual  
Slicer output 1/-1

Tap file  
Input Browse... Edit...  
Output "dfe.txt" Browse...

Advanced settings  
Edit advanced settings Edit...

OK Apply Cancel Help

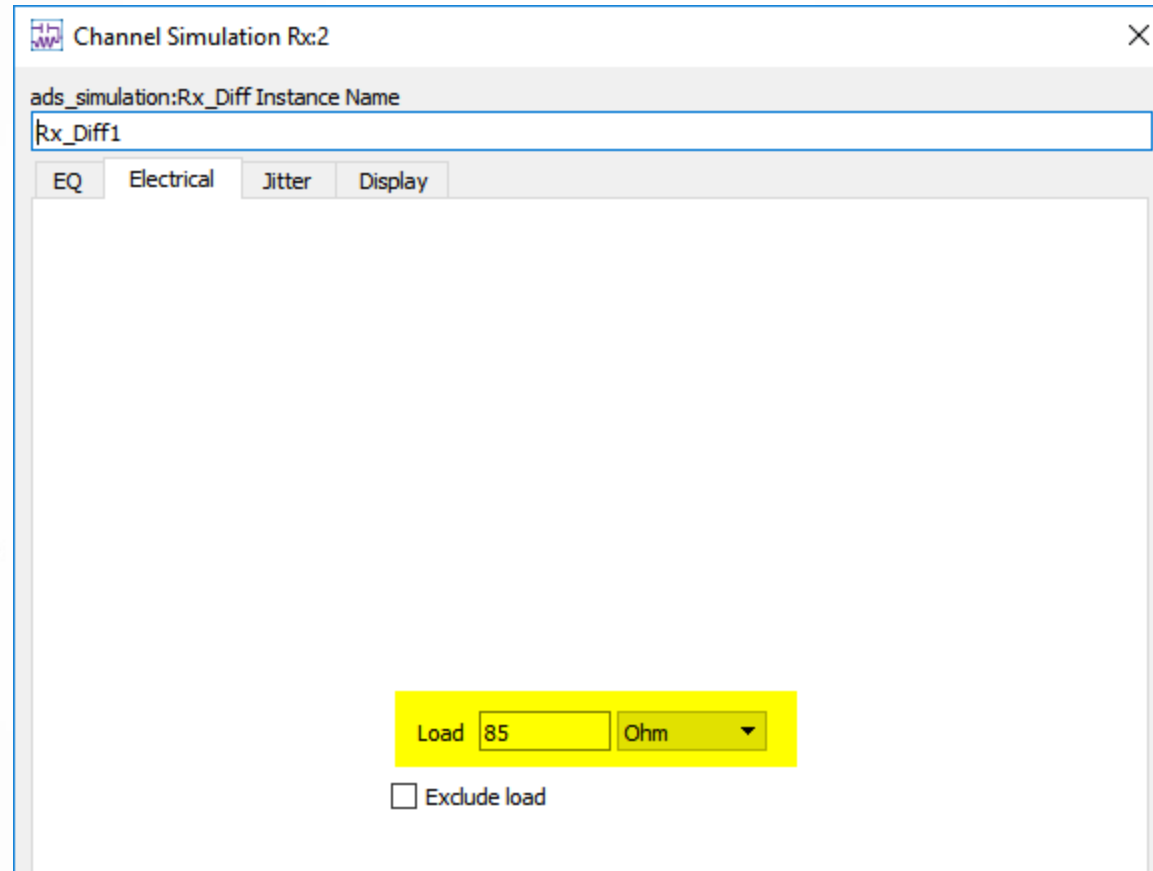
Right-click: Drag to pan the window.

Rx\_Diff Rx\_Diff1 ads\_device:drawing 7.125, 2.750 0.625, 0.000 in

VAR Preset  
pre={0.0,0.0,0.0,-0.1,-0.125,-0.1,-0.125,-0.167}  
main={0.75,0.833,0.8,0.875,1,0.9,0.875,0.7,0.75,0.833}  
post={-0.25,-0.167,-0.2,-0.125,0.0,0,-0.2,-0.125,0}

VAR CTLE  
z2={-5.34e9,-4.76e09,-4.24e9,-3.78e9,-3.37e9,-3.00e9,-2.68e9,-2.39e9,-2.13e9,-1.9e9,-1.69e9}

# ADS TX/RX Model (RX Load Impedance)





# ADS TX/RX Model (RX Jitter)

The screenshot shows the 'Channel Simulation Rx:2' dialog box with the 'Jitter' tab selected. The instance name is 'Rx\_Diff1'. Under 'Specify the jitter PDF:', the 'DJRJ' option is selected. The 'Sigma(UI)' field is set to 'RXRJ/UI', 'Min(UI)' is '-1\*RXDJ/UI', and 'Max(UI)' is 'RXDJ/UI'. To the right, a list of variables is shown, including 'VAR2' (Preset=9, CTLE=0), 'VAR6' (data rate=32e9, UI=1/data rate, voltageSwing=0.8, risefalltime=0.33\*UI), and 'VAR Jitter' (TXRJ=0.188e-12, TXDJ=1.25e-12, RXRJ=0.276e-12, RXDJ=1.875e-12).

Channel Simulation Rx:2

ads\_simulation:Rx\_Diff Instance Name  
Rx\_Diff1

EQ Electrical Jitter Display

SJ Amplitude (UI)

Amplitude noise (V)

Specify the jitter PDF:

Random: Sigma(UI)

DJRJ: Sigma(UI)  Min(UI)  Max(UI)

Dual-Dirac: Sigma(UI)  Mean1(UI)  Mean2(UI)

VAR Eqn VAR2  
Preset=9  
CTLE=0

VAR Eqn VAR6  
data rate=32e9  
UI=1/data rate  
voltageSwing=0.8  
risefalltime=0.33\*UI

VAR Eqn VAR Jitter  
TXRJ=0.188e-12  
TXDJ=1.25e-12  
RXRJ=0.276e-12  
RXDJ=1.875e-12

# EYE Probe

Eye\_Probe:2

ads\_simulation:Eye\_Probe Instance Name

RX\_out

Parameters Measurements Display

Bit Error Rate Contour

Contour width and height for this BER value: 1e-12

Draw contour and calculate width and height corresponding to each value in this BER list: list(1e-12)

Extrapolate in bit-by-bit mode

Transient Analysis

Name of the VtPRBS source: Data rate 1.0 Gbps  Save transient analysis output for all named nodes (Warning: Saving all nodes can lead to a very big dataset file)

Use Eye Mask

"PCIE5.msk" Browse View/Edit

DDR4 Mask

Width (UI) 0 Height 0.0 V  Customize Vertical Center 0.0 V  Mask Group 1

More...

OK Apply Cancel Help

Eye\_Probe:5

ads\_simulation:Eye\_Probe Instance Name

RX\_out

Parameters Measurements Display

Measurement Selection

Available

- LevelMean
- Level1
- JitterRMS
- RiseTime
- Level0
- CheckMaskViolation
- SNR
- Amplitude
- HeightDR

>> Add >>

<< Remove <<

Selected

- HeightAtBER
- Density
- Height
- Width
- WidthAtBER
- Bathtub
- Contour

Remove All


Add All

Measurement Info


This probe computes the eye diagram related measurements. save a particular measurement, select the measurement from the list on the left and use the 'Add' button.

OK Apply Cancel

# Batch CTLE and Preset

 ChannelSim

ChannelSim  
ChannelSim1  
NumberOfBits=1000  
ToleranceMode=Auto  
EnforcePassivity=no  
Mode=Bit-by-bit

 BATCH SIMULATION

BatchSimController  
BatchSim1  
Var="CTLE" Start=0 Stop=10 Step=6 Lin=  
Var="Preset" Start=0 Stop=9 Step=5 Lin=  
UseSweepPlan=yes  
Analysis[1]="ChannelSim1"  
UseSweepModule=no  
SweepModule=""  
SweepArgument=  
UseSeparateProcess=yes  
MergeDatasets=yes  
RemoveDatasets=yes

BatchSimulation:2

BatchSimController Instance Name  
BatchSim1

Sweep Simulation Display

Use sweep plan  Use sweep module

Sweep Plan

z2 Add

Var="CTLE" Start=0 Stop=10 Step=6 Lin=  
Var="Preset" Start=0 Stop=9 Step=5 Lin=

Sweep Type Linear

Start/Stop  Center/Span

Start 0 None  
Stop 10 None  
Step-size 6 None  
Num. of pts. 3

Up Down Remove

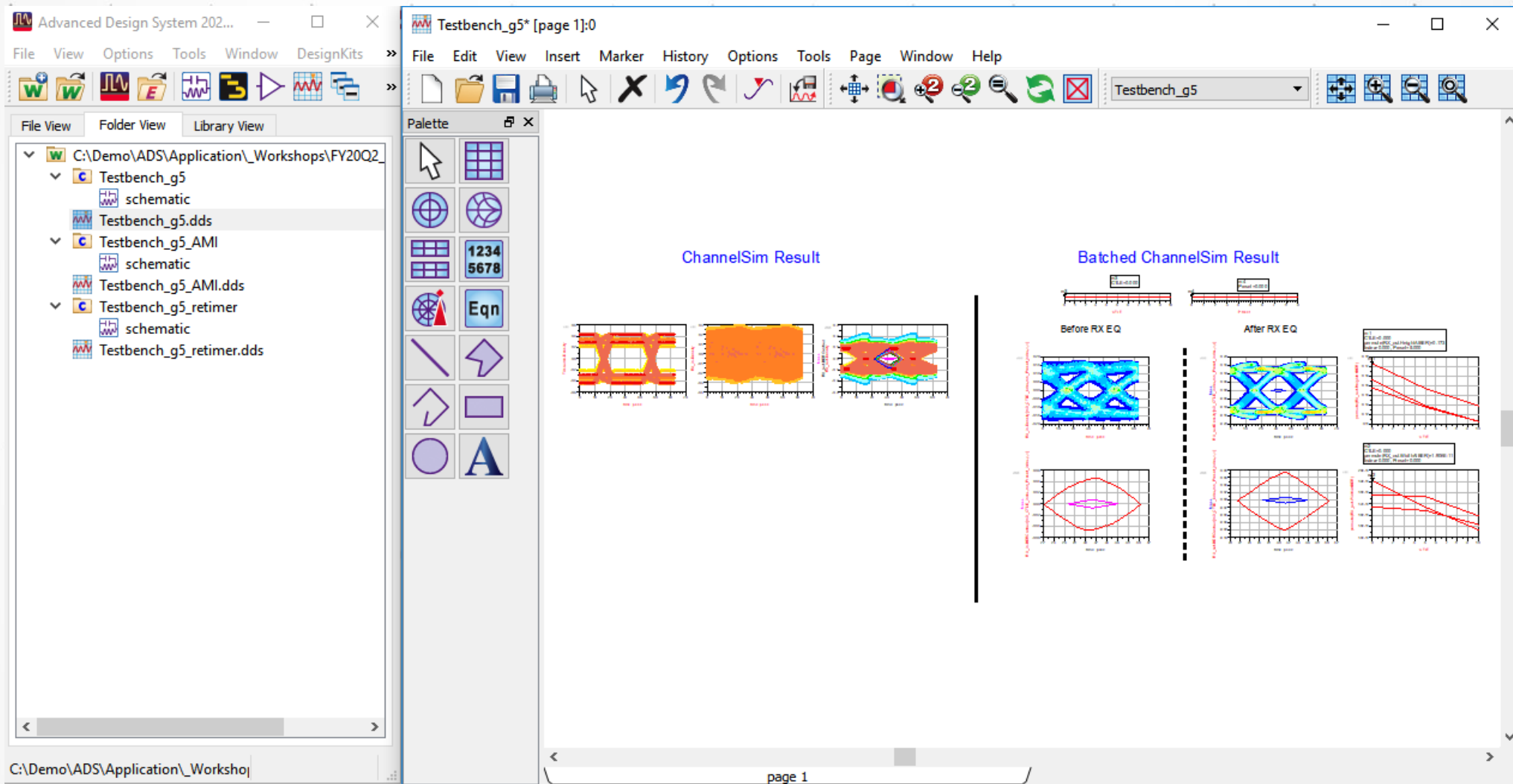
Sweep Module

Module name

File name Browse... Edit...

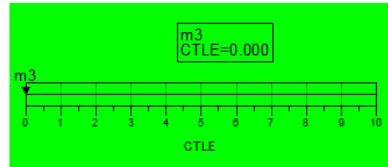
OK Apply Cancel Help

# Results (38s, 9 scenarios)

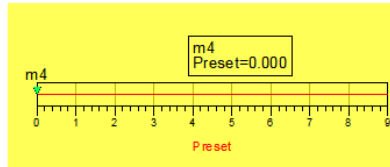


# Best Setup, In terms of EYE\_Height and EYE\_Width

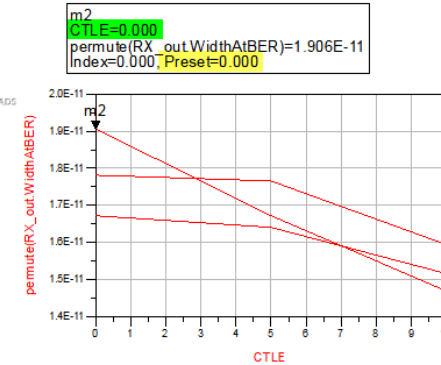
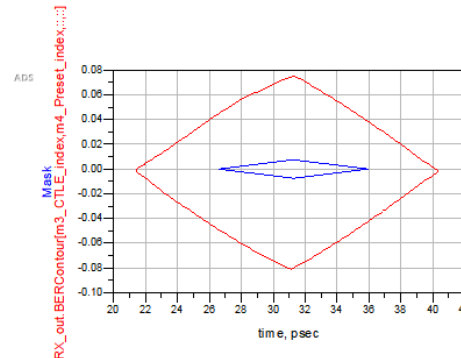
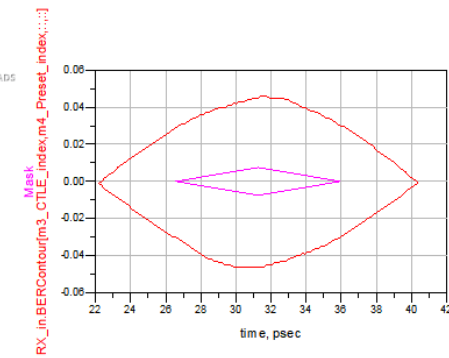
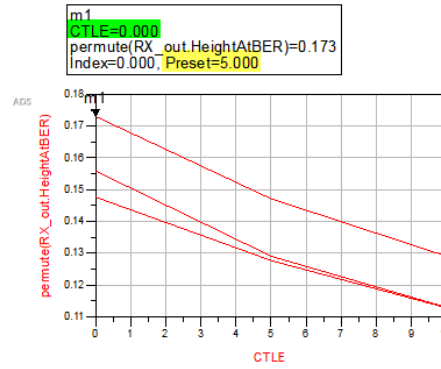
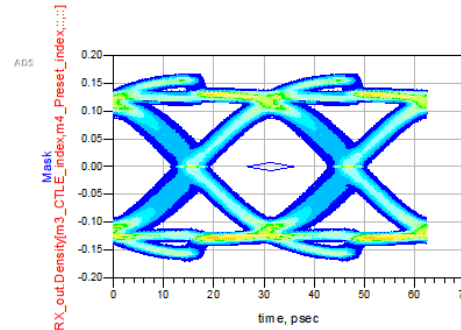
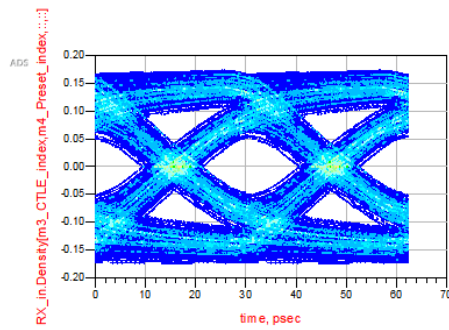
## Batched ChannelSim Result



Before RX EQ



After RX EQ



# Gen5 AMI Model and Testbench

- 5\PCIE5\_wrk\data\g5\_AMI
- | Name                   |
|------------------------|
| eesof_pcie5_rx.ami     |
| eesof_pcie5_rx.ibs     |
| eesof_pcie5_rx_x64.dll |
| eesof_pcie5_tx.ami     |
| eesof_pcie5_tx.ibs     |
| eesof_pcie5_tx_x64.dll |

The screenshot displays the Advanced Design System (ADS) 2021 interface for a schematic titled "Testbench\_g5\_AMI [PCIE3\_lib:Testbench\_g5\_AMI:schematic] (Schematic):5".

**File View:** Shows a project structure with folders for "Testbench\_g5" and "Testbench\_g5\_AMI", each containing "schematic" and ".dds" files. A "Testbench\_g5\_retimer" folder is also present.

**Parts Panel:** Lists simulation components such as "ChannelSim", "Sweep Plan", "Tx", "Rx", "Tx Cphy", "Rx Cphy", "Tx AMI", "Rx AMI", "Tx Retimer", and "Rx Retimer".

**Simulation-ChannelSim:** Shows parameters for "ChannelSim 1":  
NumberOfBits=1000  
ToleranceMode=Auto  
EnforcePassivity=no  
Mode=Bit-by-bit

**BATCH SIMULATION:** Shows parameters for "BatchSim 1":  
Var="CTLE" Start=0 Stop=10 Step=5 Lin=  
Var="Preset" Start=0 Stop=0 Step=5 Lin=  
UseSweepPlan=yes  
Analysis[1]="ChannelSim1"  
UseSweepModule=no  
SweepArgument=  
UseSeparateProcess=yes  
MergeDatasets=yes  
RemoveDatasets=yes

**VAR:** Shows parameters for "VAR 2":  
Preset=0  
CTLE=0  
cte\_ami=(CTLE+5)\*(-1)

**Schematic:** The main workspace shows a signal path from a "Tx AMI" block through a channel (labeled "36GB @ 16GHz") to an "Rx AMI" block. The channel is connected to a "SIP1" component. Eye diagrams are shown at the input and output of the Rx AMI block, labeled "EyeDiff\_Probe RX\_in" and "Eye\_Probe RX\_out".



# Gen5 AMI Model (TX Preset)

**Tx AMI:5**

Tx\_AMI Instance Name: Tx\_AMI1

IBIS File: g5\_AMI\eesof\_pcie5\_tx.ibs

Component: eesof\_pcie5\_tx

Set all data: Typ

Use package

Channel Index: 0

Package | Pin | Model | I-V Data | Driver Schedule | SubModel | Alias | **AMI** | PRBS | Encoder | Display

AMI file: C:\Demo\ADS\Application\Workshops\FY20Q2\_PCIE5\PCIE5\_1

**AMI Parameters**

Parameter list:

- Reserved\_Parameters
  - AMI\_Version
  - Init\_Returns\_Impulse
  - GetWave\_Exists
  - Max\_Init\_Aggressors
  - Tx\_Rj
  - Tx\_Dj
  - Tx\_DCD
- Model\_Specific
  - tx\_preset**

tx\_preset: Preset (User specified)

Use 'Set all data' setting

Parameter information: (Format List 0 1 2 3 4 5 6 7 8 9) (Default 4) (Description Tx EQ Prese)

Save Out/InOut parameters

**Additional Jitter**

Tx\_Sj

Tx\_Sj\_Frequency

Number of time points per UI:  Same as channelsim controller

Asynchronous clock: Clock offset (ppm)

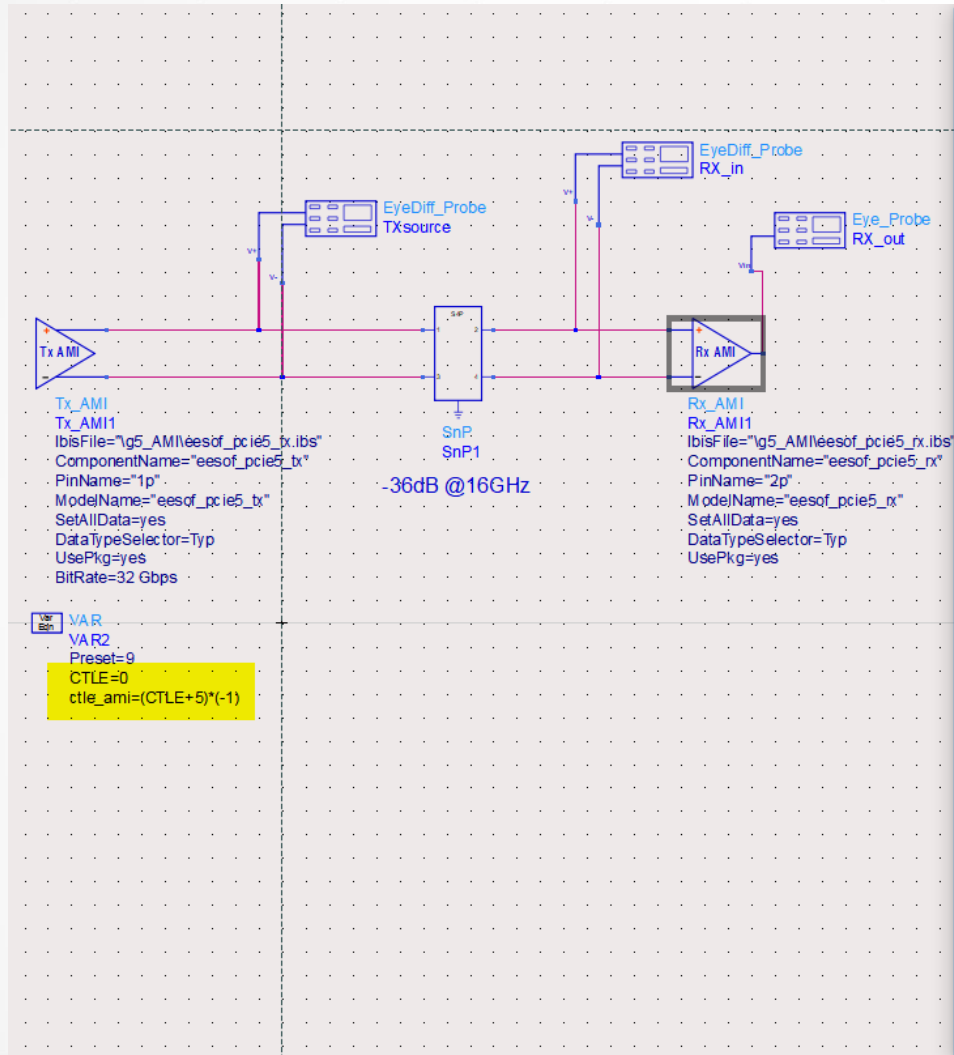
OK Apply Cancel Help



Tx\_AMI  
Tx\_AMI1  
IbisFile="g5\_AMI\eesof\_pcie5\_tx.ibs"  
ComponentName="eesof\_pcie5\_tx"  
PinName="1p"  
ModelName="eesof\_pcie5\_tx"  
SetAllData=yes  
DataTypeSelector=Typ  
UsePkg=yes  
BitRate=32 Gbps

VAR  
VAR2  
Preset=9  
CTLE=0  
ctle\_ami=(CTLE+5)\*(-1)

# Gen5 AMI Model (RX CTLE)



Rx AMI:5

Rx\_AMI Instance Name  
Rx\_AMI1

IBIS File: lg5\_AMI\eesof\_pcie5\_rx.ibs Select IBIS File... View...

Component: eesof\_pcie5\_rx

Set all data Typ Channel Index: 0

Use package Less

Package Pin Model I-V Data Driver Schedule SubModel Alias AMI Display

AMI file: C:\Demo\ADS\Application\Workshops\FY20Q2\_PCIE5\PCIE5\_ View

AMI Parameters

Parameter list

- Max\_Init\_Aggressors
- Ignore\_Bits
- Rx\_Rj
- Rx\_DJ
- Rx\_DCD
- Model\_Specific
  - rx\_ctle\_dcgain
  - rx\_dfe\_alpha
  - rx\_dfe\_tapfile
  - rx\_dfe\_tap1\_limit

rx\_ctle\_dcgain: ctle\_ami User specified

Use 'Set all data' setting

Parameter information

(Format: List -5 -6 -7 -8 -9 -10 -11 -12 -13 -14 -15) (Default -5) (Des

Save Out/InOut parameters

Additional Jitter

Rx\_Sj  
Rx\_Noise

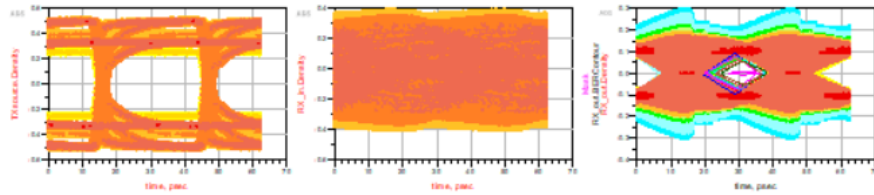
Number of time points per UI  
 Same as channelsim controller Number of time points per UI

Asynchronous dock  
Clock offset (ppm)

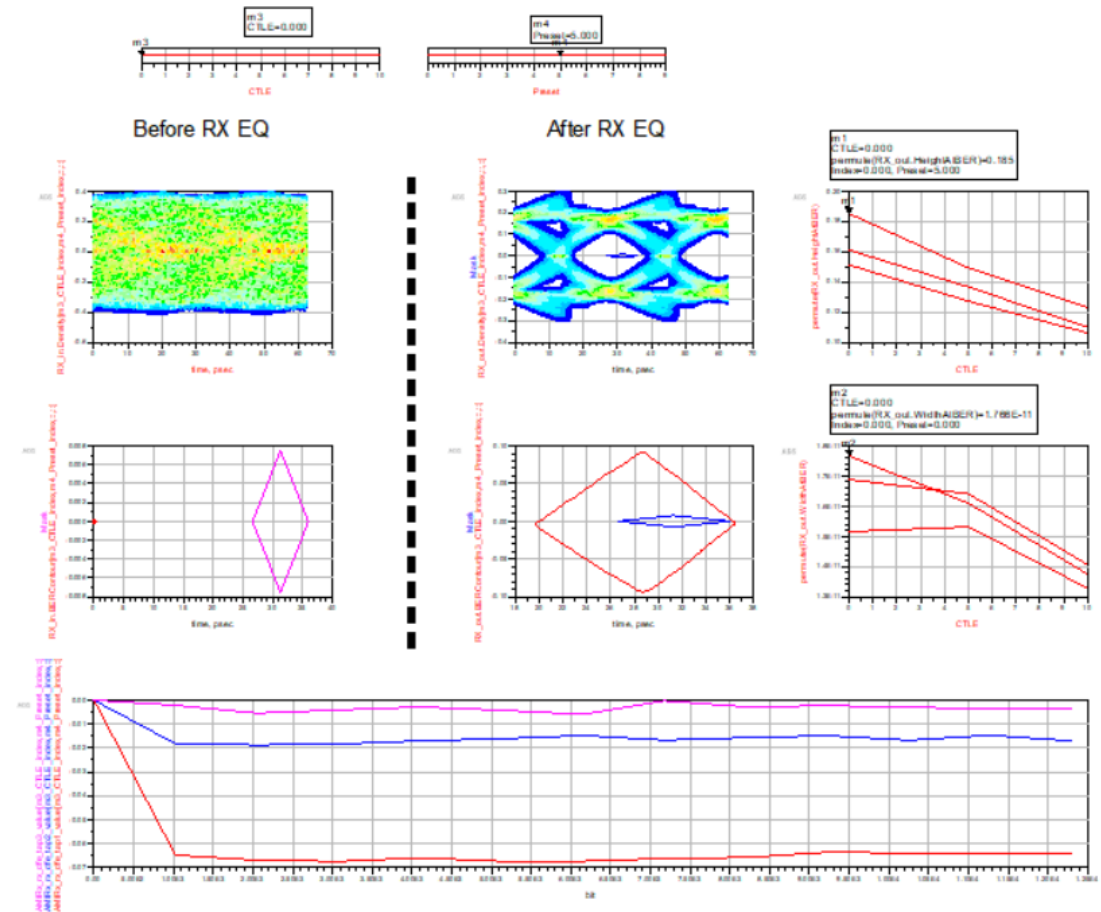
OK Apply Cancel Help

# Results (80s, 9 scenarios)

### ChannelSim Result

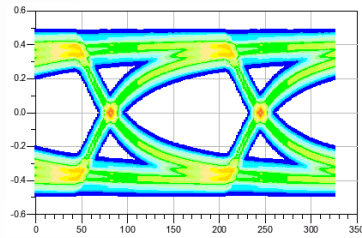
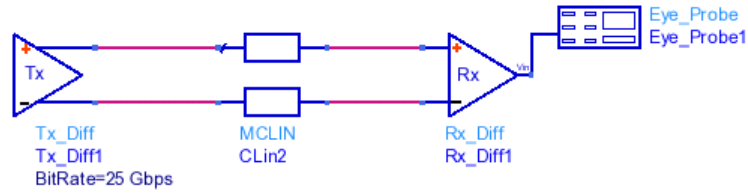


### Batched ChannelSim Result

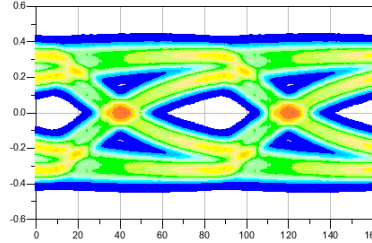


# Lab4 Repeater (Retimer/ Redriver) Usage

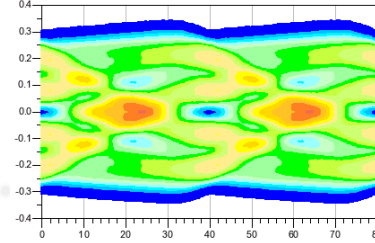
# What is Repeater



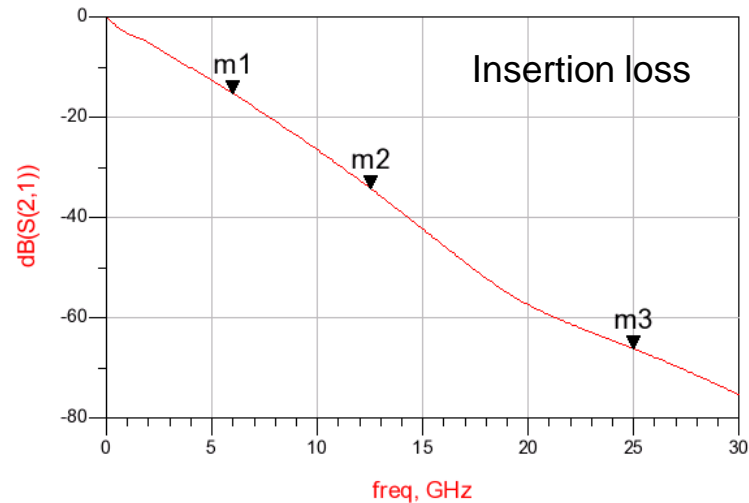
m1  
freq=6.000GHz  
dB(S(2,1))=-15.426



m2  
freq=12.50GHz  
dB(S(2,1))=-34.213

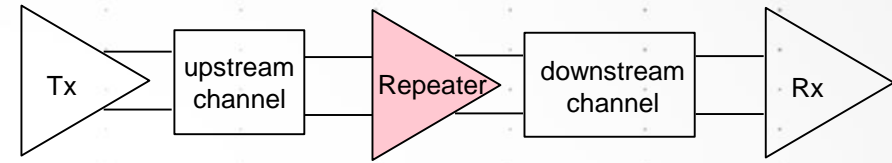


m3  
freq=25.00GHz  
dB(S(2,1))=-66.236



As data rate rises, channel loss increases, eye open decreases.

# What is Repeater

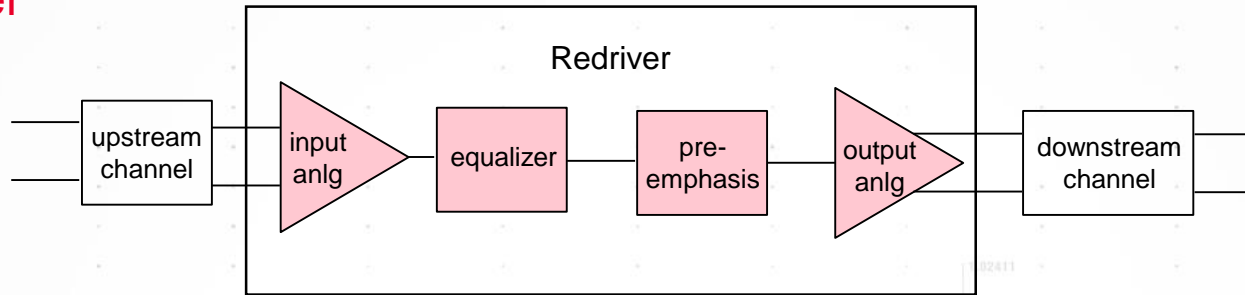


- Repeater is placed in the middle of a channel
- Equalizes incoming signal to compensate loss in upstream channel
- Retransmit signal into downstream channel and apply pre-emphasis
- Repeater is both Rx and Tx
- Two types of Repeater: Redriver and Retimer



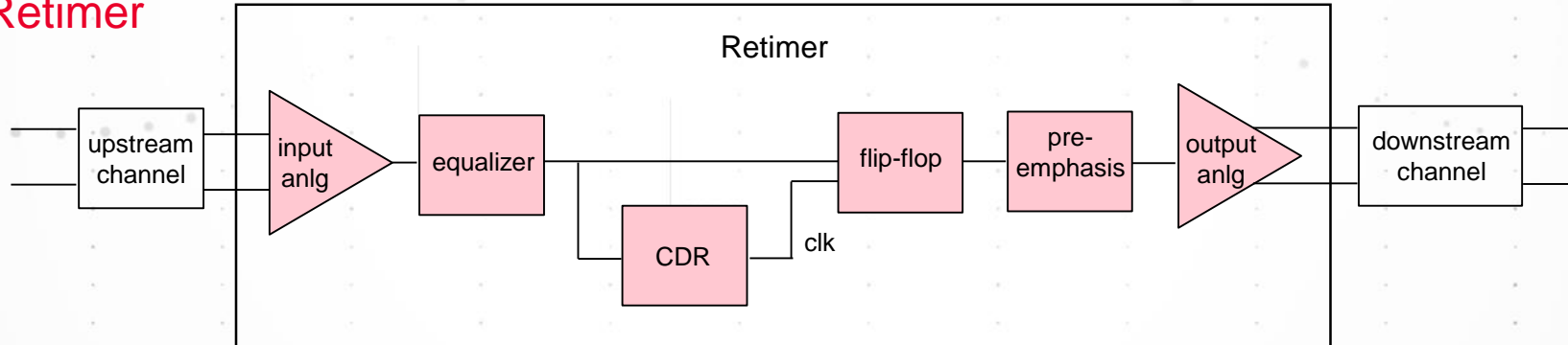
# What is Repeater

## Redriver



- Redriver output circuit is driven continuously by input signal
- No retiming is performed

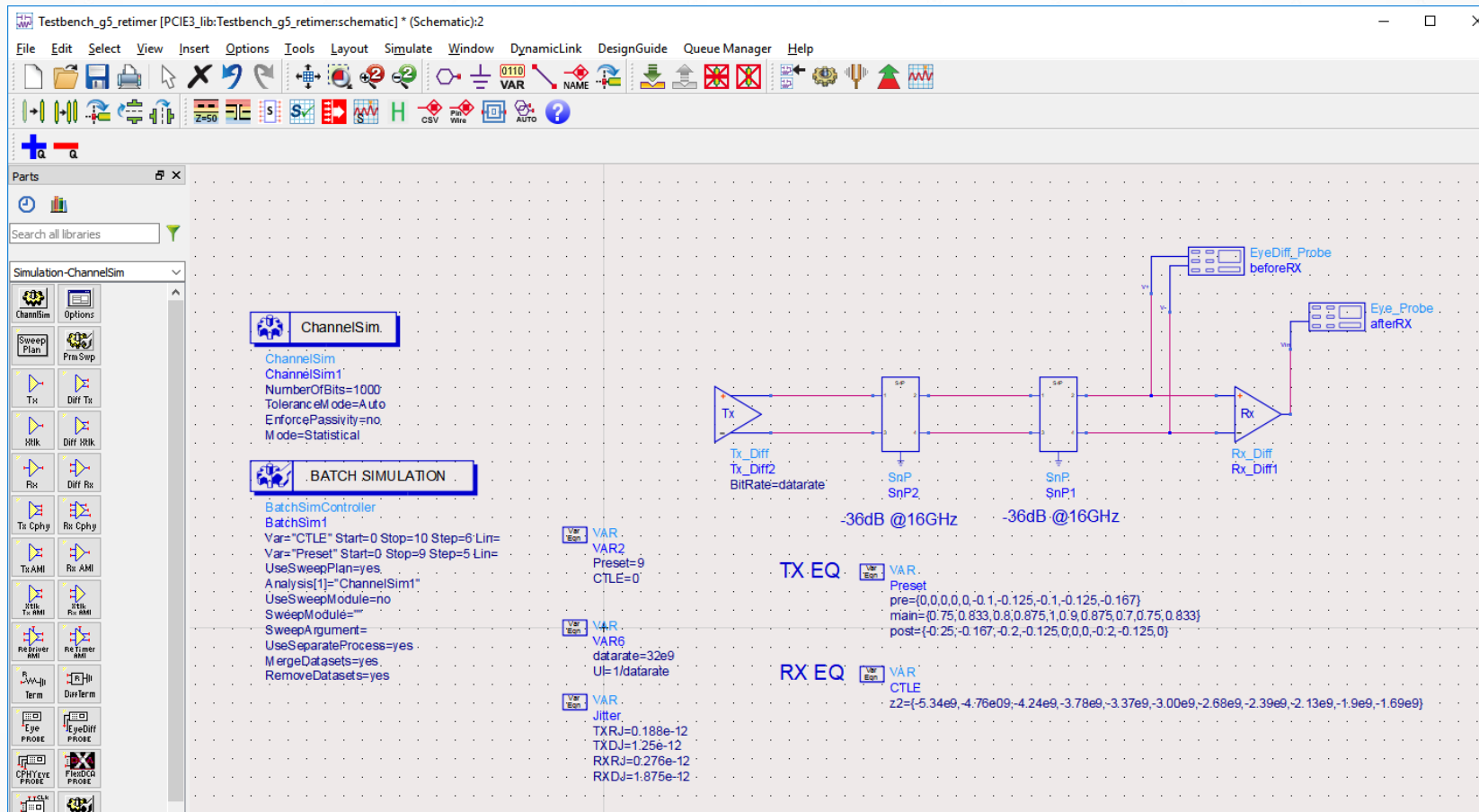
## Retimer



- Retimer output buffer is driven by switching events of flip-flop. Digital data is recovered.
- Clock-data recovery (CDR) retimes the output signal. Jitter in clock is passed down to downstream channel.

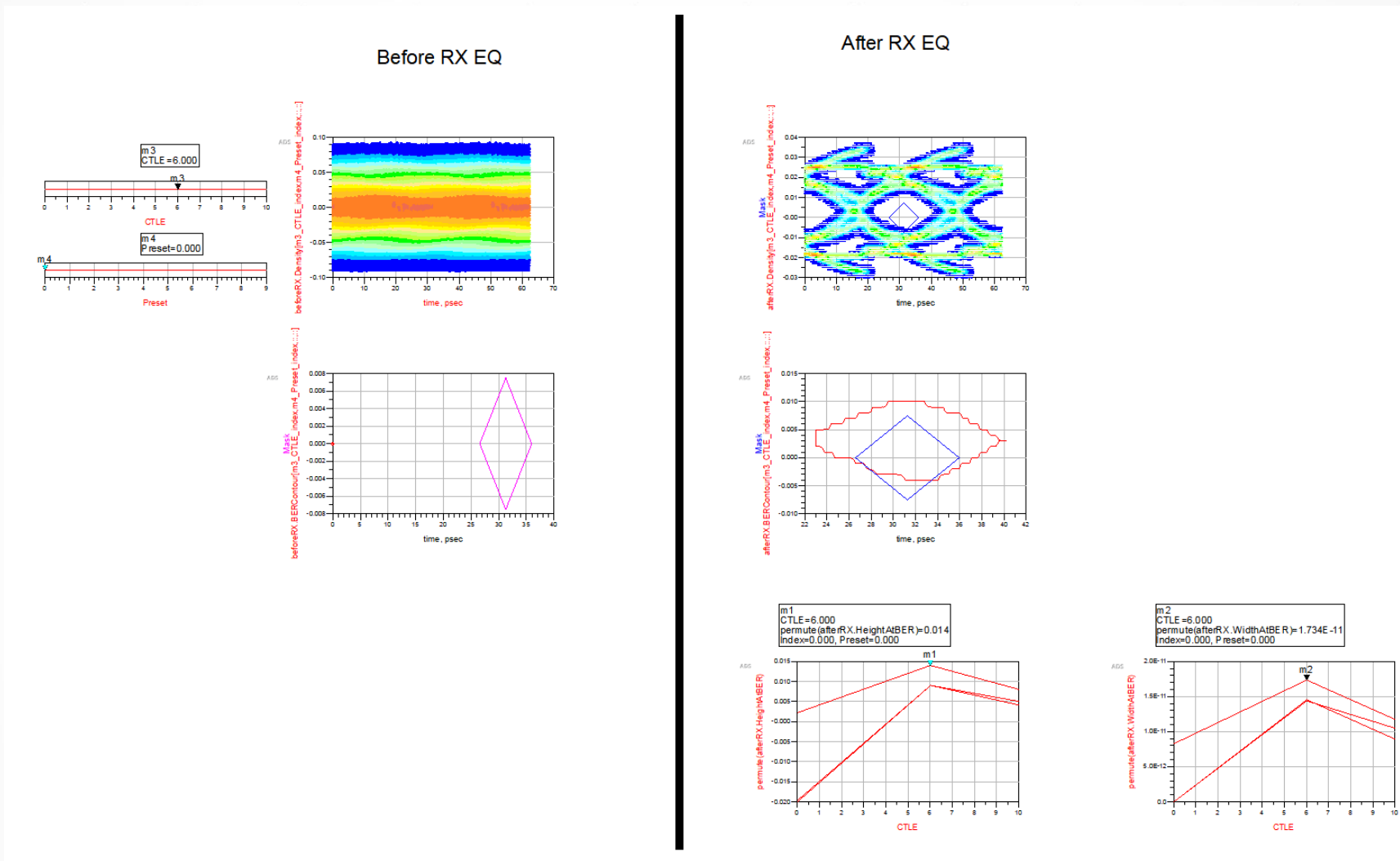
# Lab5 PCIe Gen5 Testbench with Retimer

# What if Longer Trace?



Try to maximize the EYE based on previous lab.

# What if Longer Trace?



# Add Retimer in the Middle

The screenshot displays the Advanced Design System (ADS) 2020 interface. The main window shows a schematic diagram titled "Testbench\_g5\_retimer [PCIe3\_lib:Testbench\_g5\_retimers:schematic] \* (Schematic):4". The schematic illustrates a signal path from a transmitter (Tx) through a channel to a receiver (Rx). A retimer block, labeled "Re Timer\_AM1", is inserted in the middle of the channel. The retimer block is highlighted in yellow. The schematic also shows various simulation parameters and variables.

**Channel Sim**

- ChannelSim
- ChannelSim1
- NumberOfBits=1000
- ToIeranceMode=Auto
- EntropyPassivity=no
- Mode=Bit-by-bit

**BATCH SIMULATION**

- Batch Sim Control
- Batch Sim 1
- Va ~ "CTLE" Start=0 Stop=10 Step=5 Lin
- Va ~ "Pre set" Start=0 Stop=9 Step=5 Lin
- Use Sweep Plan=yes
- Analysis[1] ~ "ChannelSim 1"
- Use Sweep Module=no
- Sweep Module=""
- Sweep Argument
- Use SeparateProcess=yes
- Merge Data sets=yes
- Remove Data sets=yes

**VAR**

- VAR2
- Pre set=9
- CTLE=0

**VAR**

- VAR6
- data rate=32 e9
- UI=1/data rate
- voltage Swing=0.8
- rise fall time=0.33 "UI"

**Jitter**

- TX RJ=0.188e-12
- TX DJ=1.25e-12
- RX RJ=0.276e-12
- RX DJ=1.875e-12

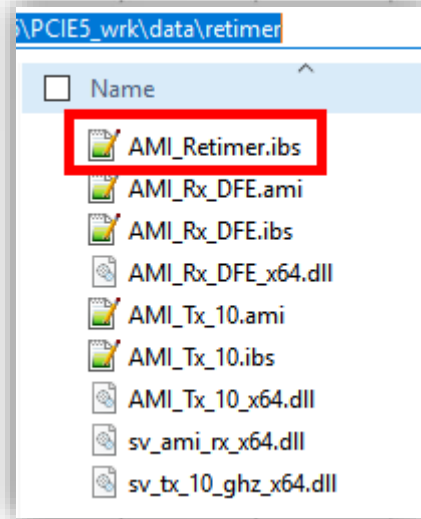
**TX EQ**

- VAR
- Pre set
- pre={0.0,0.0,0.0,-0.1,-0.125,-0.1,-0.125,-0.167}
- math={0.75,0.833,0.8,0.875,1.0,0.875,0.7,0.75,0.833}
- post={-0.25,-0.167,-0.2,-0.125,0.0,0,-0.2,-0.125,0}

**RX EQ**

- VAR
- CTLE
- z2={-5.34e9,-4.76e09,-4.24e9,-3.78e9,-3.37e9,-3.00e9,-2.68e9,-2.39e9,-2.13e9,-1.9e9,-1.69e9}

# Retimer Model

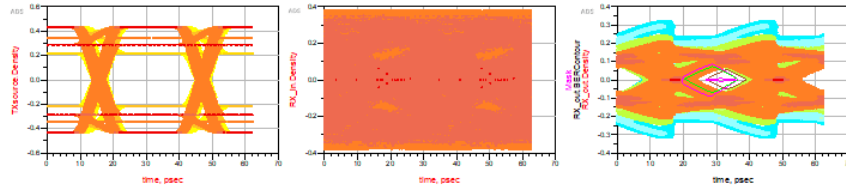


```
29 [Model] AMI_Rx_DFE
30 Model_type Input
31
32 C_comp 0p 0p 0p
33 Vinh = 0.25
34 Vinl = -0.25
35
36 [Temperature_Range] 25 125 0
37 [Voltage Range] 1.0 1.0 1.0
38
39 [Algorithmic Model]
40 Executable Windows_cl19.00.24215.1_64 AMI_Rx_DFE_x64.dll AMI_Rx_DFE.ami
41
```

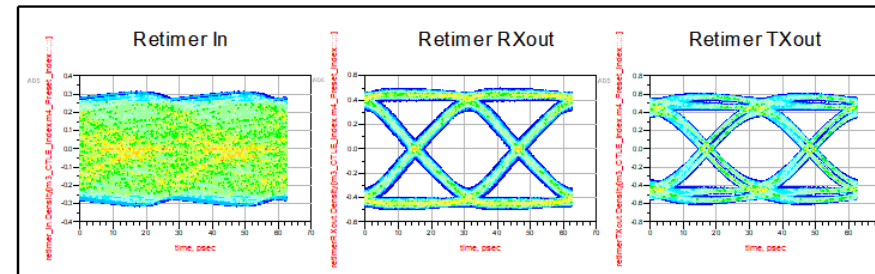
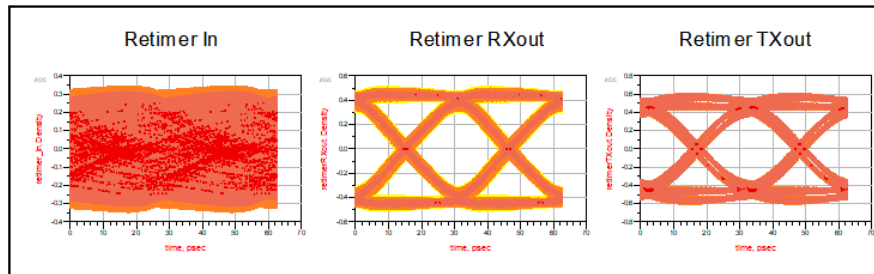
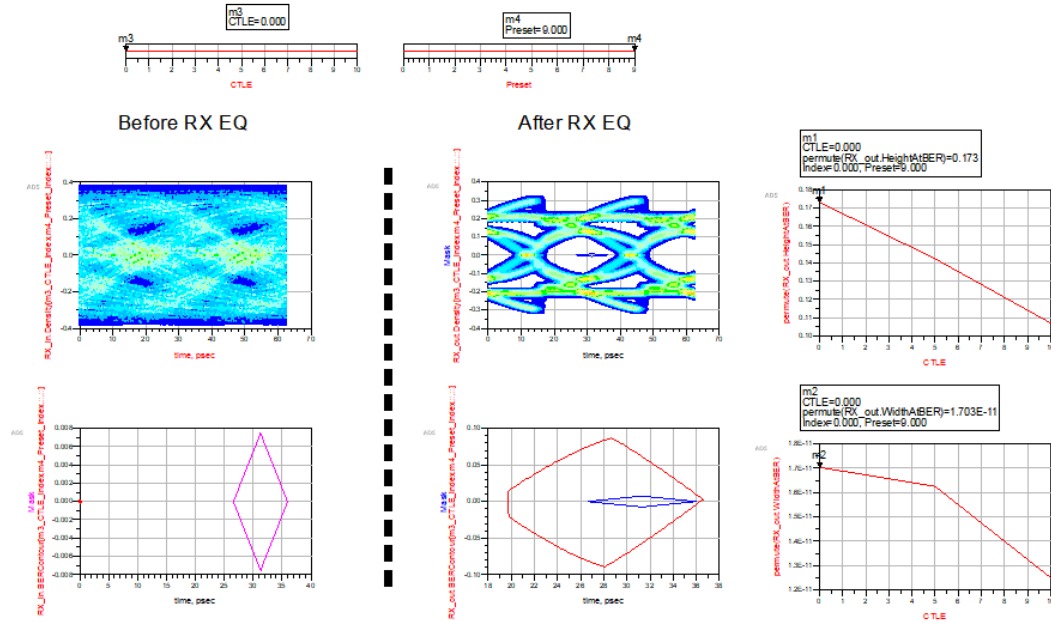
```
54 [Model] AMI_Tx_10
55 Model_type Output
56
57 C_comp 0p 0p 0p
58 Cref = 0
59 Vref = 0.5
60 Rref = 50
61 Vmeas = 0.5
62
63 [Temperature_Range] 25 125 0
64 [Voltage Range] 1.0 1.0 1.0
65
66 [Algorithmic Model]
67 Executable Windows_cl19.00.24215.1_64 AMI_Tx_10_x64.dll AMI_Tx_10.ami
68
```

# Results (200s, 9 scenarios)

ChannelSim Result



Batched ChannelSim Result





# Hand-made Retimer Model

# [Bonus] How to create Repeater.ibs File

1. Save Rx .ibs model as Repeater .ibs model
2. Change File name and Component name in .ibs file of repeater model
3. Copy Pin and Diff Pin definition from Tx .ibs model to Repeater .ibs model

```
[IBIS Ver]      5.1
[File Name]    AMI_Tx_10.ibs
[File Rev]     1.0
[Component]    AMI_Tx_10
[Manufacturer] My Company

[Package]

R_pkg 0.0  NA  NA
L_pkg 0.0  NA  NA
C_pkg 0.0  NA  NA

[Pin]  signal_name      model_name      R_pin L_pin  C_pin
lp     AMI_Tx_10_p      AMI_Tx_10
ln     AMI_Tx_10_n      AMI_Tx_10

[Diff_Pin] inv_pin vdiff tdelay_typ tdelay_min tdelay_max
lp         ln         NA      NA      NA      NA
```

**.ibs model of Tx**

```
[IBIS Ver]      5.1
[File Name]    AMI_Retimer.ibs
[File Rev]     1.0
[Component]    AMI_Retimer
[Manufacturer] My Company

[Package]

R_pkg 0.0  NA  NA
L_pkg 0.0  NA  NA
C_pkg 0.0  NA  NA

[Pin]  signal_name      model_name      R_pin L_pin  C_pin
2p     AMI_Rx_DFE_2p    AMI_Rx_DFE
2n     AMI_Rx_DFE_2n    AMI_Rx_DFE
lp     AMI_Tx_10_p      AMI_Tx_10
ln     AMI_Tx_10_n      AMI_Tx_10

[Diff_Pin] inv_pin vdiff tdelay_typ tdelay_min tdelay_max
2p         2n         NA      NA      NA      NA
lp         ln         NA      NA      NA      NA
```

**.ibs model of Redriver**

# [Bonus] How to create Repeater.ibs File

4. Copy the remaining Tx part to Redriver .ibs file **after definition of Rx** model and **before the '[END]'** command.

```
[Model] AMI_Tx_10
Model_type Output

C_comp 0p 0p 0p
Cref = 0
Vref = 0.5
Rref = 50
Vmeas = 0.5

[Temperature_Range] 25 125 0
[Voltage_Range] 1.0 1.0 1.0

[Algorithmic Model]
Executable Windows_c119.00.24215.1_64 AMI_Tx_10_x64.dll AMI_Tx_10.ami

[End Algorithmic Model]

[Pulldown]
-6.6      -0.132      -0.132      -0.132
0.0       0.0       0.0       0.0
6.6       0.132      0.132      0.132

[Pullup]
-6.6      0.132      0.132      0.132
0.0       0.0       0.0       0.0
6.6      -0.132     -0.132     -0.132

[GND Clamp]
-6.6      0.0       0.0       0.0
0.0       0.0       0.0       0.0
6.6       0.0       0.0       0.0

[Power Clamp]
-6.6      0.0       0.0       0.0
0.0       0.0       0.0       0.0
6.6       0.0       0.0       0.0

[Ramp]
dV/dt_r 0.3/1.5p 0.3/1.5p 0.3/1.5p
dV/dt_f 0.3/1.5p 0.3/1.5p 0.3/1.5p

[END]
```

**.ibs model of Tx**

```
-6.6      0.132e-9      0.0       0.0
0.0       0.0       0.0       0.0
6.6      -0.132e-9     0.0       0.0

[Model] AMI_Tx_10
Model_type Output

C_comp 0p 0p 0p
Cref = 0
Vref = 0.5
Rref = 50
Vmeas = 0.5

[Temperature_Range] 25 125 0
[Voltage_Range] 1.0 1.0 1.0

[Algorithmic Model]
Executable Windows_c119.00.24215.1_64 AMI_Tx_10_x64.dll AMI_Tx_10.ami

[End Algorithmic Model]

[Pulldown]
-6.6      -0.132      -0.132      -0.132
0.0       0.0       0.0       0.0
6.6       0.132      0.132      0.132

[Pullup]
-6.6      0.132      0.132      0.132
0.0       0.0       0.0       0.0
6.6      -0.132     -0.132     -0.132

[GND Clamp]
-6.6      0.0       0.0       0.0
0.0       0.0       0.0       0.0
6.6       0.0       0.0       0.0

[Power Clamp]
-6.6      0.0       0.0       0.0
0.0       0.0       0.0       0.0
6.6       0.0       0.0       0.0

[Ramp]
dV/dt_r 0.3/1.5p 0.3/1.5p 0.3/1.5p
dV/dt_f 0.3/1.5p 0.3/1.5p 0.3/1.5p

[END]
```

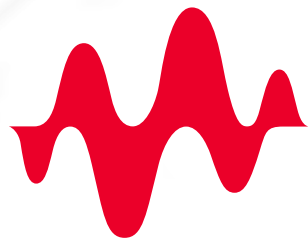
**.ibs model of Redriver**

# Summary

- ADS provides a platform to validate your PCIe Gen5 design, and it can be done by
  - Implementing JEDEC PCIe Gen5 specification by ADS generic TX/RX model.
  - Simply using Gen5 AMI models provided by Keysight.
- Repeater will be widely used in PCIe Gen5 and beyond to make impossible possible.
- Batch Simulator can help gain insight among your system configurations.

# Reference

- <https://community.keysight.com/thread/27162>
- [https://www.keysight.com/upload/cmc\\_upload/All/PCI-Express5-Specification-and-latest-information-of-Gen4-testing.pdf?fbclid=IwAR3OtS4q7yPt7mnj2SuXq7mBc4OmK1AMhIM1py19pAQyIGJXFWCg9\\_jN-FU](https://www.keysight.com/upload/cmc_upload/All/PCI-Express5-Specification-and-latest-information-of-Gen4-testing.pdf?fbclid=IwAR3OtS4q7yPt7mnj2SuXq7mBc4OmK1AMhIM1py19pAQyIGJXFWCg9_jN-FU)
- <https://www.keysight.com/sg/en/assets/7018-03143/application-notes/5990-9111.pdf?success=true>



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