From Simulation to Test
Be Ready for PCIe Gen5 Design Challenge

TU Nash

Application Engineer

2019.3.12

KEYSIGHT TECHNOLOGIES

Outline

- PCIe Gen5 Testing Solution and Challenge
- Lab1: ADS Channel Simulator Overview
- Lab2: PCIE Gen5 Overview
  - CTLE
  - DFE
  - Channel Tolerance
  - Jitter
  - EYE
- Lab3: PCIe Gen5 Testbench
- Lab4: Repeater (Retimer/ Redriver) Usage
- Lab5: PCIe Gen5 Testbench with Retimer
- Summary

Hot Keys – Schematic

Edit Commands

Following table lists the hot keys for the Edit menu options.

Menu Name	Default
Edit > Copy	Ctrl+C
Edit > Copy/Paste > Copy Using Reference	C
Edit > Cut	Ctrl+X
Edit > Delete	Del
Edit > End Command	Esc
Edit > Mirror About X	Shift+X
Edit > Mirror About Y	Shift+Y
Edit > Move > Move Component Text	F5
Edit > Move > Move Edge	
Edit > Move > Move Using Reference	M
Edit > Move > Move Wire Endpoint	Ctrl+Shift+M
Edit > Paste	Ctrl+V
Edit > Redo	Ctrl+Y
Edit > Rotate	Ctrl+R
Edit > Undo	Ctrl+Z

View Commands

Following table lists the hot keys for the View menu options.

Menu Name	Default
View > Clear Highlighting	F8
View > Command Quick Help	Shift+F1
View > Grid Display	Ctrl+G
View > Origin Crosshair	Shift+O
View > Pan View	Tab
View > Pop Out Of Hierarchy	B
View > Push Into Hierarchy	Shift+E
View > Restore Last View	Ctrl+L
View > View All	F
View > Zoom > Zoom Area	
View > Zoom > Zoom By Factor > Zoom In x2	+
View > Zoom > Zoom By Factor > Zoom Out x2	-
View > Zoom > Zoom To Selected	Z

Insert Commands

Following table lists the hot keys for the Insert menu options.

Menu Name	Default
Insert > Change Entry Layer To	Ctrl+Shift+C
Insert > Component > Component Library...	I
Insert > Measure...	Ctrl+M
Insert > Shape > Polygon	Shift+P
Insert > Shape > Rectangle	R
Insert > Shape > Undo Vertex	Backspace
Insert > Text	Ctrl+T
Insert > Wire	Ctrl+W

Window and Miscellaneous Cor

Following table lists the hot keys for the Window and Miscellaneous

Menu Name	Default
Window > Close	Ctrl+F4
Window > Layout	Ctrl+Shift+L
Window > Open Another Schematic Window	Ctrl+Shift+S
Help > Topics and Index	F1
Options > Snap Enabled	Ctrl+E
Select > Select All	Ctrl+A
Simulate > Simulate	F7

- Help > F1

Hot Keys – Data Display

File Command

Following table lists the File m

Menu Name	Default
File > New	Ctrl+N
File > Open...	Ctrl+O
File > Print...	Ctrl+P
File > Save	Ctrl+S

Edit Commands

Following table lists the Edit menu cor

Menu Name	Default
Edit > Copy	Ctrl+C
Edit > Cut	Ctrl+X
Edit > Delete	Del
Edit > End Command	Esc
Edit > Paste	Ctrl+V
Edit > Redo	Ctrl+Y
Edit > Select All	Ctrl+A
Edit > Undo	Ctrl+Z

View Commands

Following table lists the View menu command

Menu Name	Default
View > Grid Display	Ctrl+G
View > Restore Last View	Ctrl+L
View > View All	F
View > Zoom > Zoom Area	
View > Zoom > Zoom In x2	+
View > Zoom > Zoom Out x2	-

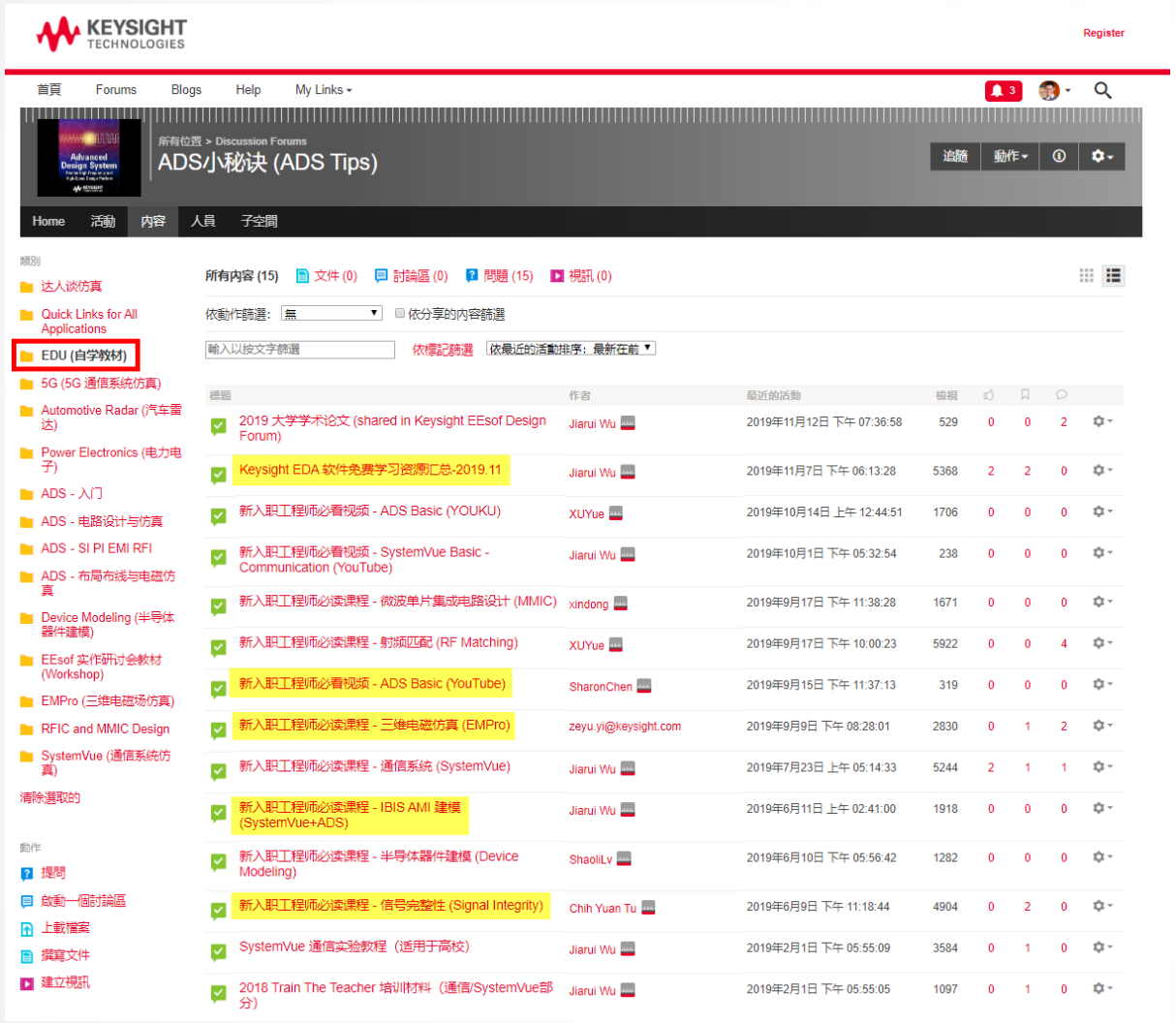
Miscellaneous Commands

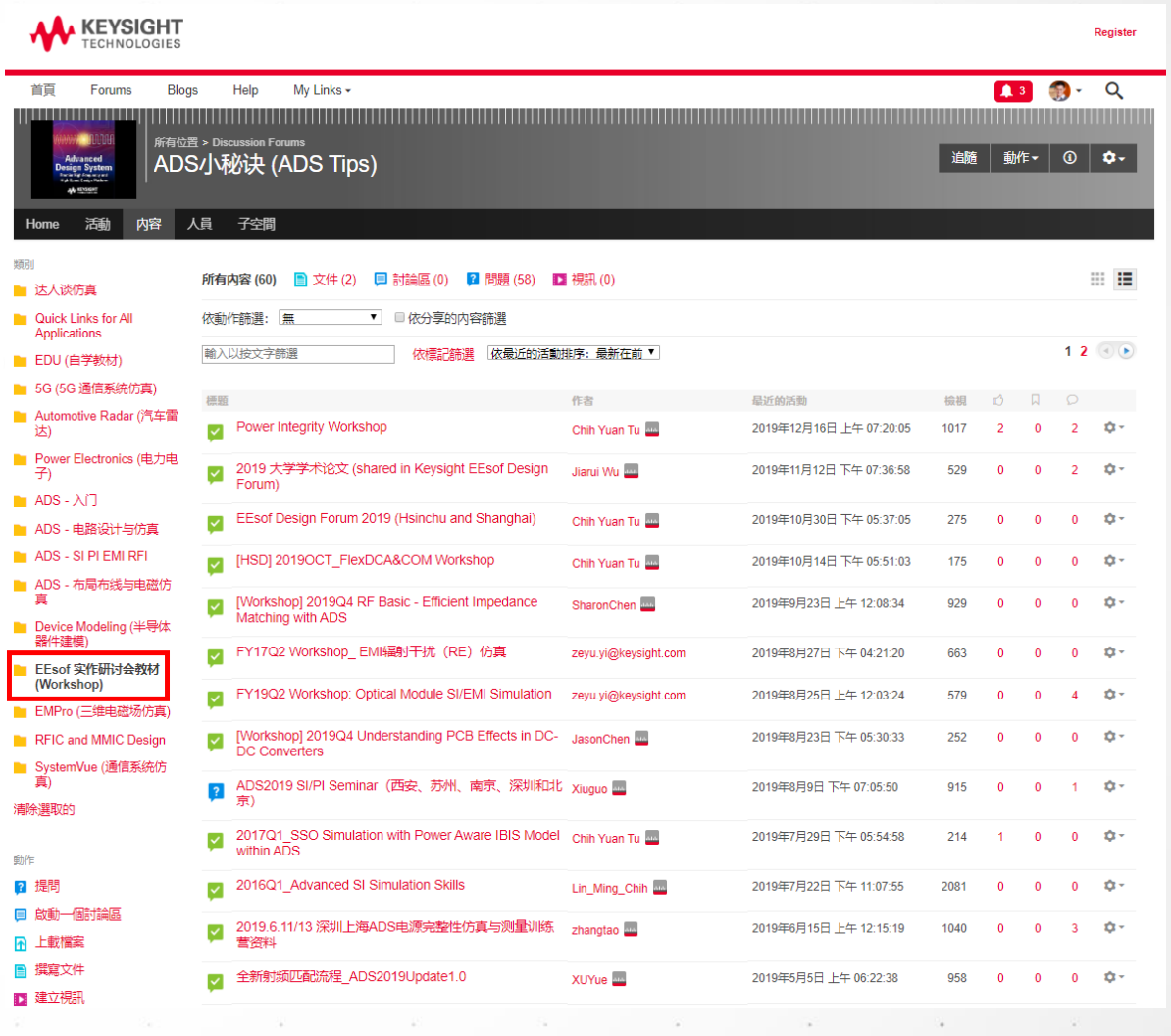
Following table lists the various other menu commands su

Menu Name	Default
Help > Topics and Index	F1
Marker > New...	Ctrl+M
Options > Hide ADS Logo on all plots	Alt+L
Options > Snap Enabled	Ctrl+E
Window > Close	Ctrl+F4
Window > New	Ctrl+Shift+D

- Help > F1

ADS Tips Forum (ADS小秘訣) www.keysight.com/find/ADS_tips





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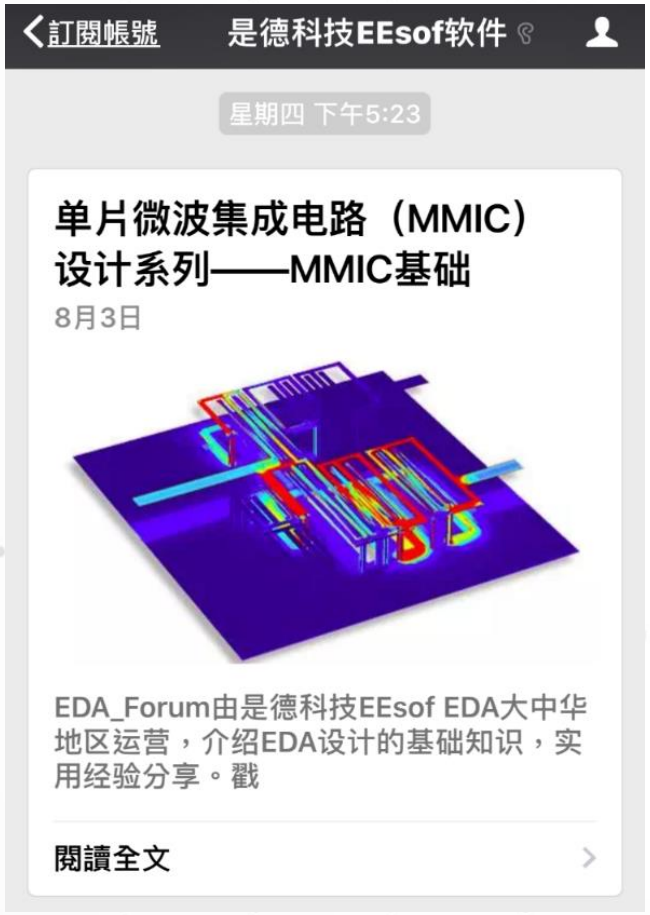

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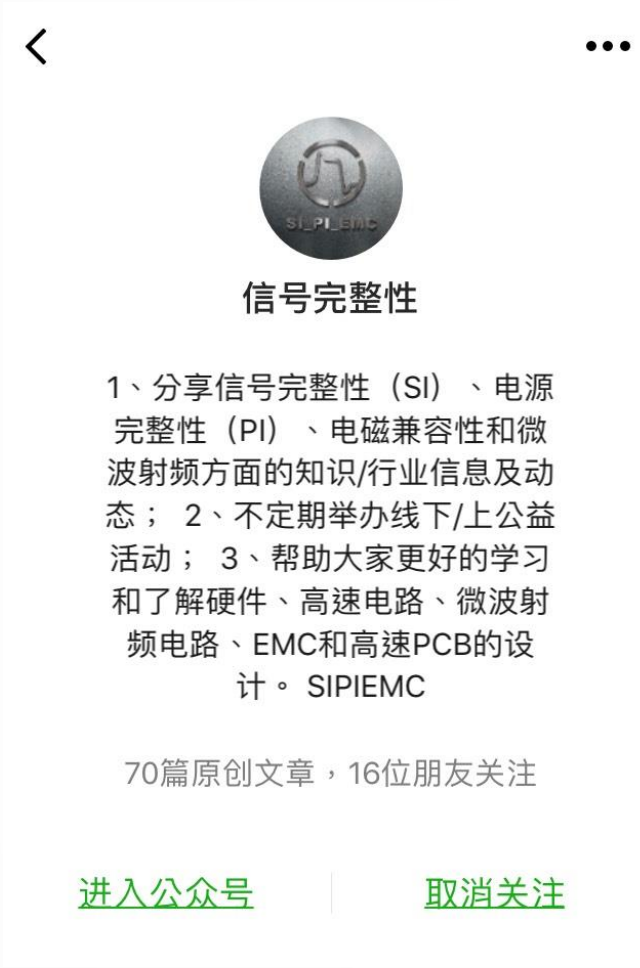

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輕鬆談電路模擬 https://ezsimulation.blogspot.com/

輕鬆談電路模擬

2019年12月17日 星期二

減少去耦合電容的數量

PCB電源平面上常並聯很多顆去耦合電容，用來抑制電源分配網路的阻抗。這些去耦合電容最早可能是出現在IC設計公司提供的公板。系統廠會依據需求修改公板，但多不會、也不敢拿掉去耦電容。但每一顆電容都關係生產成本，研發能減少一顆電容，就能為公司減少一顆電容的成本。所以，減少PCB上去耦合電容是研發直接貢獻公司利潤的機會。

要減少去耦合電容的數量，先要找出沒有在工作的電容。以是德科技的ADS為例，ADS中的PIPro可以抽取PCB電源平面的S參數。將電源平面的S參數連上去耦合電容，可以算出電源分配網路的阻抗，也能看出每一顆電容有多少電流流過。沒有電流流過，或電流量極小的電容，都是可以去除的目標電容。去掉這些電容，再次檢查電源分配網路的阻抗，如果還能確定符合IC設計公司提供的限制線的要求，那就對了。

於 12月 17, 2019　沒有留言:

標籤： Power Integrity

關於我自己

tonychen.tau

Tony Chen 目前任职于是德科技，为EDA软件业务处大中国区应用工程部经理。

檢視我的完整簡介

網誌存檔

▼ 2019 (48)

▼ 十二月 (11)

減少去耦合電容的數量

跑完模擬以後，怎麼能知道模擬的結果準不準呢？

實際案例：傳輸線模擬的結果與測試結果不同

公司應該善待模擬工程師

Dear Tony, 我適合應用工程師的工作嗎？

做完模擬，要有模擬結果報告

PCIe Gen5 Testing Solution and Challenge

Keysight PCIe Gen5 Application solution

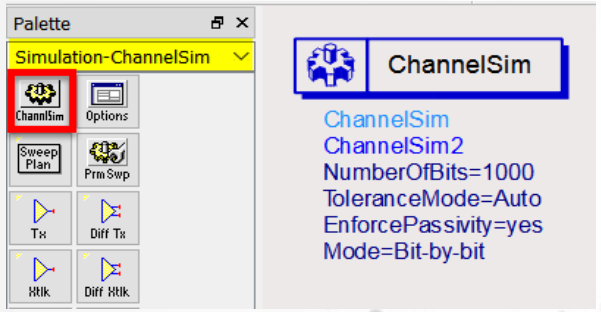
Jacky Yu

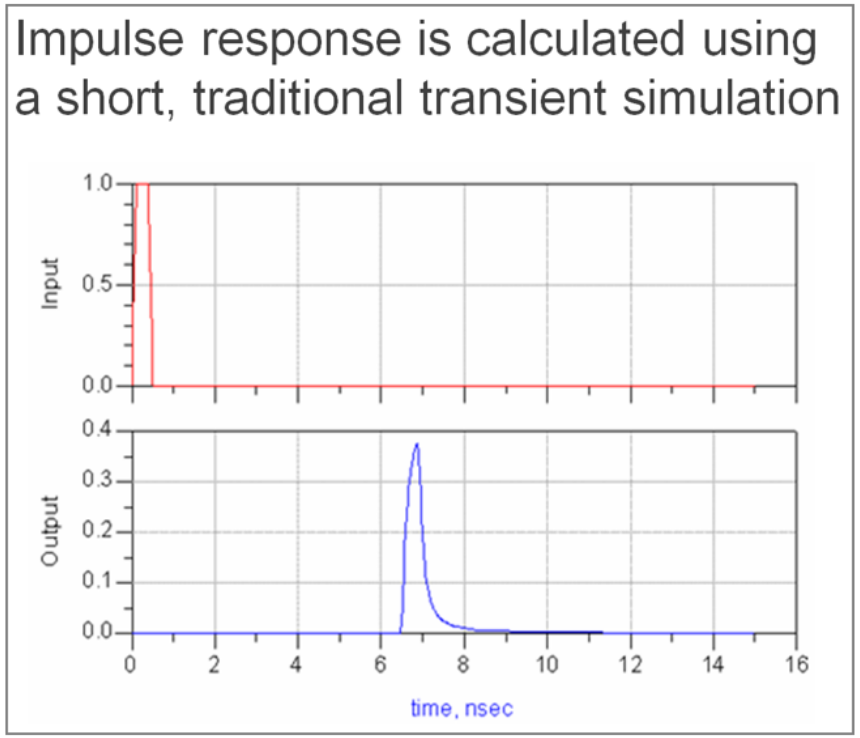
2020.MARCH

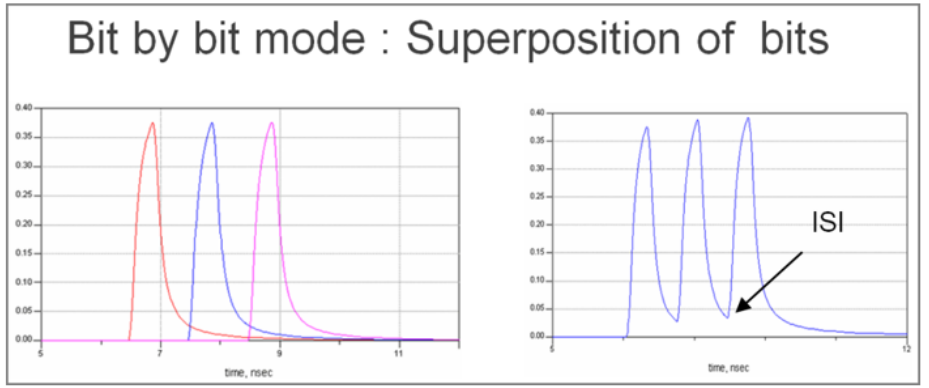
Keysight Taiwan Technologies

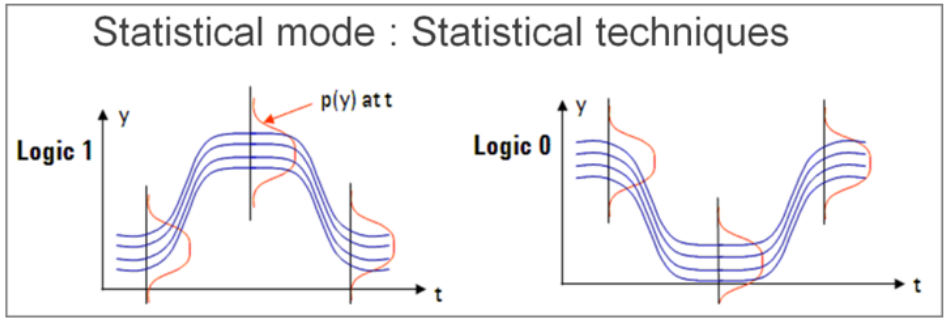
Lab1 ADS Channel Simulator Overview

Channel Simulator Methodology









Comparison of Simulation Techniques

	Netlists & IBIS traditional flow	IBIS AMI flow: Bit-by-bit ("time-domain") mode	IBIS AMI flow: Statistical mode
Method	Computational expensive: Modified nodal analysis of Kirchoff's current laws	Bit-by-bit superposition of impulse responses	Statistical calculations based on impulse response
BER floor 1 minute	~10^{-3}	~10^{-6}	~10^{-18} or lower
Applicability & Restrictions	NLTV analog & channel NLTV Tx/Rx	LTI analog & channel* *SystemVue and ADS can handle NLTV mid-channel repeaters as specified in IBIS 6.0 NLTV Tx/Rx	LTI analog & channel LTI Tx/Rx

IBIS-AMI Introduction

- I/O Buffer Information Specification (IBIS)
- Algorithmic Model Interface (AMI)

Two Kinds of AMI Model

Two Kinds of Tx/Rx Plus a "Dual" or "Hybrid" model		Model's Init_Returns_Impulse flag is:	
		False ("Can't be modeled as LTI")	True ("LTI model via impulse response")
Model's GetWave_ Exists flag is	False ("Model is pure LTI")	Empty model: not allowed	Typical case for Tx and simple Rx's (fixed Eq. and no CDR)
	True ("NLTV model via waveform modification")	Typical case for Rx (Adaptive Eq., CDR)	Buyer beware: LTI approximation of NLTV device if used in stat mode

Table 1. Two kinds of AMI model, plus a "hybrid"

Statistical Mode

		Tx model's Init_Returns_Impulse flag is	
		False ("Tx cannot be modeled nor approxi-mated as LTI")	True ("Tx can be modeled as LTI using AMI_Init()")
Rx model's Init_ Returns_ Impulse flag is	False ("Rx cannot be modeled nor approximated as LTI")	Not recommended. ChanSim issues warning	Not recommended. ChanSim issues warning
	True ("Rx can be modeled as LTI using AMI_Init()")	Not recommended. ChanSim issues warning.	"Case 1"

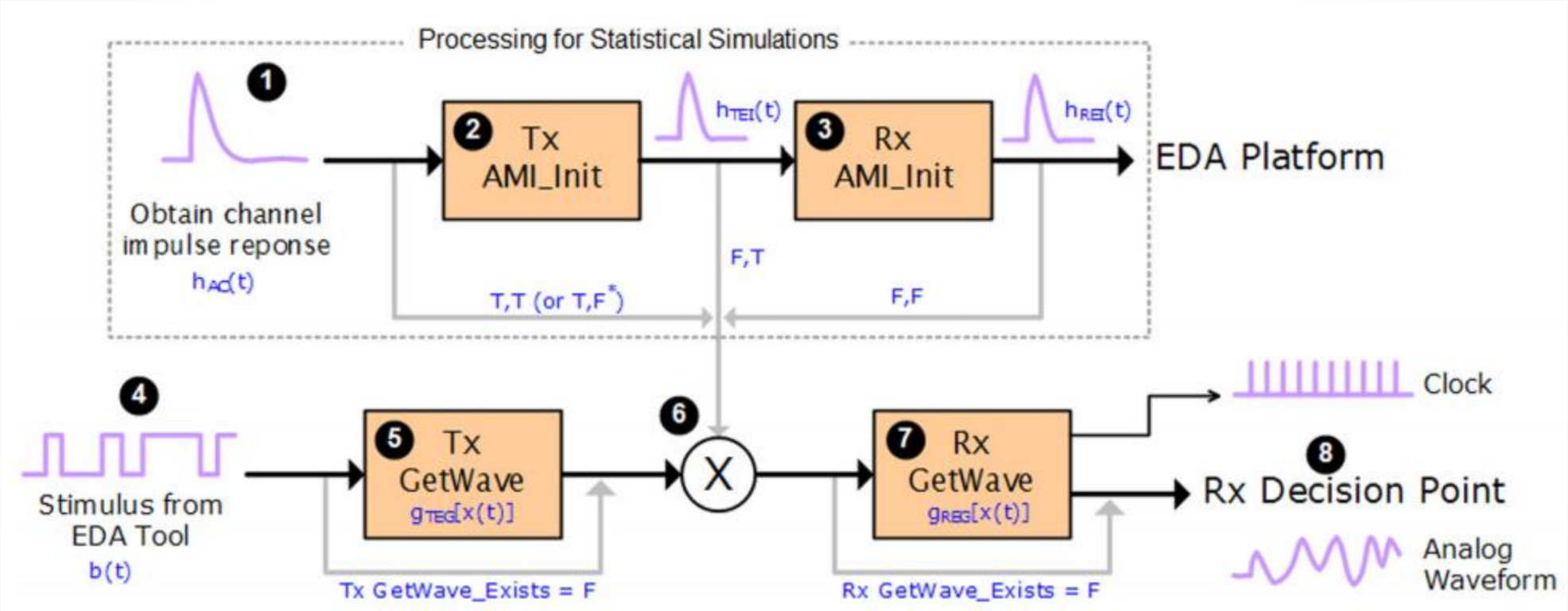
Table 2a. Channel Simulator set to statistical mode

Bit-By-Bit Mode

		Tx model's GetWave_Exists flag is	
		False ("Tx does not have AMI_GetWave()")	True ("Tx has AMI_GetWave())
Rx model's GetWave_Exists flag is	False ("Rx does not have AMI_GetWave()")	"Case 2"	"Case 5" (Practically never used)
	True ("Rx has AMI_GetWave()")	"Case 3" (Most common case)	"Case 4"

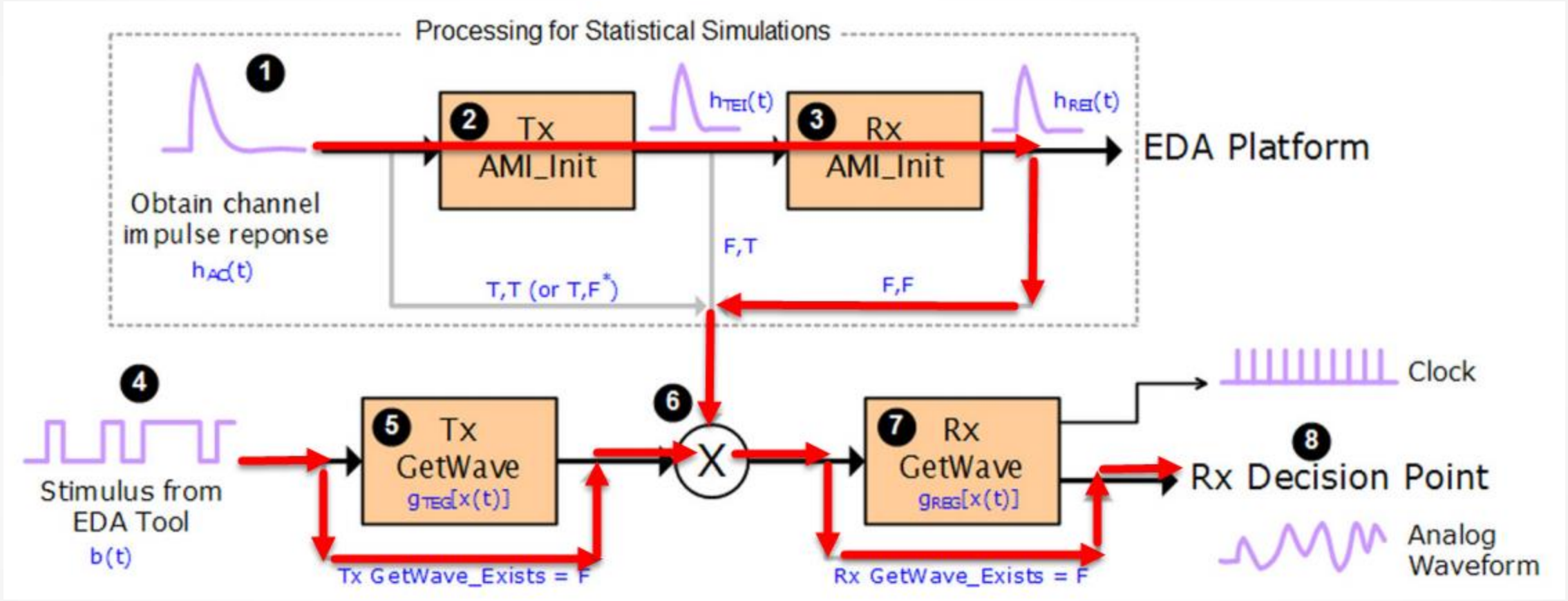
Table 2b. Channel simulator set to bit-by-bit mode. (Note: In IBIS 5.0, there was a third flag ("Use_Init_Output") besides the present Init_Returns_Impulse and GetWave_Exists flags. However, this flag caused much confusion and so Use_Init_Output is deprecated in IBIS 5.1.)

AMI Simulation Flow

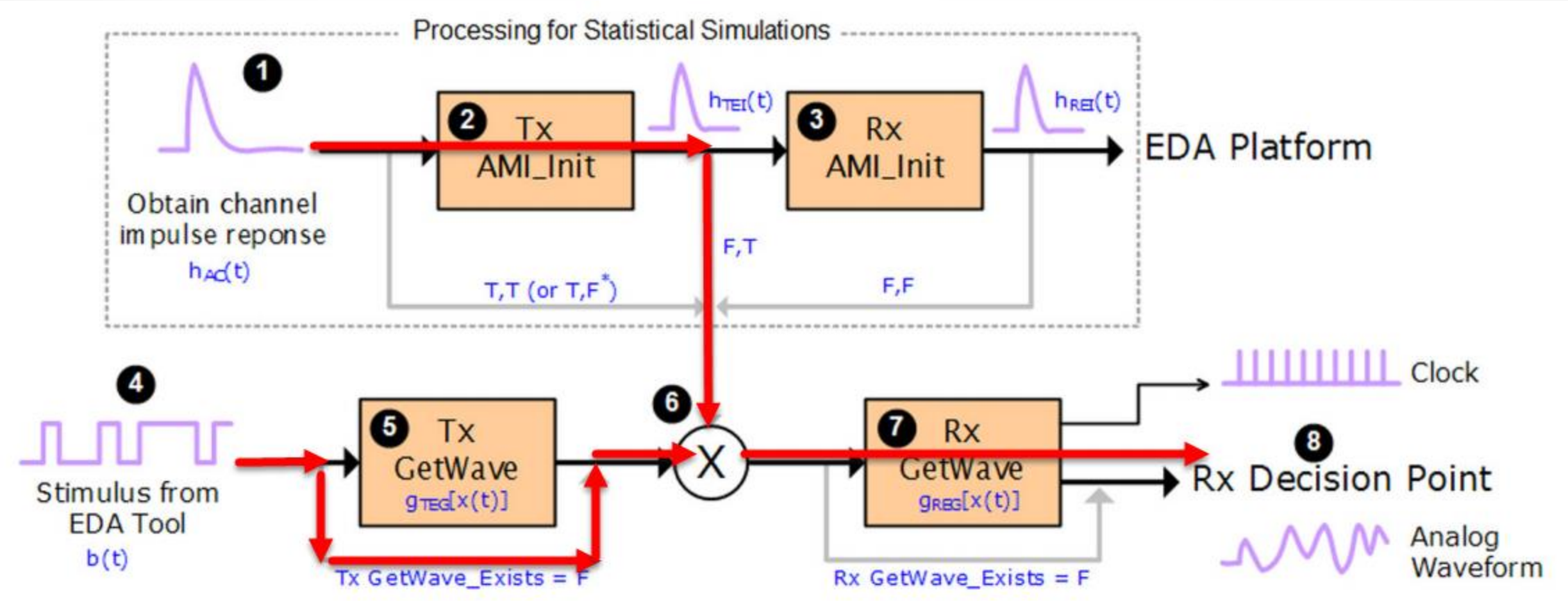


https://www.keysight.com/sg/en/assets/7018-03143/application-notes/5990-9111.pdf?success=true

Statistical (TX Init, RX Init)



Bit-by-bit (TX Init, RX GetWave)

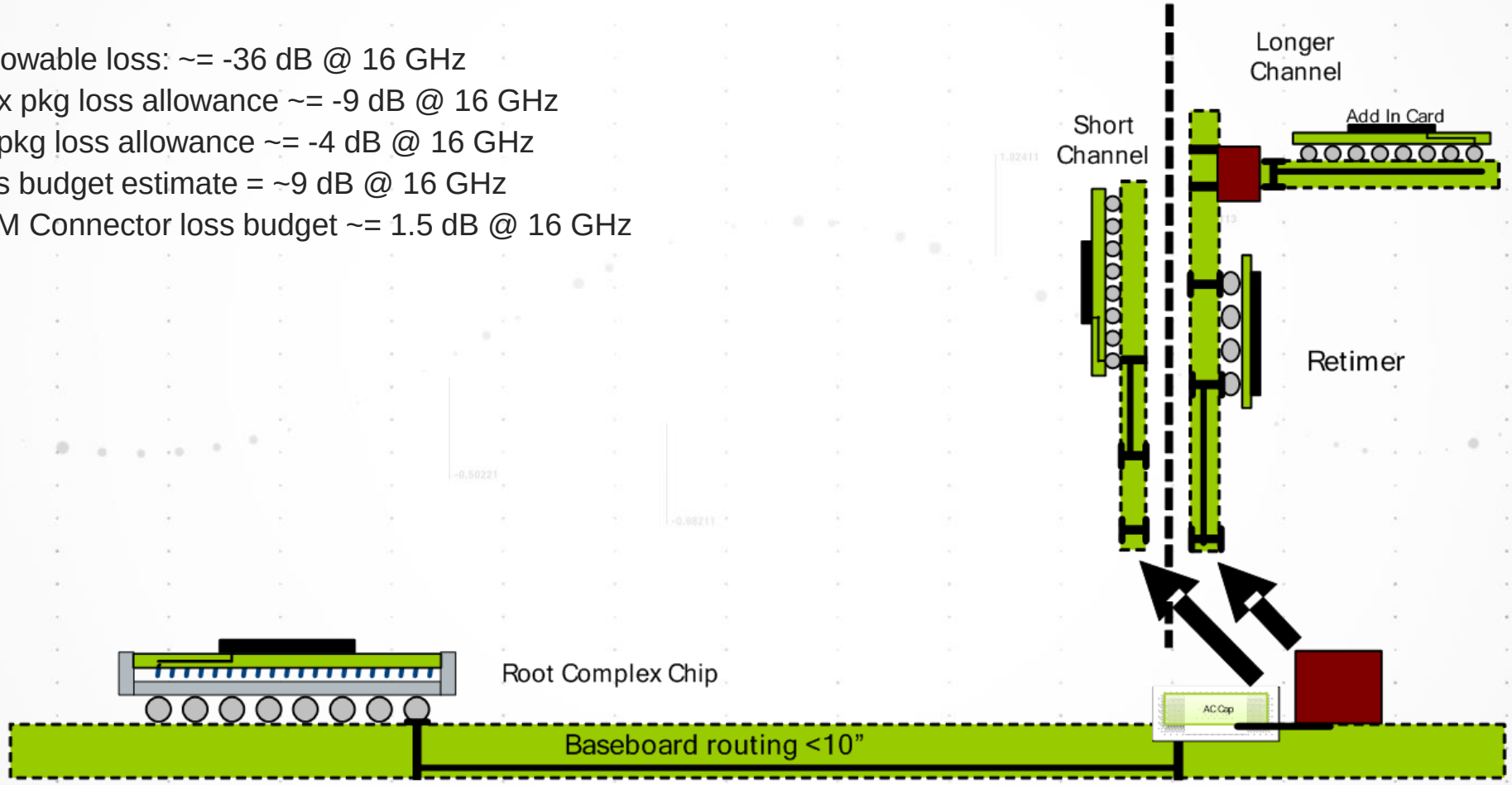


Lab2 PCIe Gen5 Overview

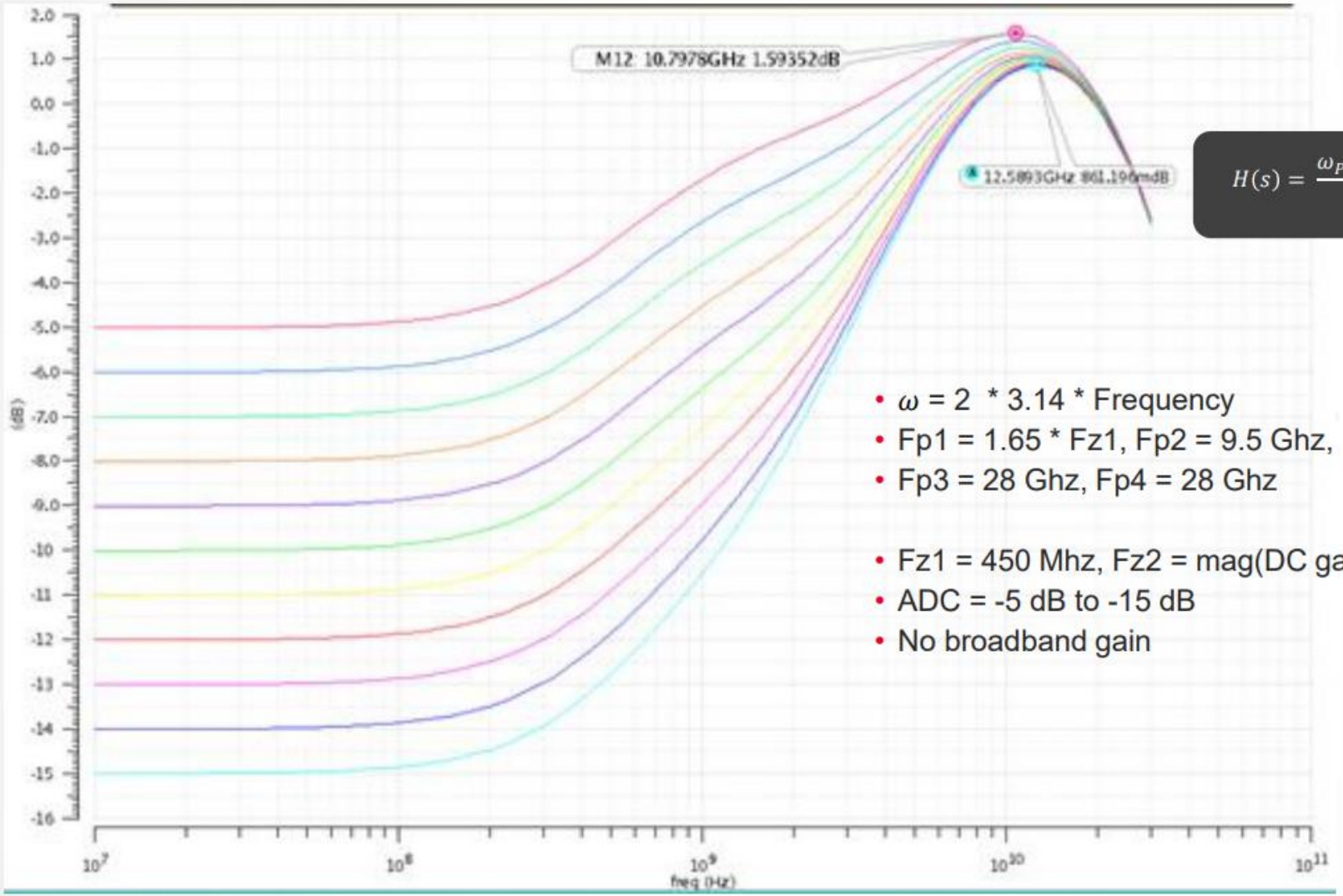
PCI Express 5.0 Channel Topology

RETIMER REQUIRED WHEN LOSS EXCEEDS -36 DB OR >1 CONNECTOR

- Estimated allowable loss: ~= -36 dB @ 16 GHz
- Root complex pkg loss allowance ~= -9 dB @ 16 GHz
- Add-in Card pkg loss allowance ~= -4 dB @ 16 GHz
- Total AIC loss budget estimate = ~9 dB @ 16 GHz
- PCIe 5.0 CEM Connector loss budget ~= 1.5 dB @ 16 GHz



CTLE (-5 to -15dB)

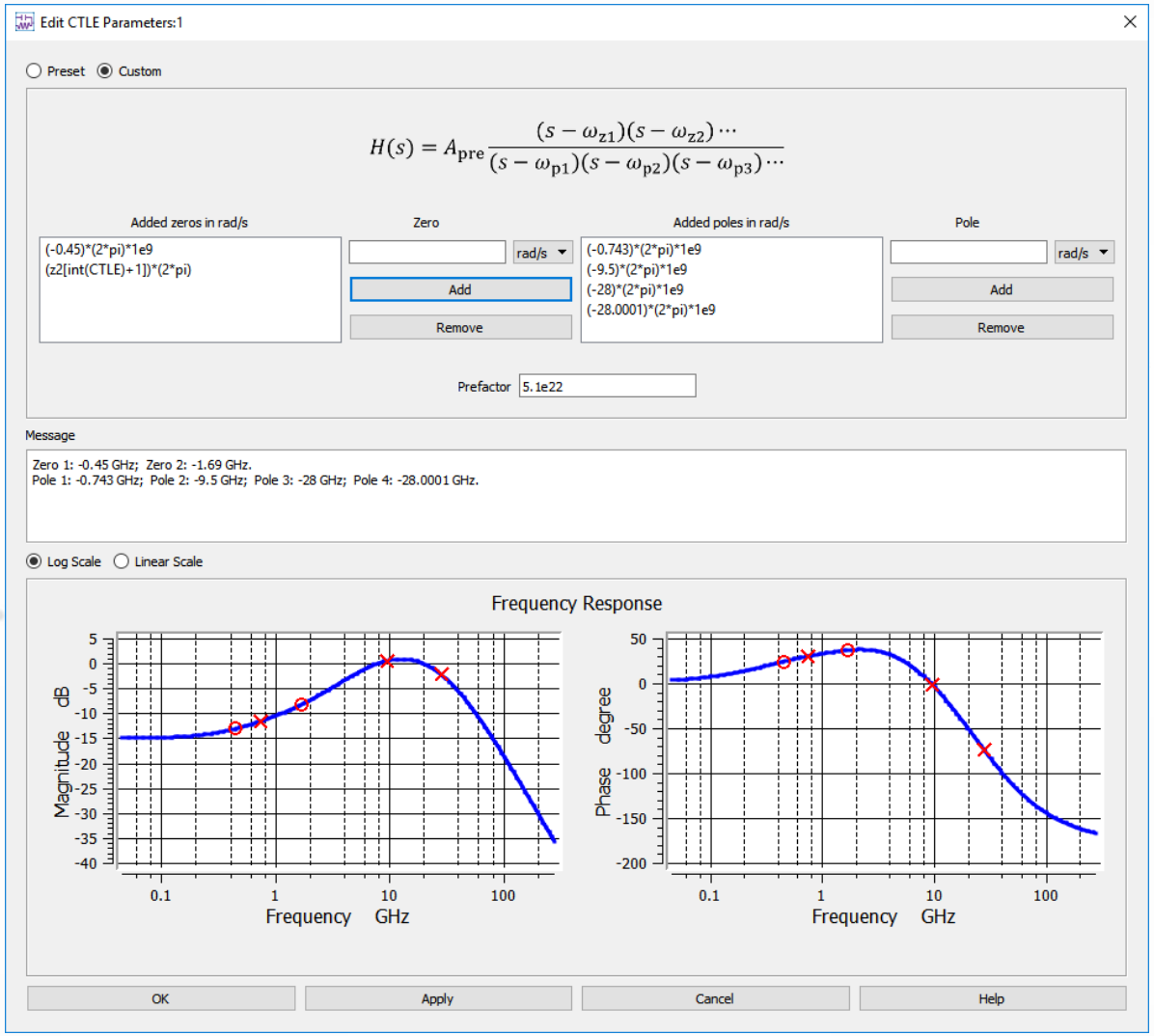


$$H(s) = \frac{\omega_{P1} * \omega_{P3} * \omega_{P4}}{\omega_{Z1}} * \frac{(s + \omega_{Z1})(s + \omega_{P2} * A_{DC})}{(s + \omega_{P1})(s + \omega_{P2})(s + \omega_{P3})(s + \omega_{P4})}$$

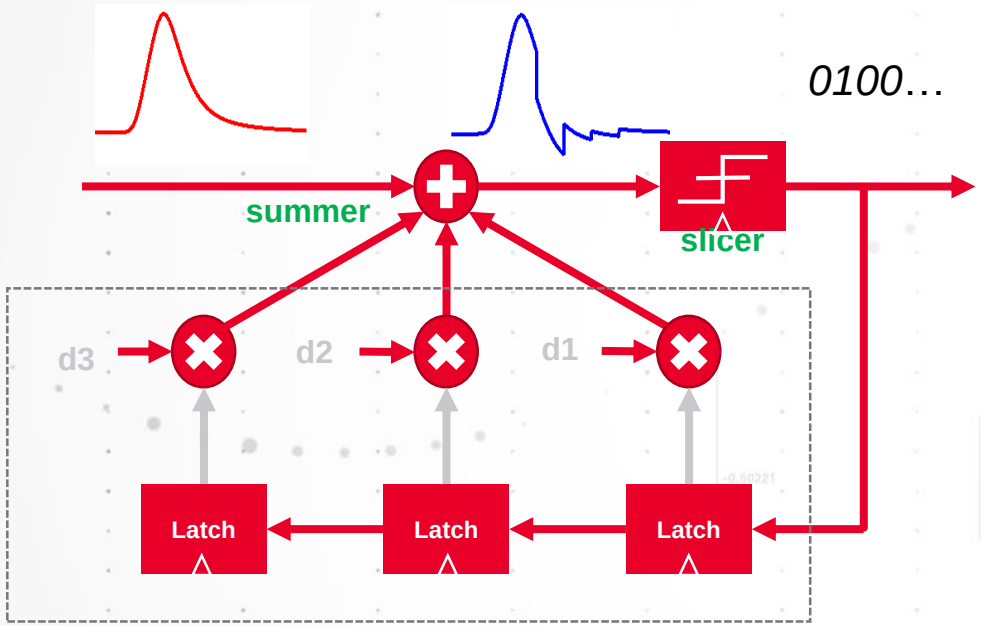
- ω = 2 * 3.14 * Frequency
- Fp1 = 1.65 * Fz1, Fp2 = 9.5 Ghz,
- Fp3 = 28 Ghz, Fp4 = 28 Ghz

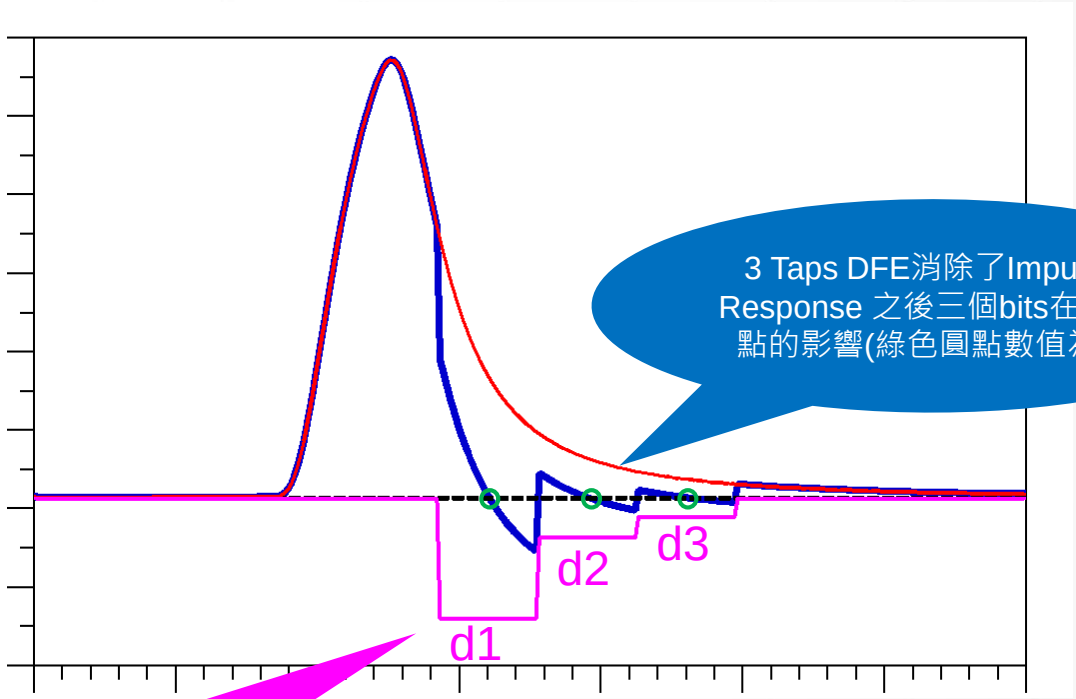
- Fz1 = 450 Mhz, Fz2 = mag(DC gain)* Fp2
- ADC = -5 dB to -15 dB
- No broadband gain

CTLE (-15dB)


Edit CTLE Parameters:1
Preset
Custom
$H(s) = A_{pre}\frac{(s-\omega_{z1})(s-\omega_{z2})\cdots}{(s-\omega_{p1})(s-\omega_{p2})(s-\omega_{p3})\cdots}$
Added zeros in rad/s
(-0.45)*(2*pi)*1e9
(z2[int(CTLE)+1])*(2*pi)
Zero
rad/s
Add
Remove
Added poles in rad/s
(-0.743)*(2*pi)*1e9
(-9.5)*(2*pi)*1e9
(-28)*(2*pi)*1e9
(-28.0001)*(2*pi)*1e9
Pole
rad/s
Add
Remove
Prefactor
5.1e22
Message
Zero 1: -0.45 GHz; Zero 2: -1.69 GHz.
Pole 1: -0.743 GHz; Pole 2: -9.5 GHz; Pole 3: -28 GHz; Pole 4: -28.0001 GHz.
Log Scale
Linear Scale
Frequency Response
Magnitude dB
Frequency GHz
Phase degree
Frequency GHz
OK
Apply
Cancel
Help

DFE (Decision Feed-back Equalizer)





3 Taps DFE消除了Impulse Response 之後三個bits在取樣點的影響(綠色圓點數值為0)

粉紅色曲線是補償訊號，與輸入訊號(紅色曲線)相加之後得到輸出訊號(藍色曲線)

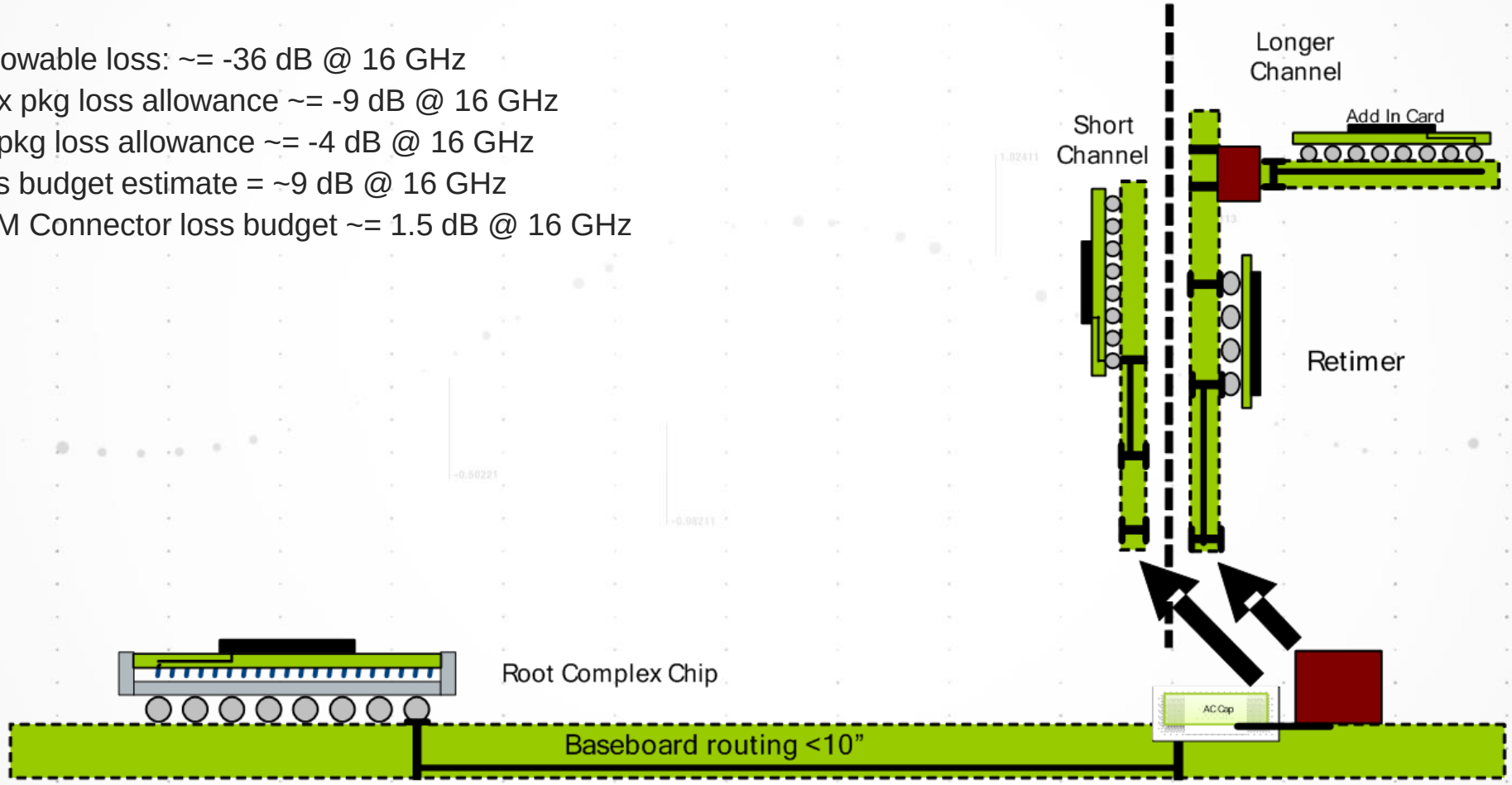
DFE

- $d1 = (\frac{h1}{h0}) \leq 0.8$
- $|d2, d3| \leq 20mV$

Note:
h1: tap magnitude
h0: cursor strength

Channel Tolerance

- Estimated allowable loss: ~= -36 dB @ 16 GHz
- Root complex pkg loss allowance ~= -9 dB @ 16 GHz
- Add-in Card pkg loss allowance ~= -4 dB @ 16 GHz
- Total AIC loss budget estimate = ~9 dB @ 16 GHz
- PCIe 5.0 CEM Connector loss budget ~= 1.5 dB @ 16 GHz

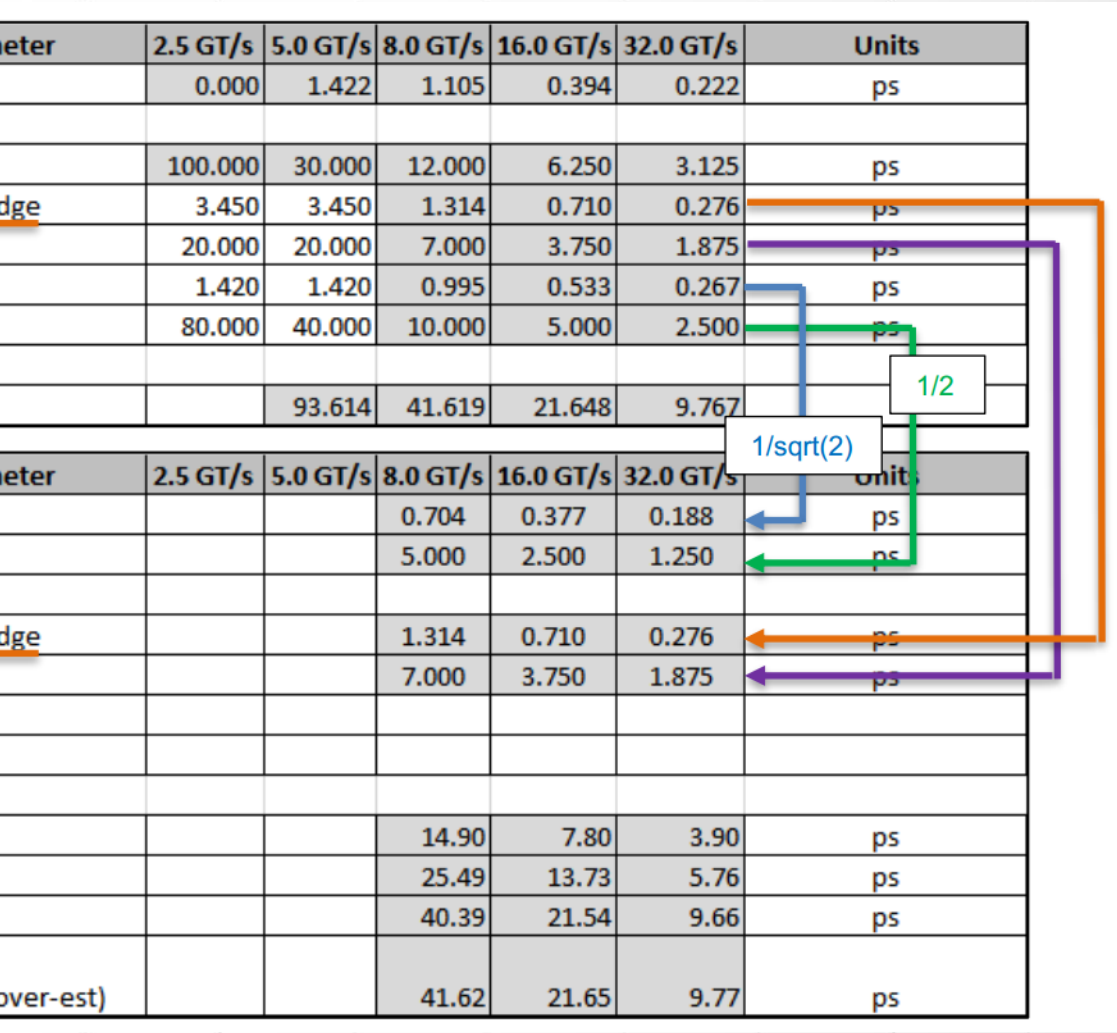


Jitter

$T_{TX\text{-}CH\text{-}URJ\text{-}32G}$	Tx uncorrelated Rj	0.276	ps RMS
$T_{TX\text{-}CH\text{-}UDJDD\text{-}32G}$	Tx uncorrelated DjDD	1.875	ps PP
$T_{TX\text{-}CH\text{-}UPW\text{-}RJ\text{-}32G}$	Uncorrelated PW Rj	0.27	ps RMS
$T_{TX\text{-}CH\text{-}UPW\text{-}DJ\text{-}32G}$	PW DDj	2.5	ps PP

Label	Jitter Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units
jit_hfrj_nui	Tx Rj (HF+LF) edge	0.000	1.422	1.105	0.394	0.222	ps
T-TX UDJDD	Tx Dj (HF+LF) edge	100.000	30.000	12.000	6.250	3.125	ps
TTX-CH-URJ	Tx Rj (LF) + Clk Rj edge	3.450	3.450	1.314	0.710	0.276	ps
TTX-CH-UDJDD	Tx Dj (LF) edge	20.000	20.000	7.000	3.750	1.875	ps
TTX-CH-UPW-RJ	Tx Rj (HF) PW	1.420	1.420	0.995	0.533	0.267	ps
TTX-CH-UPW-DJ	Tx Dj (HF) PW	80.000	40.000	10.000	5.000	2.500	ps
Total Jitter	T-TX UTJ + Clk Rj		93.614	41.619	21.648	9.767	

Label	Jitter Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units
Tx_Rj	Tx Rj (HF) edge			0.704	0.377	0.188	ps
Tx_Dj	Tx Dj (HF) edge			5.000	2.500	1.250	ps
Tx_DCD							
Rx_Rj	Tx Rj (LF) + Clk Rj edge			1.314	0.710	0.276	ps
Rx_Dj	Tx Dj (LF) edge			7.000	3.750	1.875	ps
Rx_DCD							
Rx_Noise							
Tx Total Jitter	Tx Dj + Tx Rj			14.90	7.80	3.90	ps
Rx Total Jitter	Rx Dj + Rx Rj			25.49	13.73	5.76	ps
Total Jitter	Tx + Rx			40.39	21.54	9.66	ps
T_TX_UTJ + T_REFCLK_RMS	Total Jitter check (over-est)			41.62	21.65	9.77	ps



- Deterministic **edge** jitter = (1/2) Deterministic **pulse width** jitter
- Random **edge** jitter = (1/sqrt(2)) Random **pulse width** jitter

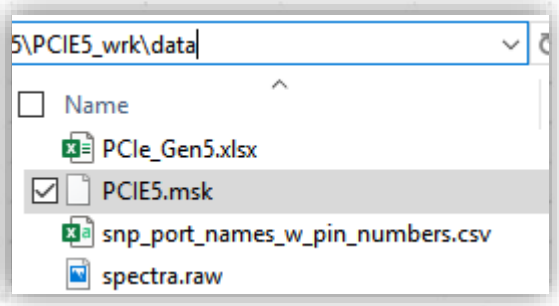
Total RJ Verification

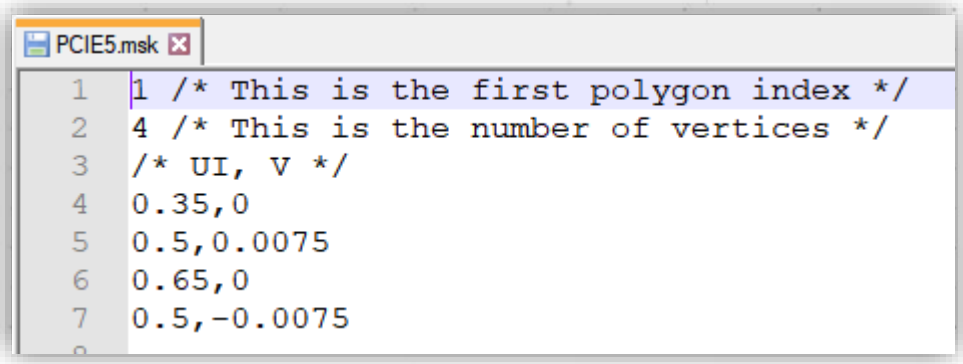
Label	Jitter Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units
Rj check 1	Tx Rj + Rx Rj			1.491	0.804	0.334	ps
Rj check 2	Tx Rj (HF+LF) + Clk Rj			1.491	0.804	0.334	ps
Rj check 3	Tx Rj (HF) + Tx Rj (LF) + Clk Rj			1.491	0.804	0.334	ps

Label	Jitter Parameter	Formula
Rj check 1	Tx Rj + Rx Rj	'=SQRT(Tx_Rj^2+Rx_Rj^2)
Rj check 2	Tx Rj (HF+LF) + Clk Rj	'=SQRT(jit_hfrj_nui^2+T_REFCLK_RMS^2)
Rj check 3	Tx Rj (HF) + Tx Rj (LF) + Clk Rj	'=SQRT(((TTX_CH_UPW_RJ/SQRT(2))^2)+TTX_CH_URJ^2)

EYE

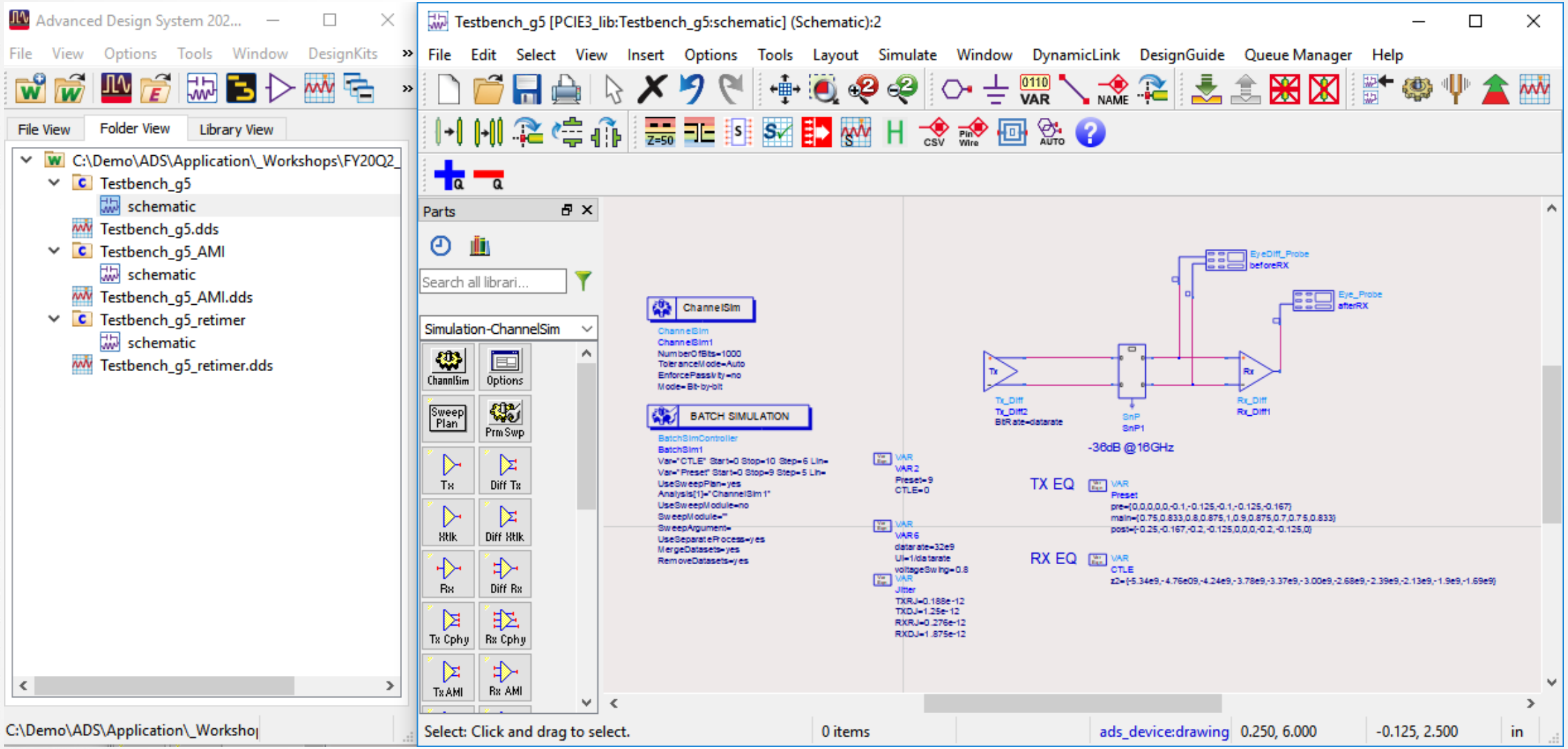
- $Eye\ Height \leq 15mVPP$
- $Eye\ Width\ at\ zero\ crossing \leq 0.3\text{UI}$



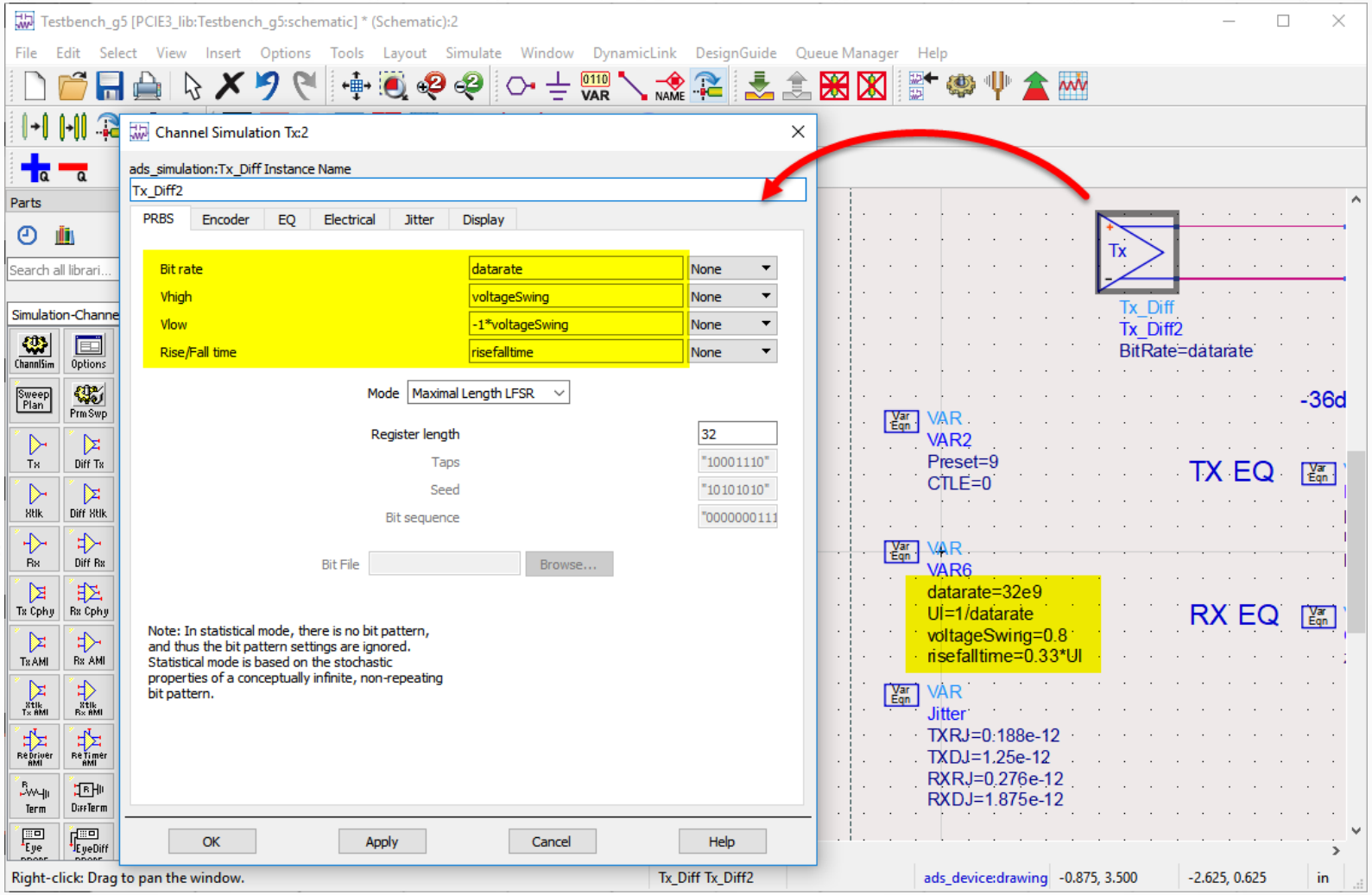


Lab3 PCIe Gen5 Testbench

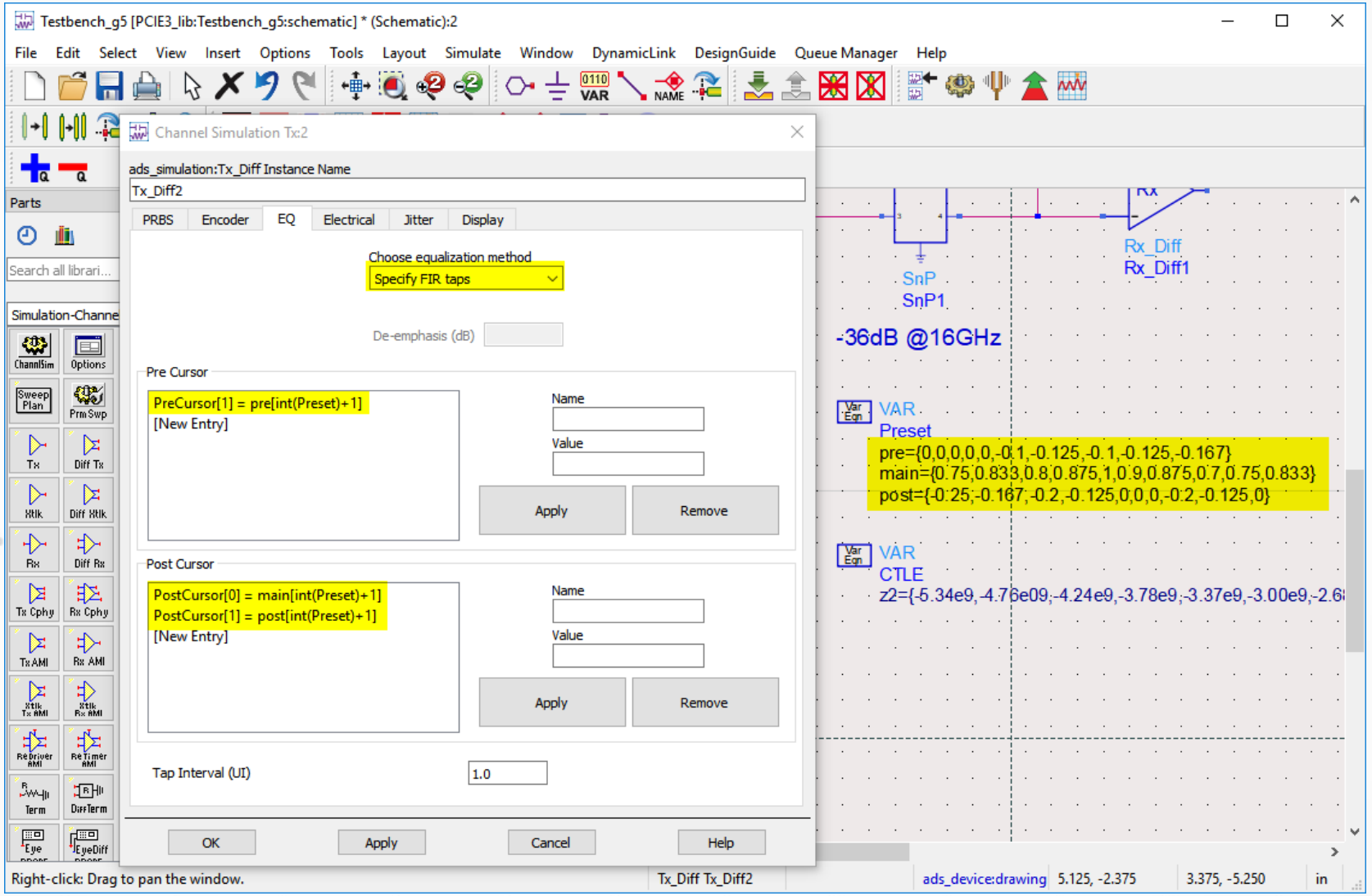
ADS TX/RX Model



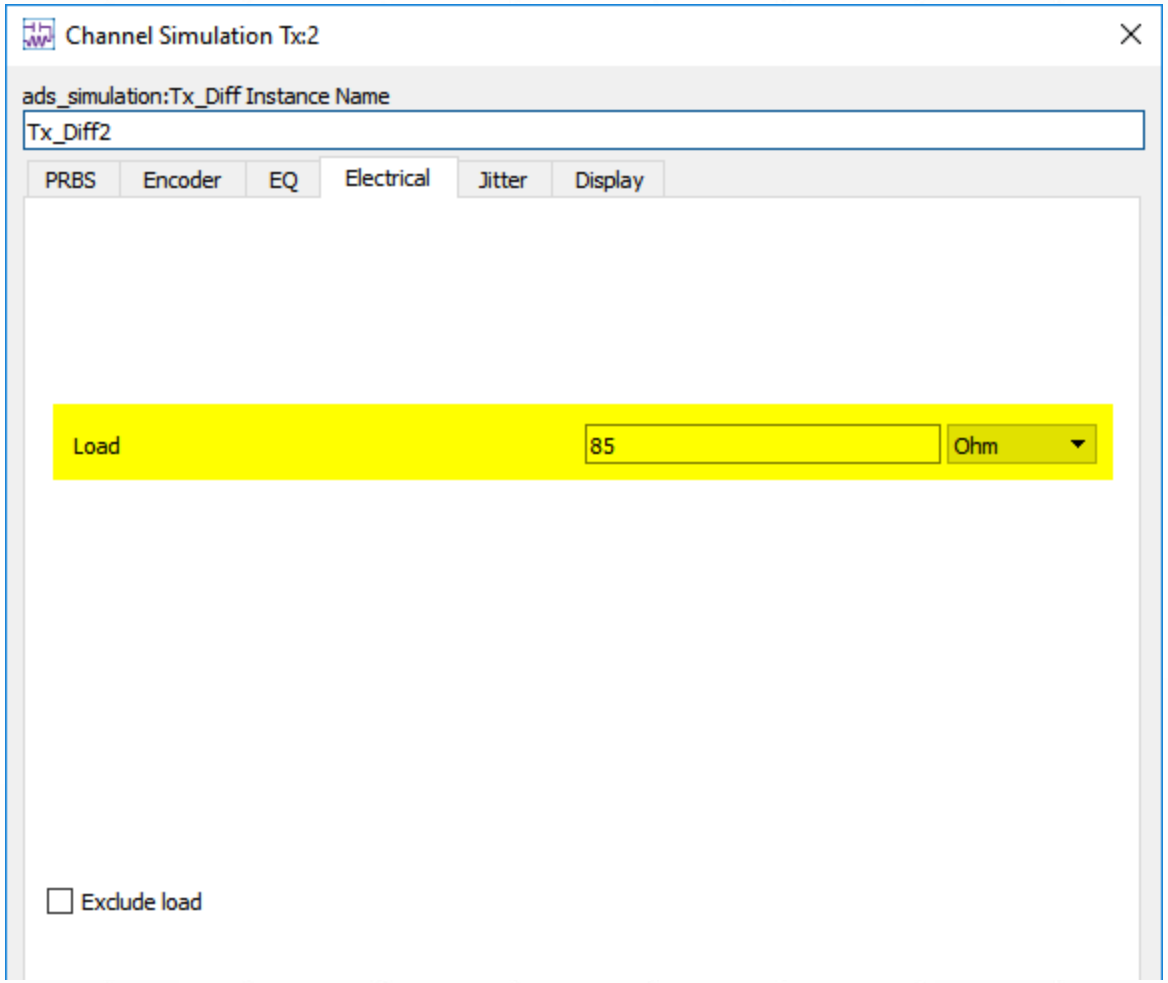
ADS TX/RX Model (TX PRBS)



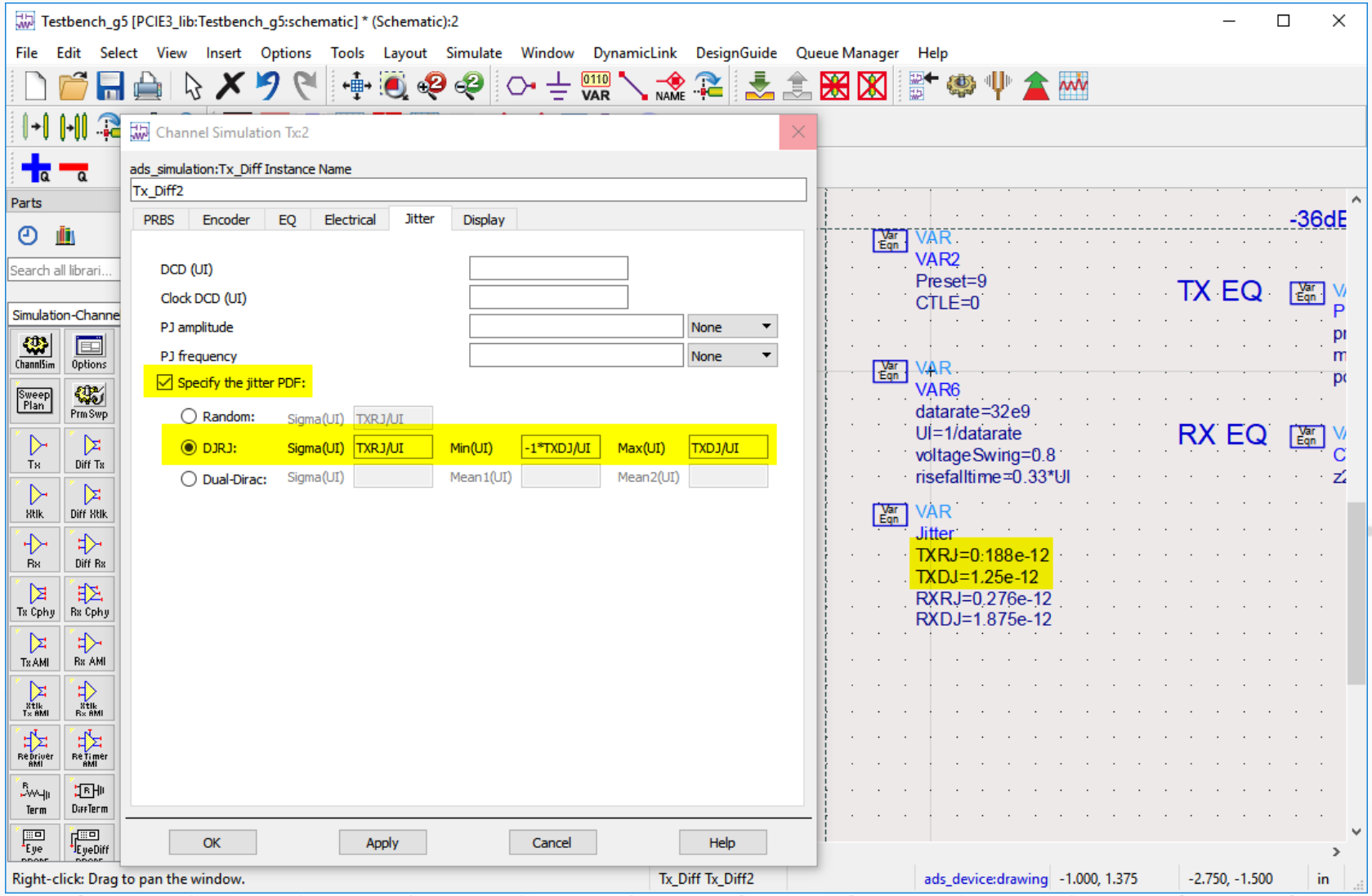
ADS TX/RX Model (TX Preset)



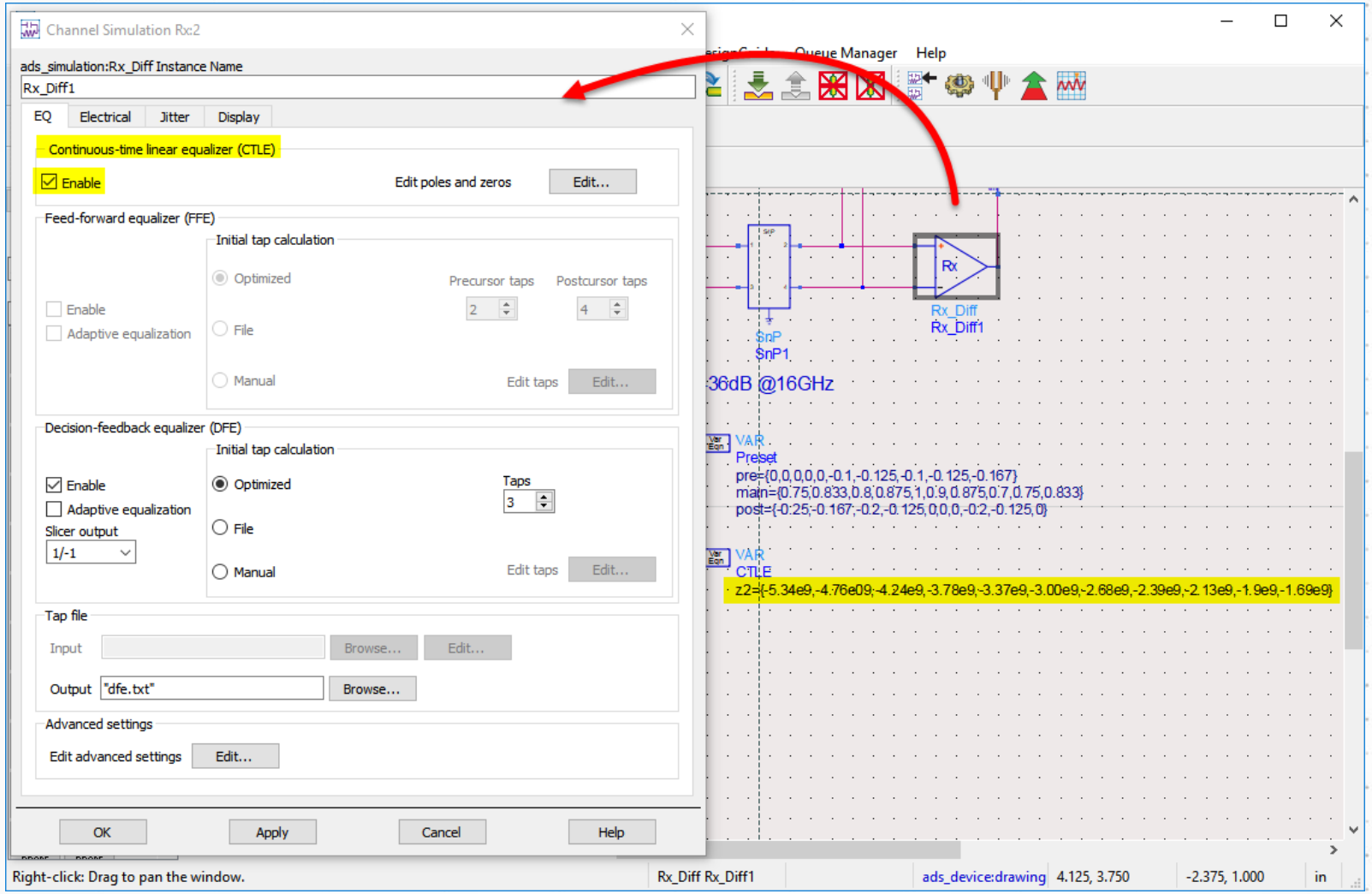
ADS TX/RX Model (TX Source Impedance)



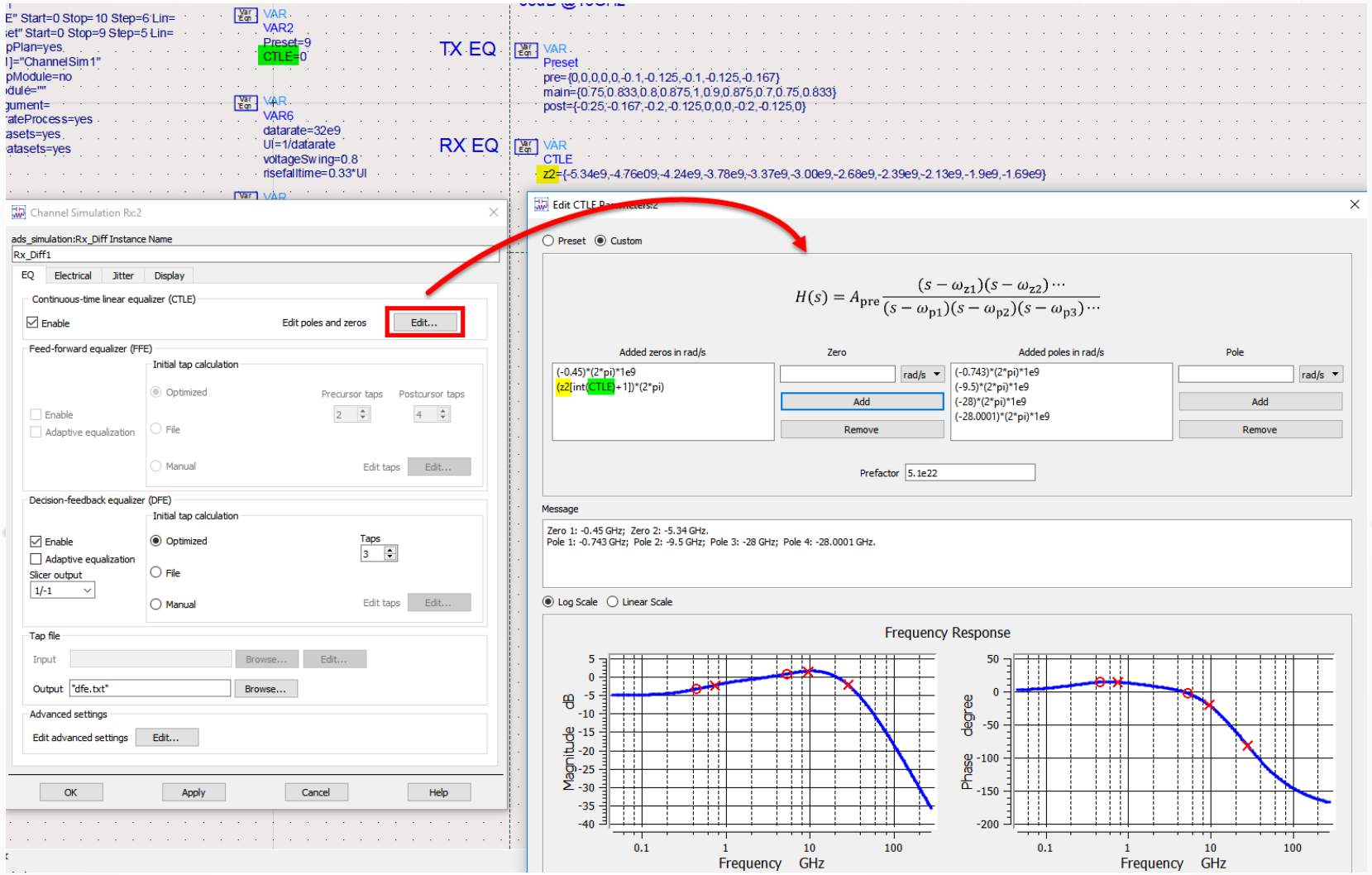
ADS TX/RX Model (TX Jitter)



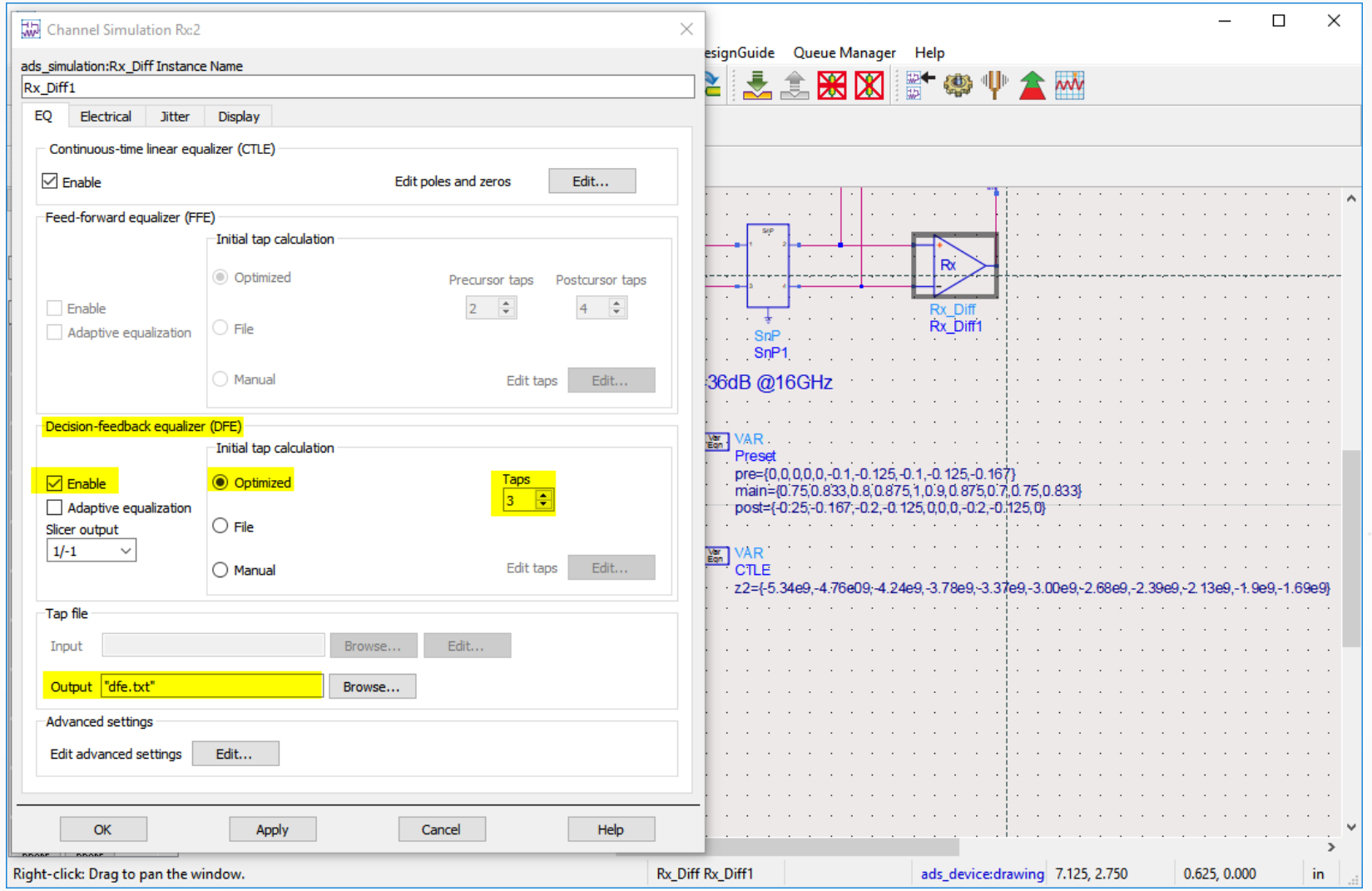
ADS TX/RX Model (RX CTLE)



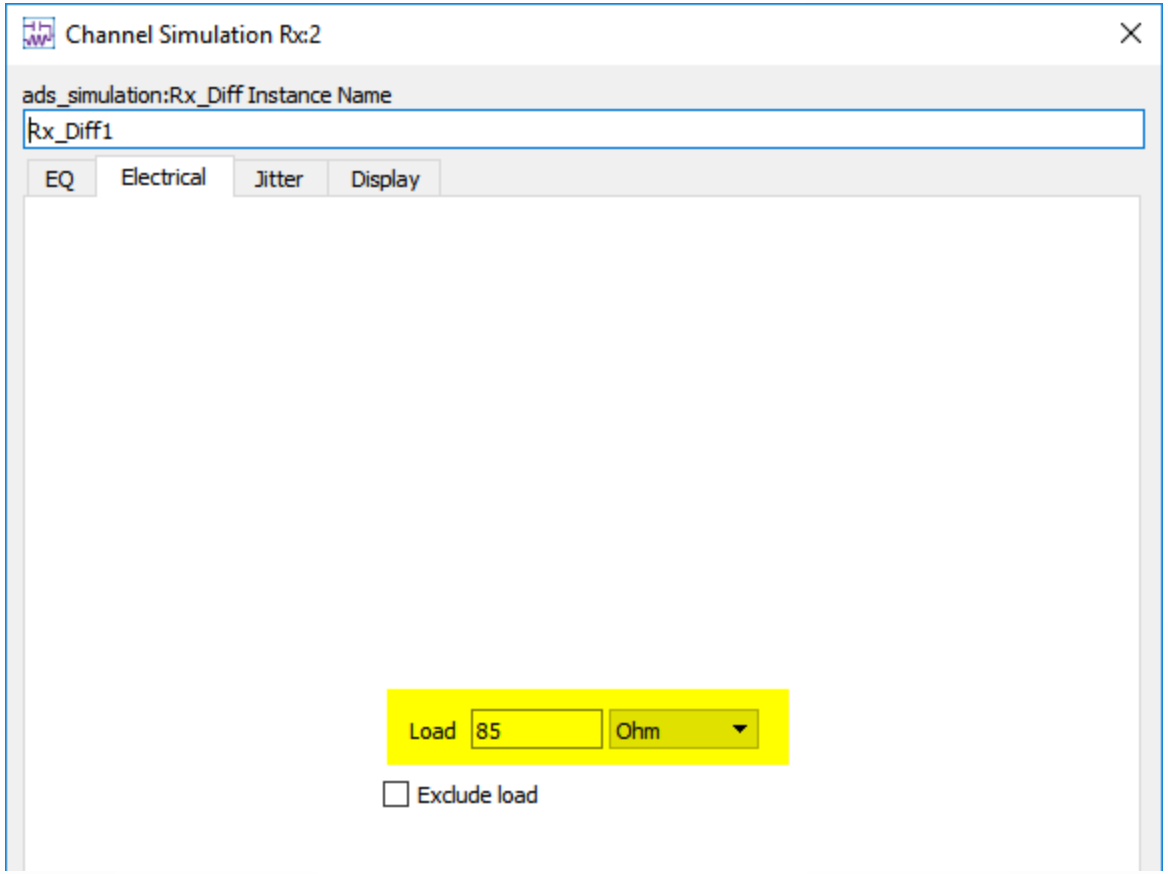
ADS TX/RX Model (RX CTLE)



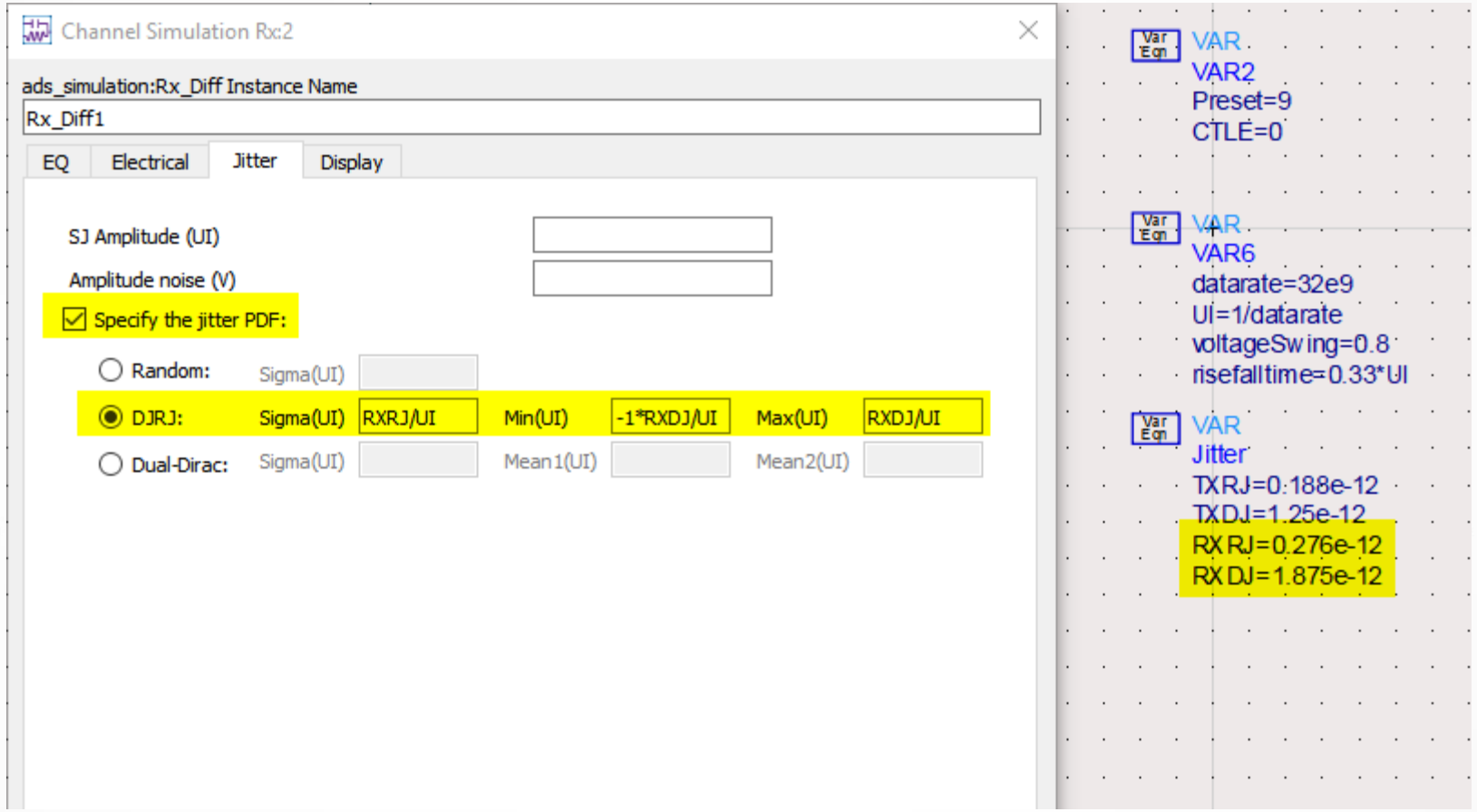
ADS TX/RX Model (RX 3-tap DFE)



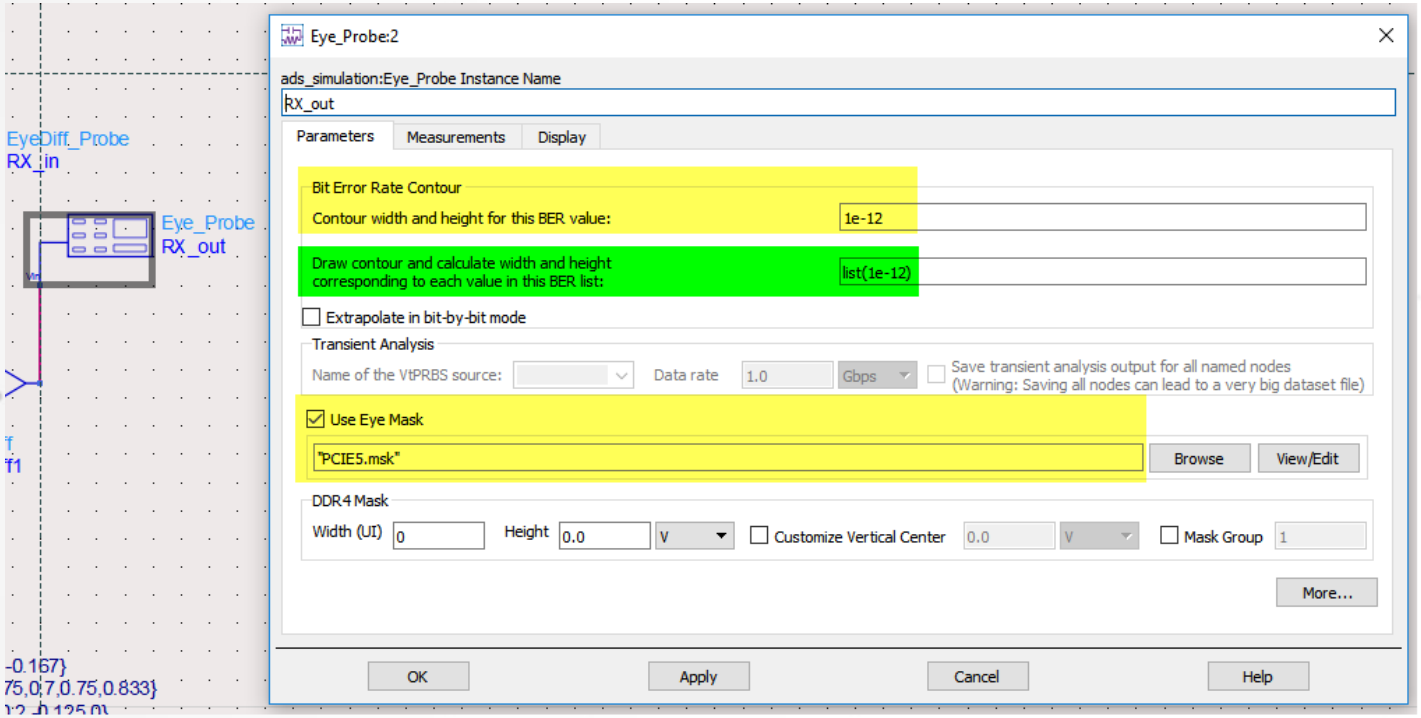
ADS TX/RX Model (RX Load Impedance)

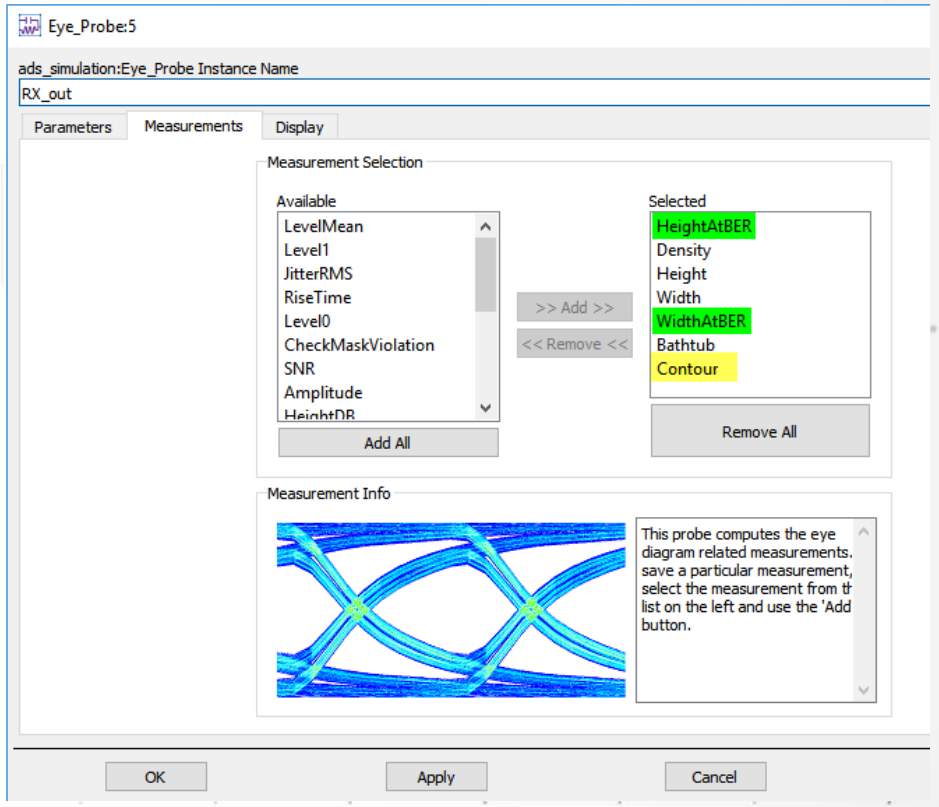


ADS TX/RX Model (RX Jitter)

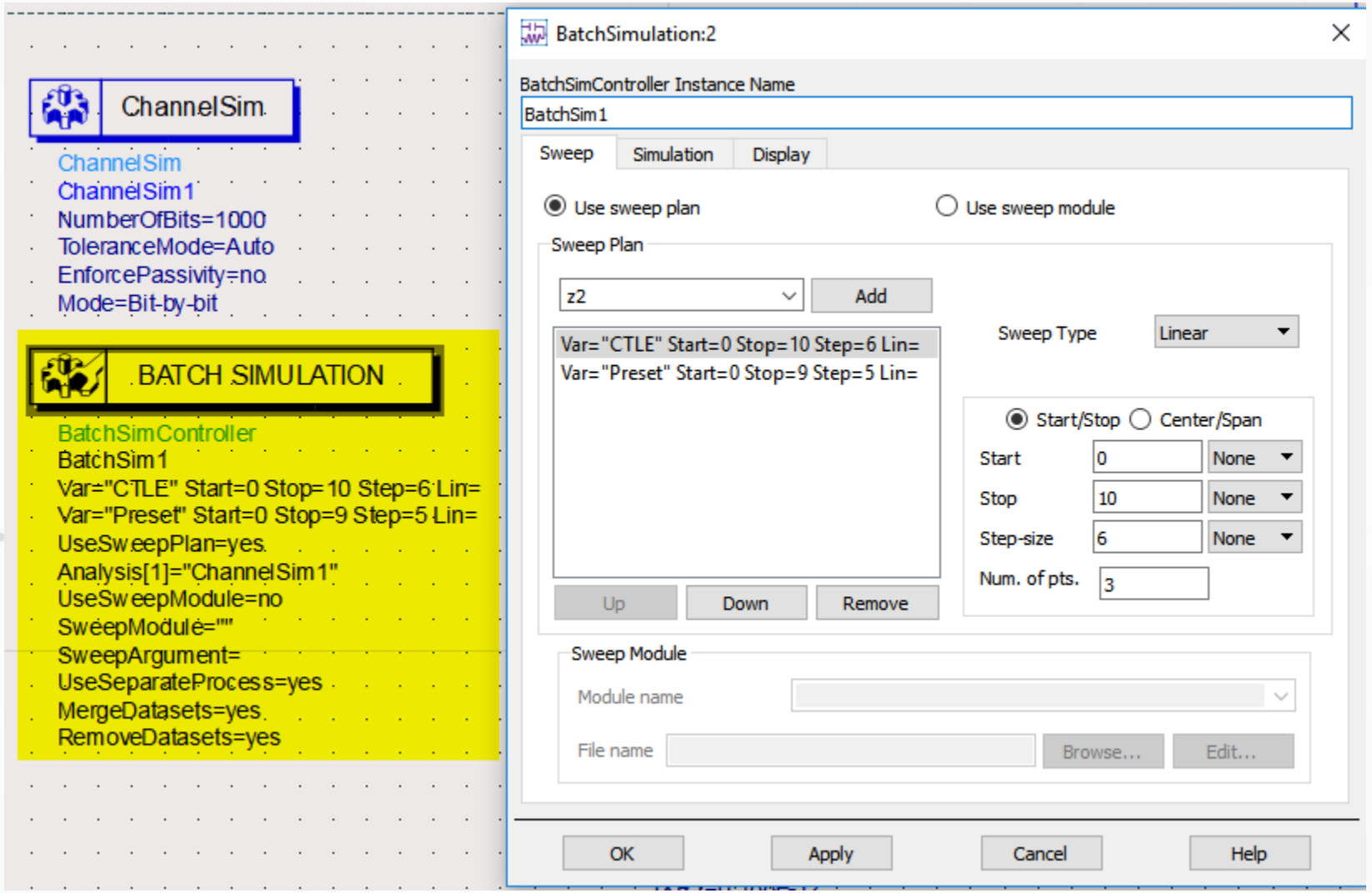


EYE Probe

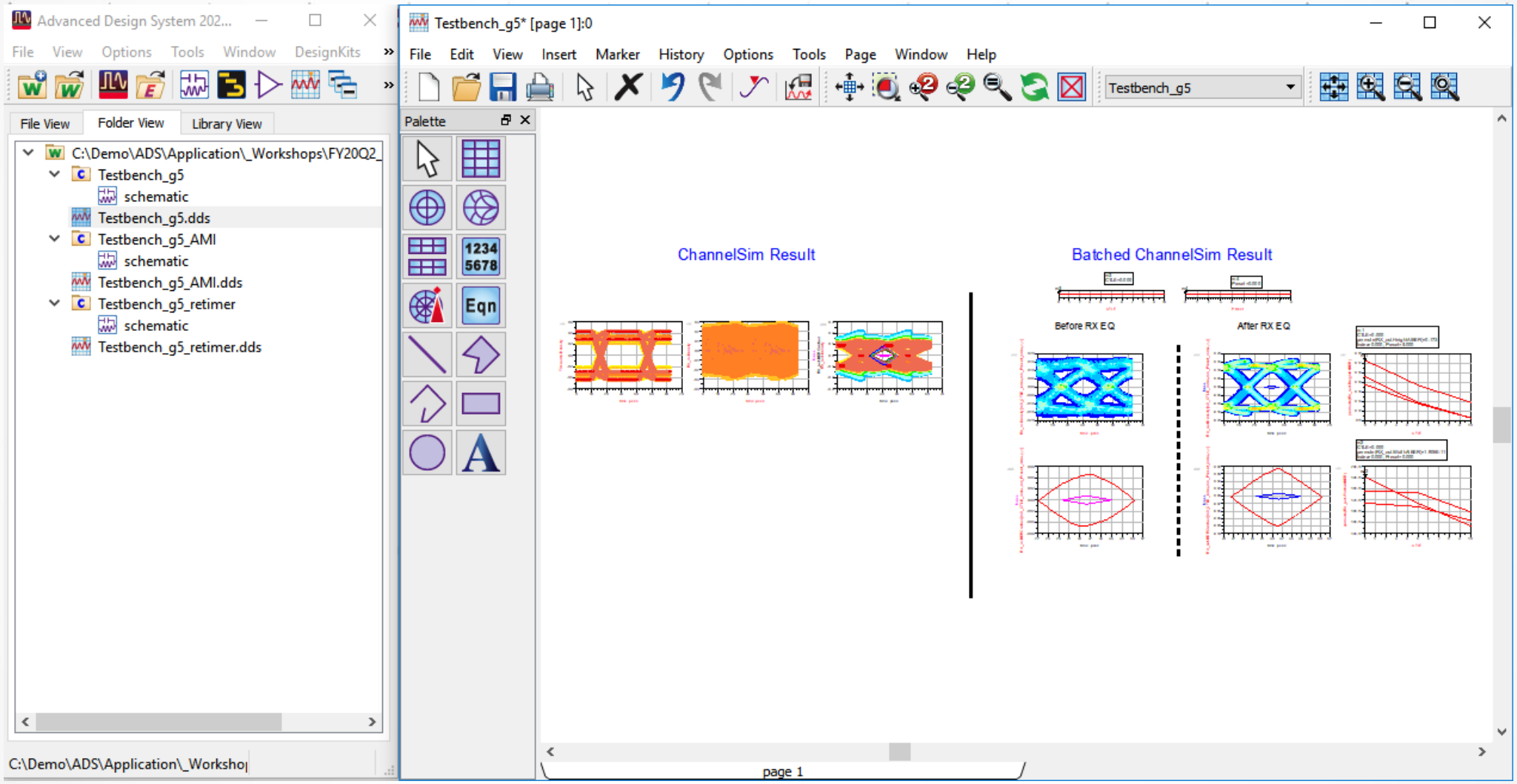

EyeDiff_Probe
RX_in
Eye_Probe
RX_out
Eye_Probe:2
ads_simulation:Eye_Probe Instance Name
RX_out
Parameters
Measurements
Display
Bit Error Rate Contour
Contour width and height for this BER value:
1e-12
Draw contour and calculate width and height corresponding to each value in this BER list:
list(1e-12)
Extrapolate in bit-by-bit mode
Transient Analysis
Name of the VtPRBS source:
Data rate
1.0
Gbps
Save transient analysis output for all named nodes
(Warning: Saving all nodes can lead to a very big dataset file)
Use Eye Mask
"PCIE5.msk"
Browse
View/Edit
DDR4 Mask
Width (UI)
0
Height
0.0
V
Customize Vertical Center
0.0
Mask Group
1
More...
OK
Apply
Cancel
Help


Eye_Probe:5
ads_simulation:Eye_Probe Instance Name
RX_out
Parameters
Measurements
Display
Measurement Selection
Available
LevelMean
Level1
JitterRMS
RiseTime
Level0
CheckMaskViolation
SNR
Amplitude
Add All
>> Add >>
<< Remove <<
Selected
HeightAtBER
Density
Height
Width
WidthAtBER
Bathtub
Contour
Remove All
Measurement Info
This probe computes the eye diagram related measurements. save a particular measurement, select the measurement from th list on the left and use the 'Add button.
OK
Apply
Cancel

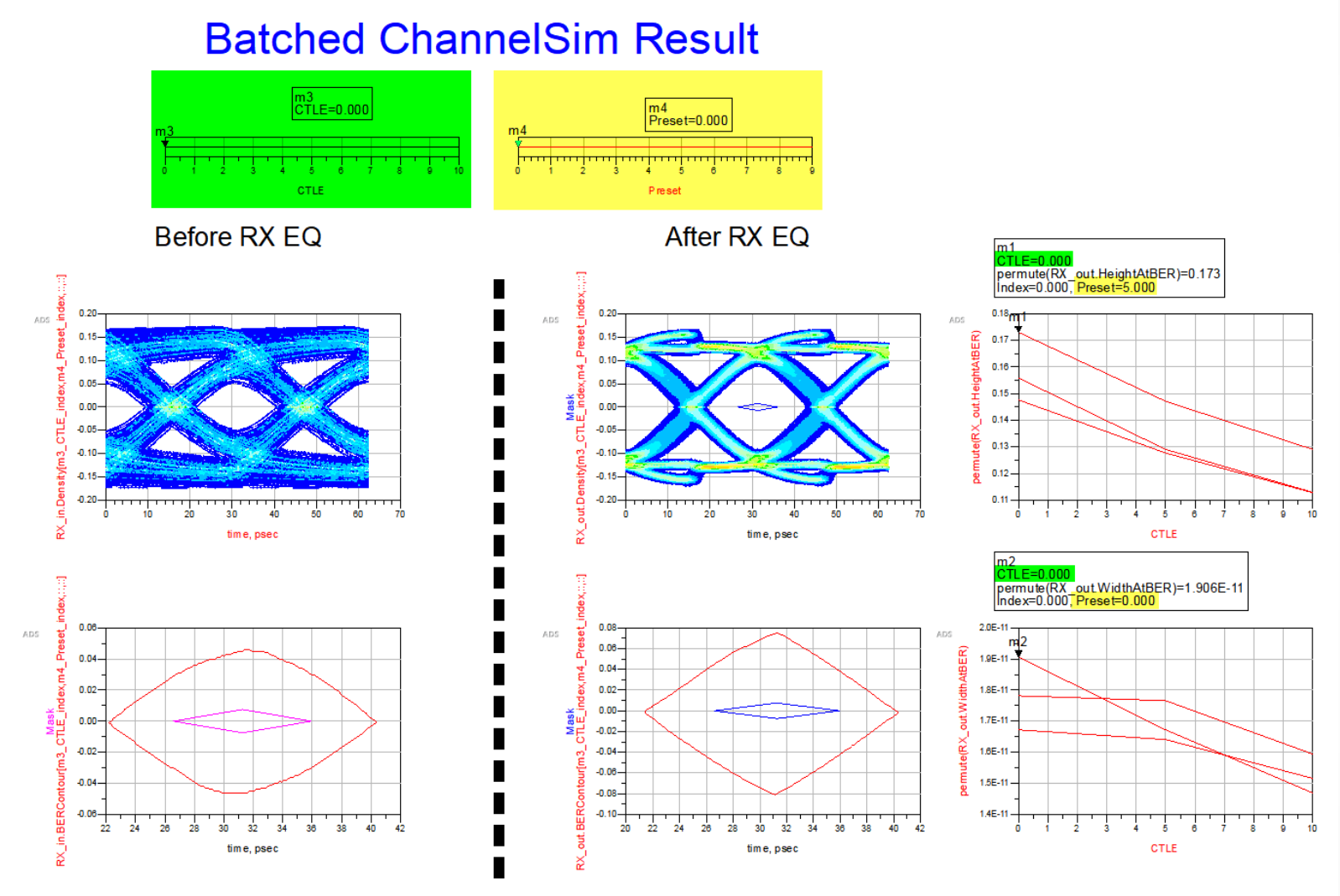
Batch CTLE and Preset



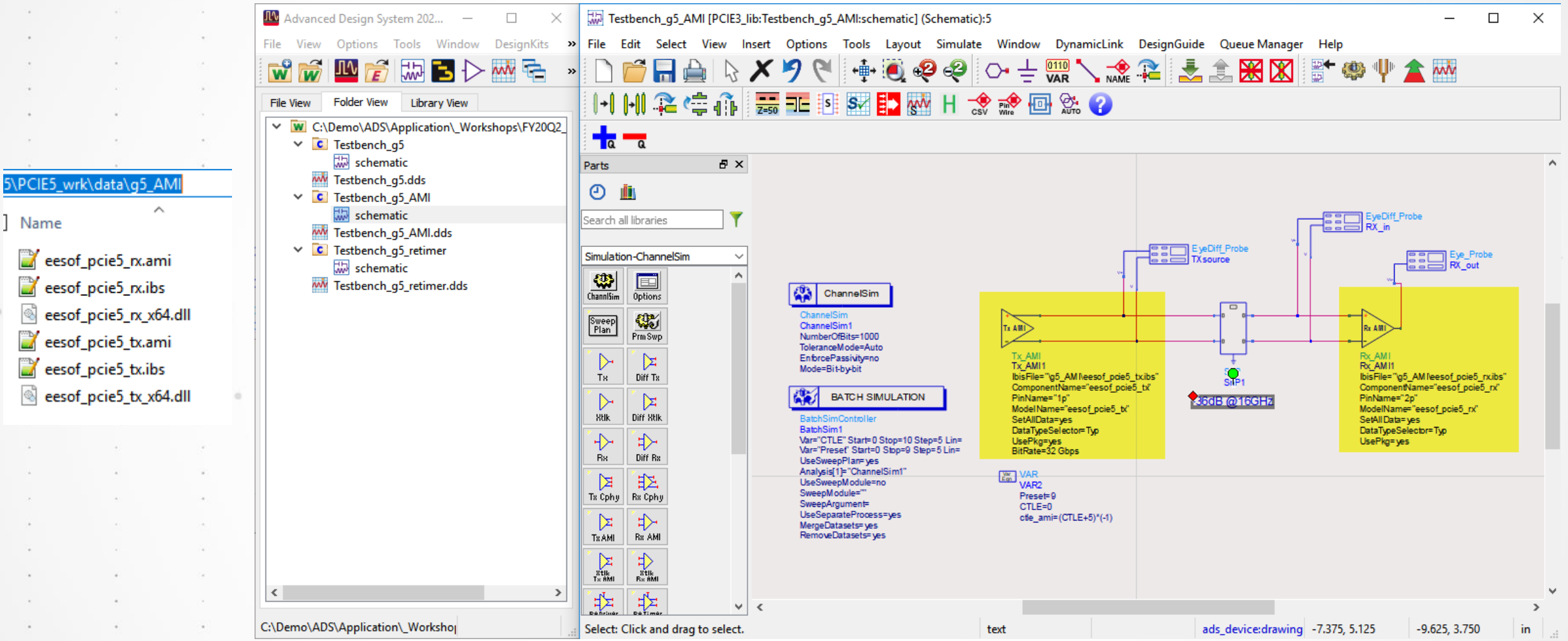
Results (38s, 9 scenarios)



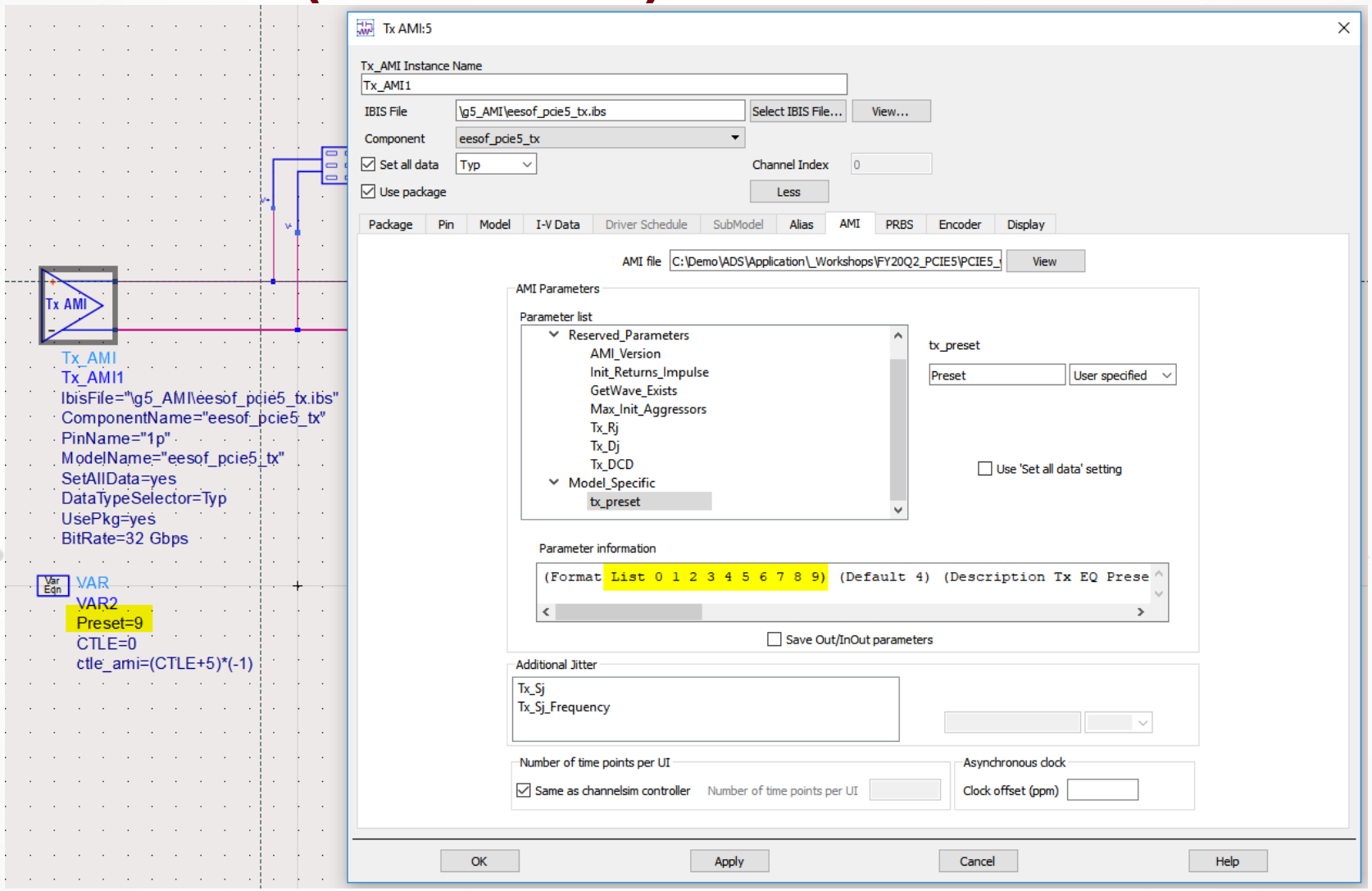
Best Setup, In terms of EYE_Height and EYE_Width



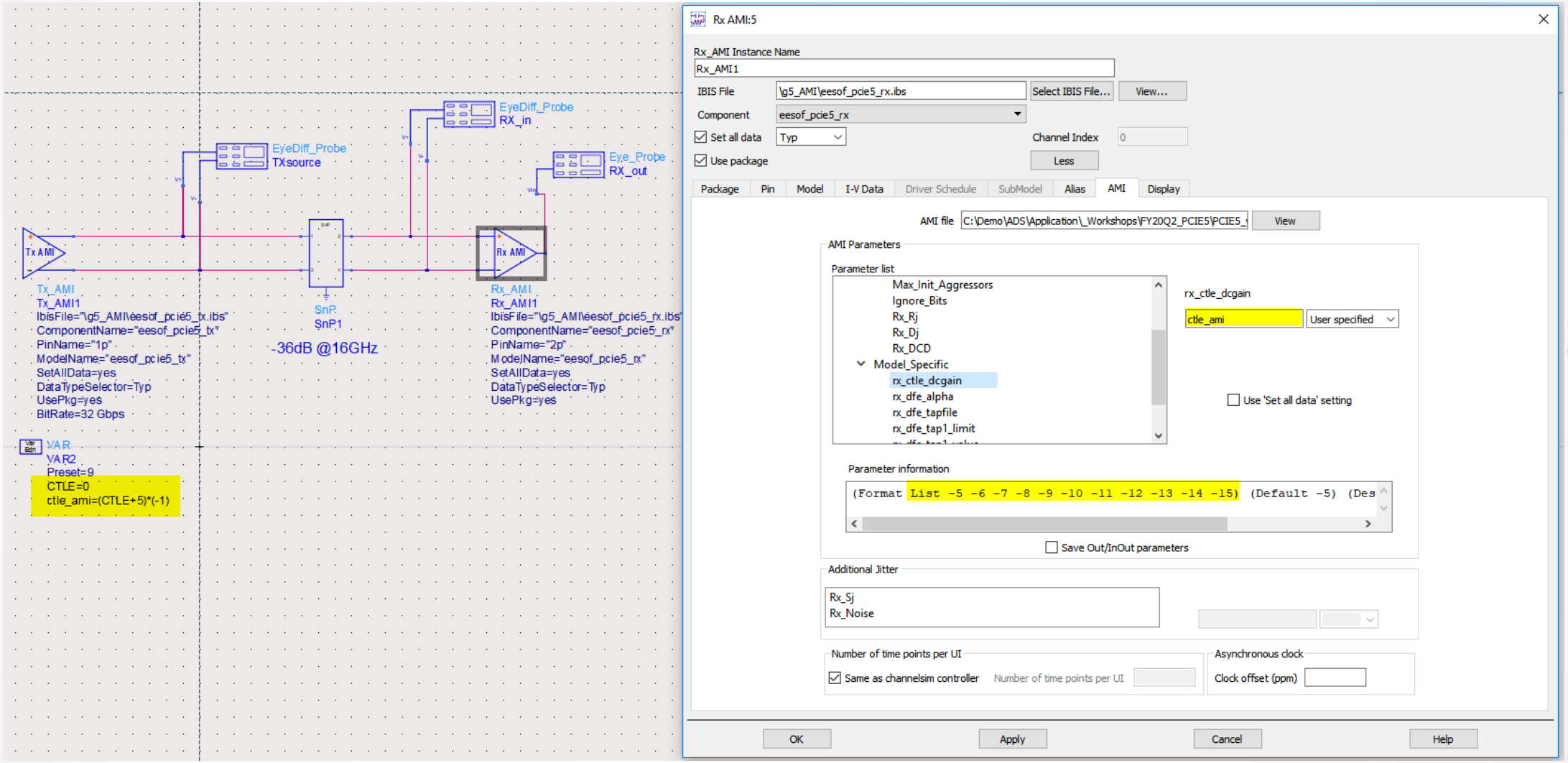
Gen5 AMI Model and Testbench



Gen5 AMI Model (TX Preset)

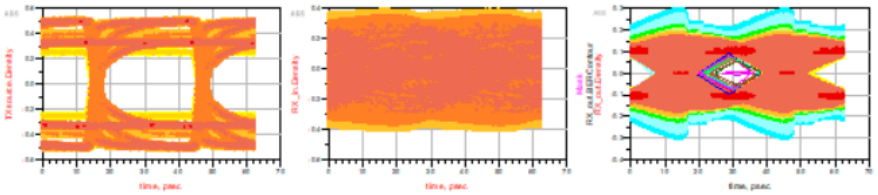


Gen5 AMI Model (RX CTLE)

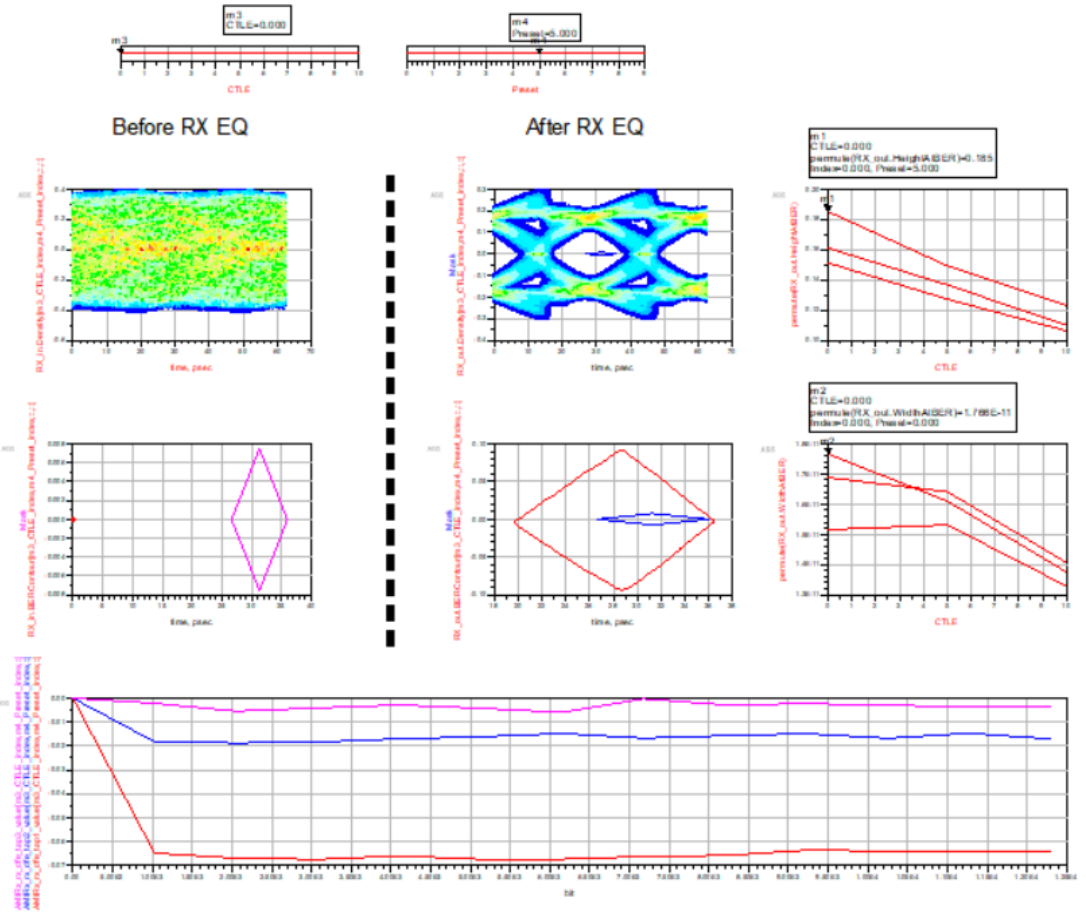


Results (80s, 9 scenarios)

ChannelSim Result

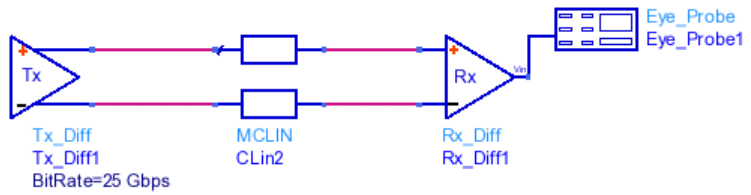


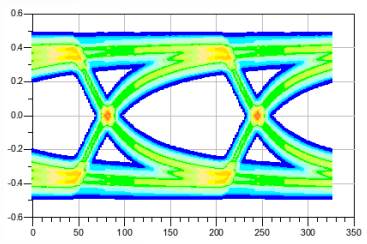
Batched ChannelSim Result

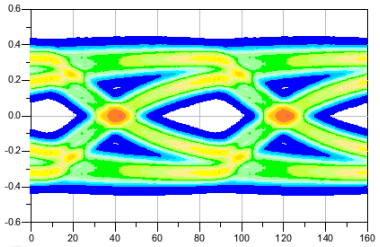


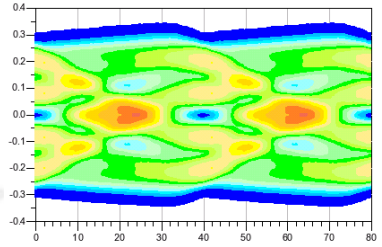
Lab4 Repeater (Retimer/ Redriver) Usage

What is Repeater





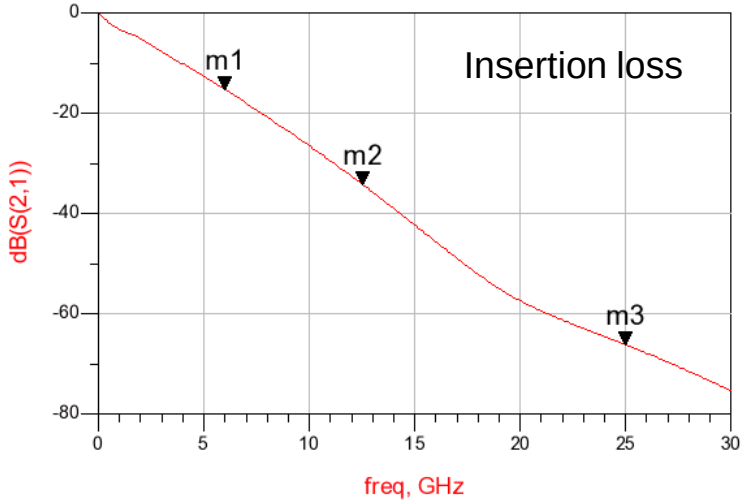




m1
freq=6.000GHz
dB(S(2,1))=-15.426

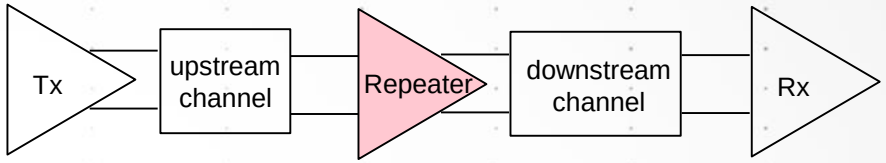
m2
freq=12.50GHz
dB(S(2,1))=-34.213

m3
freq=25.00GHz
dB(S(2,1))=-66.236



As data rate rises, channel loss increases, eye open decreases.

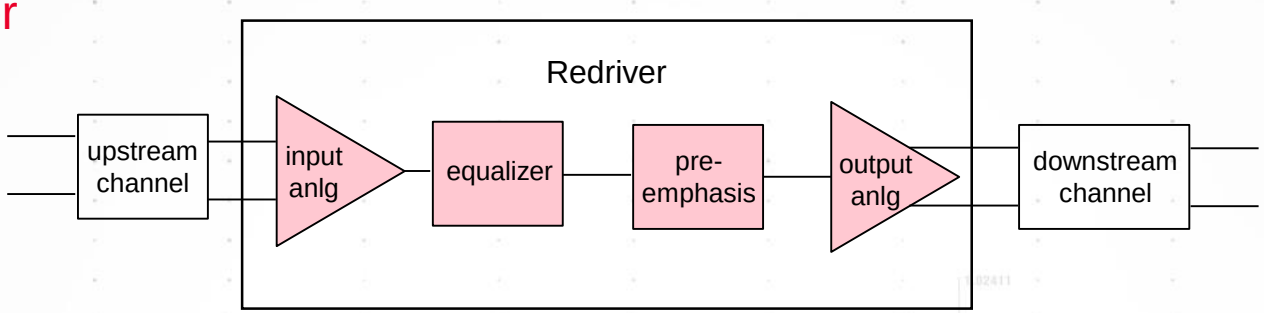
What is Repeater



- Repeater is placed in the middle of a channel
- Equalizes incoming signal to compensates loss in upstream channel
- Retransmit signal into downstream channel and apply pre-emphasis
- Repeater is both Rx and Tx
- Two types of Repeater: Redriver and Retimer

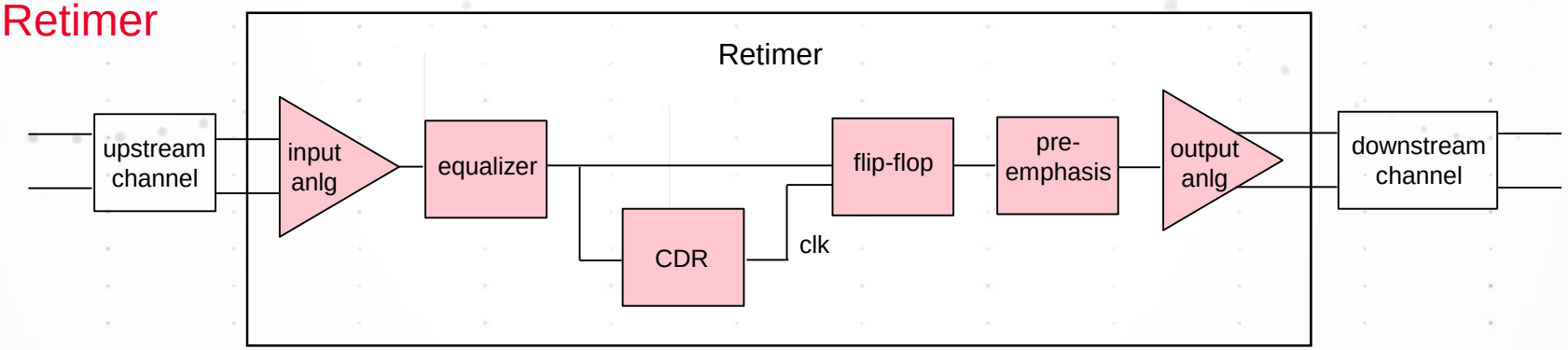
What is Repeater

Redriver



- Redriver output circuit is driven continuously by input signal
- No retiming is performed

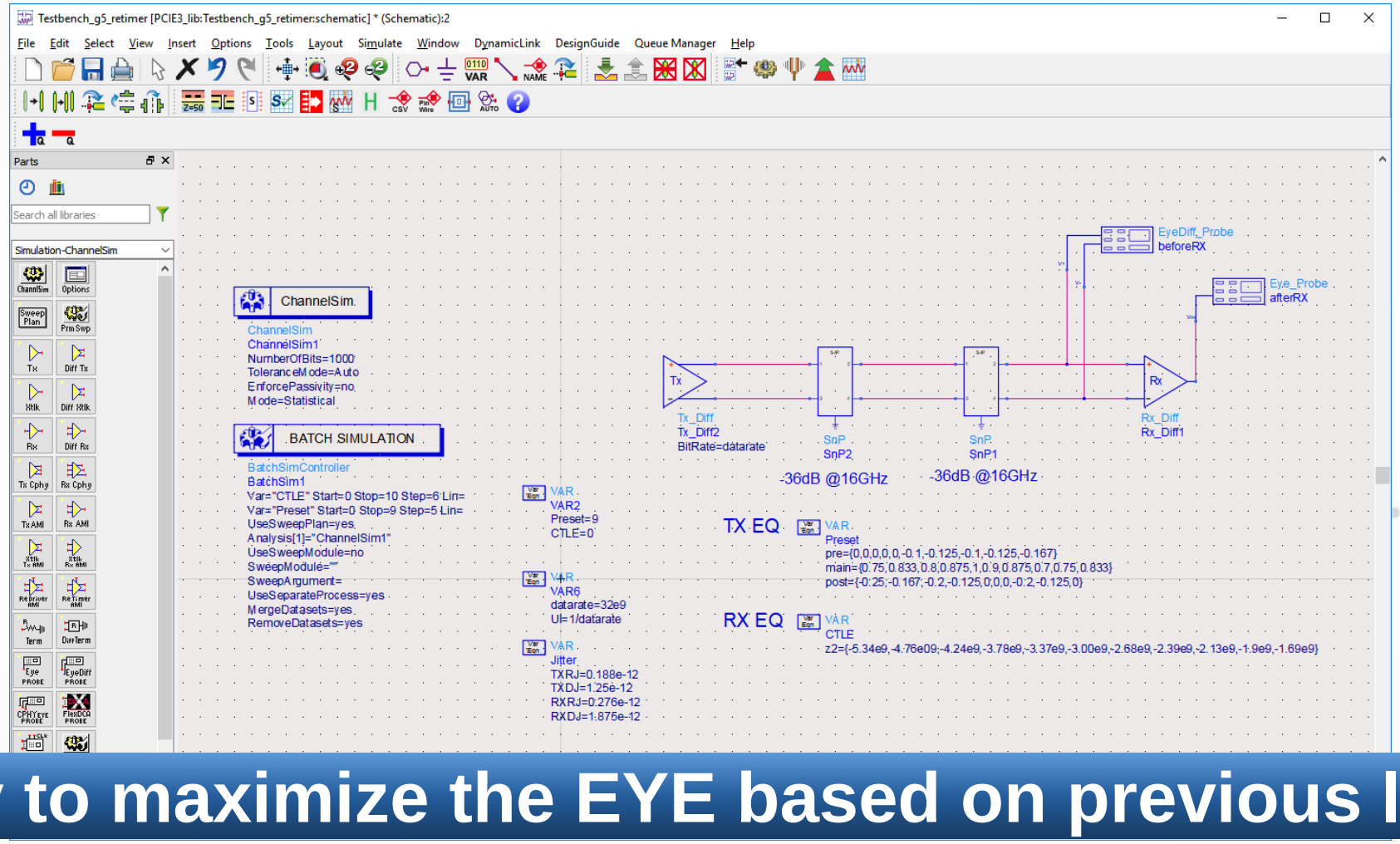
Retimer



- Retimer output buffer is driven by switching events of flip-flop. Digital data is recovered.
- Clock-data recovery (CDR) retimes the output signal. Jitter in clock is passed down to downstream channel.

Lab5 PCIe Gen5 Testbench with Retimer

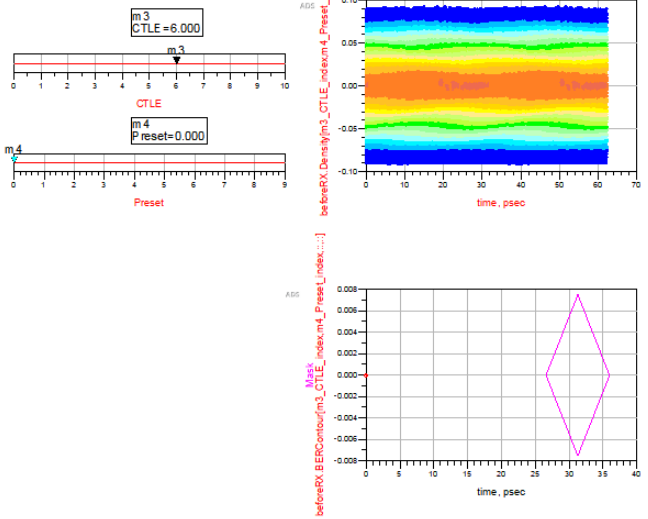
What if Longer Trace?



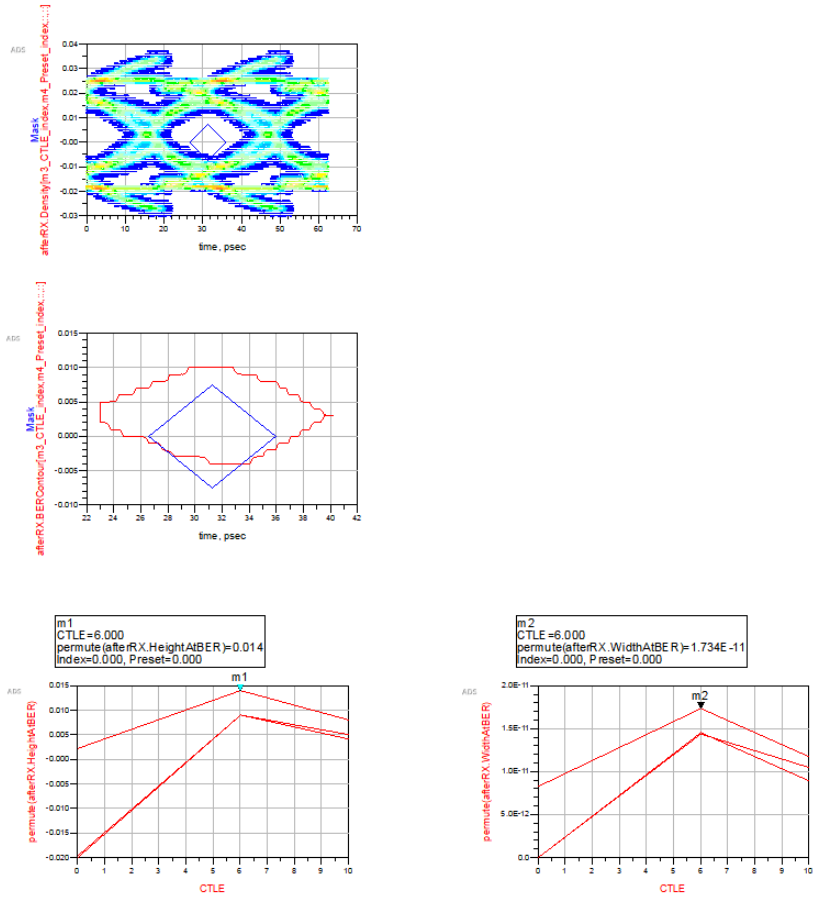
Try to maximize the EYE based on previous lab.

What if Longer Trace?

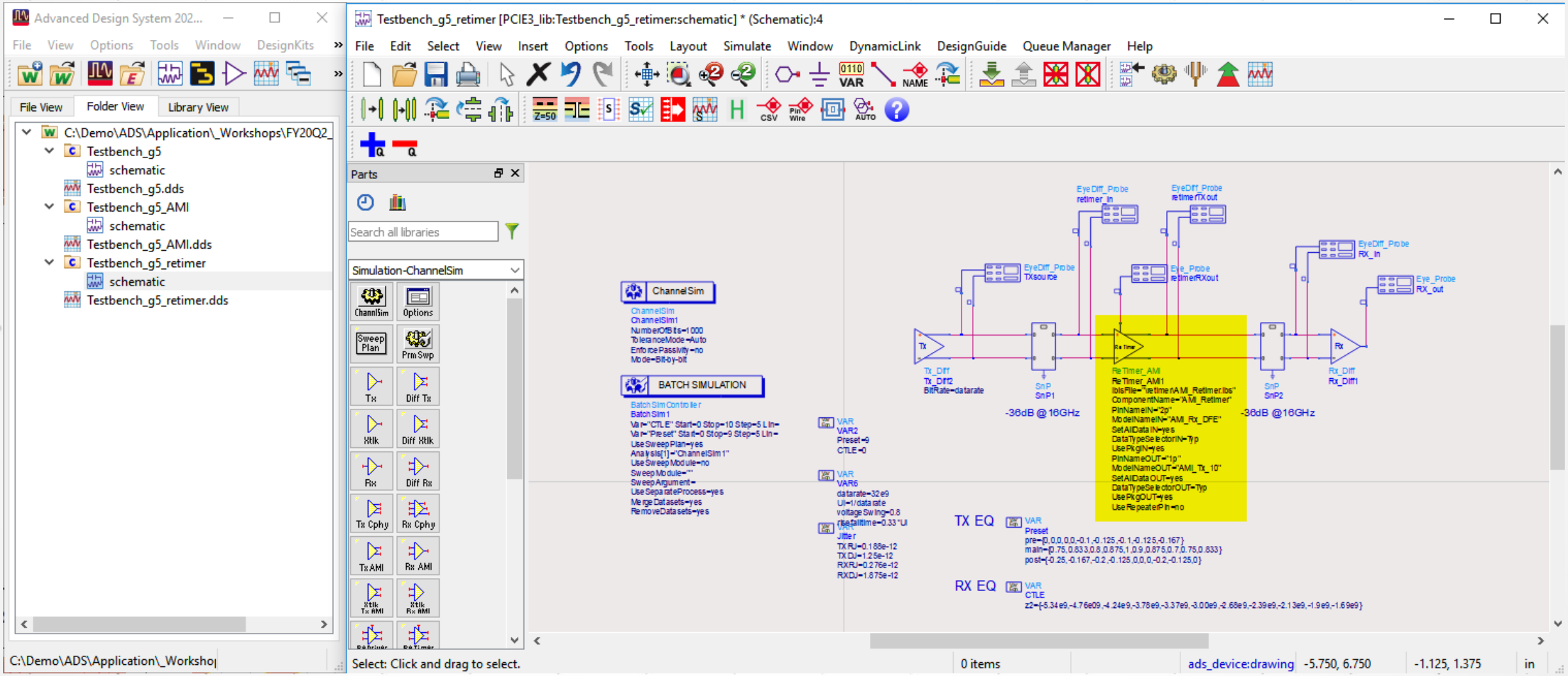
Before RX EQ



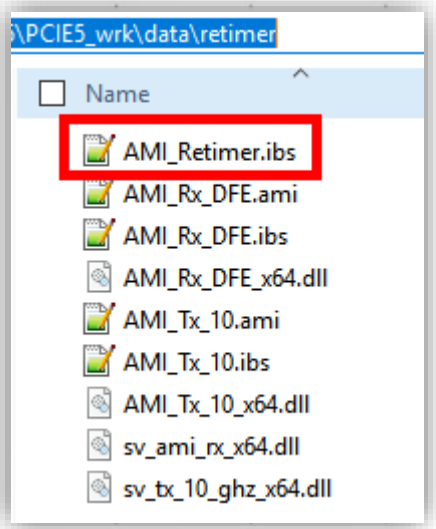
After RX EQ



Add Retimer in the Middle



Retimer Model

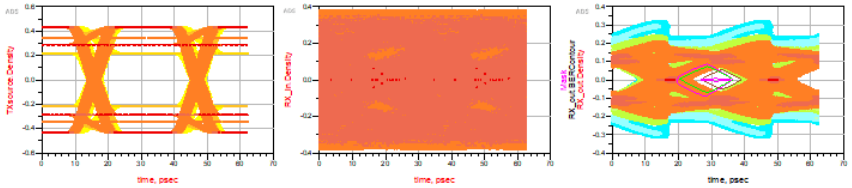


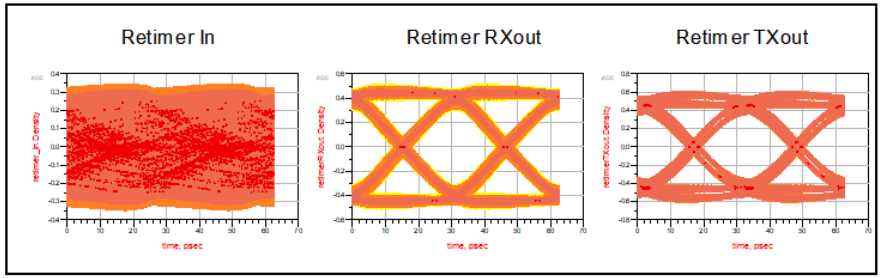

```
29  [Model] AMI_Rx_DFE
30  Model_type Input
31
32  C_comp 0p 0p 0p
33  Vinh = 0.25
34  Vinl = -0.25
35
36  [Temperature_Range] 25 125 0
37  [Voltage Range] 1.0 1.0 1.0
38
39  [Algorithmic Model]
40  Executable Windows_cl19.00.24215.1_64 AMI_Rx_DFE_x64.dll AMI_Rx_DFE.ami
41
```

```
54  [Model] AMI_Tx_10
55  Model_type Output
56
57  C_comp 0p 0p 0p
58  Cref = 0
59  Vref = 0.5
60  Rref = 50
61  Vmeas = 0.5
62
63  [Temperature_Range] 25 125 0
64  [Voltage Range] 1.0 1.0 1.0
65
66  [Algorithmic Model]
67  Executable Windows_cl19.00.24215.1_64 AMI_Tx_10_x64.dll AMI_Tx_10.ami
68
```

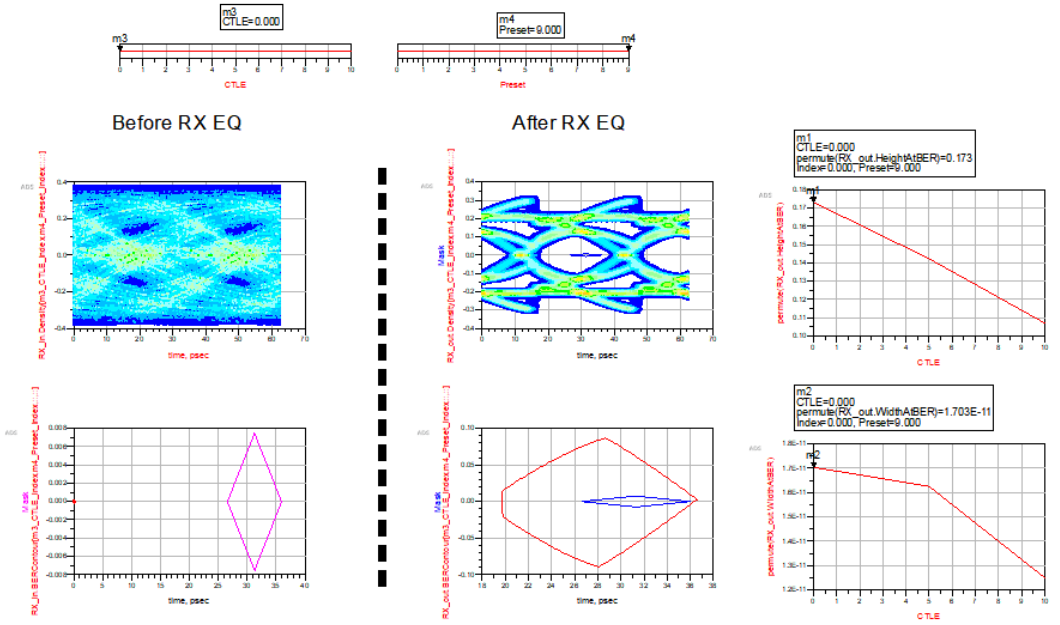
Results (200s, 9 scenarios)

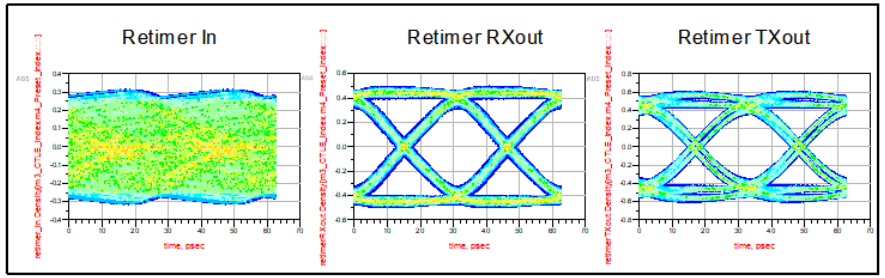
ChannelSim Result





Batched ChannelSim Result





Hand-made Retimer Model

[Bonus] How to create Repeater.ibs File

1. Save Rx .ibs model as Repeater .ibs model
2. Change File name and Component name in .ibs file of repeater model
3. Copy Pin and Diff Pin definition from Tx .ibs model to Repeater .ibs model

```
[IBIS Ver]      5.1
[File Name]     AMI_Tx_10.ibs
[File Rev]      1.0
[Component]     AMI_Tx_10
[Manufacturer] My Company

[Package]

R_pkg  0.0     NA       NA
L_pkg  0.0     NA       NA
C_pkg  0.0     NA       NA

[Pin]     signal_name              model_name        R_pin L_pin  C_pin
1p        AMI_Tx_10_p              AMI_Tx_10
1n        AMI_Tx_10_n              AMI_Tx_10

[Diff_Pin] inv_pin vdiff tdelay_typ tdelay_min tdelay_max
1p        1n             NA     NA     NA     NA
```

2

3

```
[IBIS Ver]      5.1
[File Name]     AMI_Retimer.ibs
[File Rev]      1.0
[Component]     AMI_Retimer
[Manufacturer] My Company

[Package]

R_pkg  0.0     NA       NA
L_pkg  0.0     NA       NA
C_pkg  0.0     NA       NA

[Pin]     signal_name              model_name        R_pin L_pin  C_pin
2p        AMI_Rx_DFE_2p            AMI_Rx_DFE
2n        AMI_Rx_DFE_2n            AMI_Rx_DFE
1p        AMI_Tx_10_p              AMI_Tx_10
1n        AMI_Tx_10_n              AMI_Tx_10

[Diff_Pin] inv_pin vdiff tdelay_typ tdelay_min tdelay_max
2p        2n             NA     NA     NA     NA
1p        1n             NA     NA     NA     NA
```

.ibs model of Tx

.ibs model of Redriver

[Bonus] How to create Repeater.ibs File

4. Copy the remaining Tx part to Redriver .ibs file after definition of Rx model and before the '[END]' command.

```
[Model] AMI_Tx_10
Model_type Output

C_comp 0p 0p 0p
Cref = 0
Vref = 0.5
Rref = 50
Vmeas = 0.5

[Temperature_Range] 25 125 0
[Voltage Range] 1.0 1.0 1.0

[Algorithmic Model]
Executable Windows_cl19.00.24215.1_64 AMI_Tx_10_x64.dll AMI_Tx_10.ami

[End Algorithmic Model]

[Pulldown]
-6.6              -0.132            -0.132            -0.132
 0.0              0.0               0.0               0.0
 6.6              0.132             0.132             0.132

[Pullup]
-6.6              0.132             0.132             0.132
 0.0              0.0               0.0               0.0
 6.6              -0.132            -0.132            -0.132

[GND Clamp]
-6.6              0.0               0.0               0.0
 0.0              0.0               0.0               0.0
 6.6              0.0               0.0               0.0

[Power Clamp]
-6.6              0.0               0.0               0.0
 0.0              0.0               0.0               0.0
 6.6              0.0               0.0               0.0

[Ramp]
dV/dt_r 0.3/1.5p 0.3/1.5p 0.3/1.5p
dV/dt_f 0.3/1.5p 0.3/1.5p 0.3/1.5p

[END]
```

.ibs model of Tx

4

```
-6.6              0.132e-9          0.0               0.0
 0.0              0.0               0.0               0.0
 6.6              -0.132e-9         0.0               0.0

[Model] AMI_Tx_10
Model_type Output

C_comp 0p 0p 0p
Cref = 0
Vref = 0.5
Rref = 50
Vmeas = 0.5

[Temperature_Range] 25 125 0
[Voltage Range] 1.0 1.0 1.0

[Algorithmic Model]
Executable Windows_cl19.00.24215.1_64 AMI_Tx_10_x64.dll AMI_Tx_10.ami

[End Algorithmic Model]

[Pulldown]
-6.6              -0.132            -0.132            -0.132
 0.0              0.0               0.0               0.0
 6.6              0.132             0.132             0.132

[Pullup]
-6.6              0.132             0.132             0.132
 0.0              0.0               0.0               0.0
 6.6              -0.132            -0.132            -0.132

[GND Clamp]
-6.6              0.0               0.0               0.0
 0.0              0.0               0.0               0.0
 6.6              0.0               0.0               0.0

[Power Clamp]
-6.6              0.0               0.0               0.0
 0.0              0.0               0.0               0.0
 6.6              0.0               0.0               0.0

[Ramp]
dV/dt_r 0.3/1.5p 0.3/1.5p 0.3/1.5p
dV/dt_f 0.3/1.5p 0.3/1.5p 0.3/1.5p

[END]
```

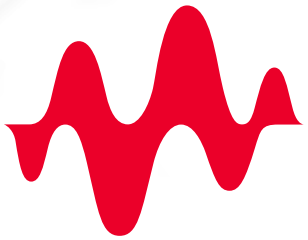
.ibs model of Redriver

Summary

- ADS provides a platform to validate your PCIe Gen5 design, and it can be done by
  - Implementing JEDEC PCIe Gen5 specification by ADS generic TX/RX model.
  - Simply using Gen5 AMI models provided by Keysight.
- Repeater will be widely used in PCIe Gen5 and beyond to make impossible possible.
- Batch Simulator can help gain insight among your system configurations.

Reference

- https://community.keysight.com/thread/27162
- https://www.keysight.com/upload/cmc_upload/All/PCI-Express5-Specification-and-latest-information-of-Gen4-testing.pdf?fbclid=IwAR3OtS4q7yPt7mnj2SuXq7mBc4OmK1AMhIM1py19pAQylGJXFWCg9_jN-FU
- https://www.keysight.com/sg/en/assets/7018-03143/application-notes/5990-9111.pdf?success=true



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