

Optical and Electrical 400G Network Test Overview

400G高速傳輸之光電測試及驗證方案

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Agenda

- **High Speed Network Overview**
- FAQ
- 400G Network Test discussion
- Sampling Scope And CDR Basic

Standards covering data center networking

SEVERAL CLASSES WITH MULTIPLE STANDARDS IN EACH

CEI (Common Electrical Interface) -- Optical Internetworking Forum (We are member)

- Electrical link – chip to chip, chip to module, backplane, cables
- Each standard covers a narrow range of data rates
- Base standards that Ethernet, Fibre Channel, and InfiniBand are built on



Ethernet – IEEE 802.3xx (We are member)

- Electrical and optical links between equipment, backplanes and cables
- Finishing 100G class, starting on 400G



Fibre Channel -- Fibre Channel Industry Association (We are member)

- Optical links between data center equipment
- Completed 32GFC, working on 128G (4x32), next project : 64GFC



InfiniBand -- InfiniBand Trade Association

- Electrical and optical links between supercomputing equipment
- Finishing 300G (12x25G), working on 600G (12x50G)



IEEE 802.3 History

Ethernet standard	Date	Description
802.3	1983	<u>10BASE5</u> 10 Mbit/s (1.25 MB/s) over thick coax..
802.3i	1990	<u>10BASE-T</u> 10 Mbit/s (1.25 MB/s) over twisted pair
802.3u	1995	<u>100BASE-TX</u> , <u>100BASE-T4</u> , <u>100BASE-FX</u> Fast Ethernet at 100 Mbit/s (12.5 MB/s) with <u>auto-negotiation</u>
802.3ab	1999	<u>1000BASE-T</u> Gbit/s Ethernet over twisted pair at 1 Gbit/s (125 MB/s)
802.3ae	2002	<u>10 Gigabit Ethernet</u> over fiber; 10GBASE-SR, 10GBASE-LR, 10GBASE-ER, 10GBASE-SW, 10GBASE-LW, 10GBASE-EW
802.3af	2003	<u>Power over Ethernet</u> (15.4 W)
802.3an	2006	<u>10GBASE-T</u> 10 Gbit/s (1,250 MB/s) Ethernet over unshielded twisted pair (UTP)
802.3az	2010	<u>Energy-Efficient Ethernet</u>
802.3ba	2010	40 Gbit/s and 100 Gbit/s Ethernet.
802.3bp	2016	1000BASE-T1 – Gigabit Ethernet over a single twisted pair, automotive & industrial environments
802.3bs	2017	<u>200GbE</u> (200 Gbit/s) over single-mode fiber and <u>400GbE</u> (400 Gbit/s) over optical physical media
802.3bz	2016	<u>2.5GBASE-T</u> and <u>5GBASE-T</u> – 2.5 Gigabit and 5 Gigabit Ethernet over <u>Cat-5/Cat-6</u> twisted pair
802.3cd	2018	Media Access Control Parameters for 50 Gbit/s and Physical Layers and Management Parameters for 50, 100, and 200 Gbit/s Operation

IEEE 802.3 History (Cont.)

Ethernet standard	Date	Description
802.3-1998	1998	(802.3aa) A revision of base standard incorporating the above amendments and errata
802.3-2002	2002	(802.3ag) A revision of base standard incorporating the three prior amendments and errata
802.3-2005	2005	(802.3am) A revision of base standard incorporating the four prior amendments and errata.
802.3-2008	2008	(802.3ay) A revision of base standard incorporating the 802.3an/ap/aq/as amendments, two corrigenda and errata.
802.3-2012	2012	(802.3bh) A revision of base standard incorporating the 802.3at/av/az/ba/bc/bd/bf/bg amendments, a corrigenda and errata.
802.3-2015	2015	802.3bx – a new consolidated revision of the 802.3 standard including amendments 802.3bk/bj/bm
802.3-2018	2018	802.3cj – 802.3-2015 maintenance, merge recent amendments bn/bp/bq/br/bs/bw/bu/bv/by/bz/cc/ce

Ethernet Naming Convention

Optical:

S : MMF 100m

D : SMF 500m

F : SMF 2km

L : SMF 10km

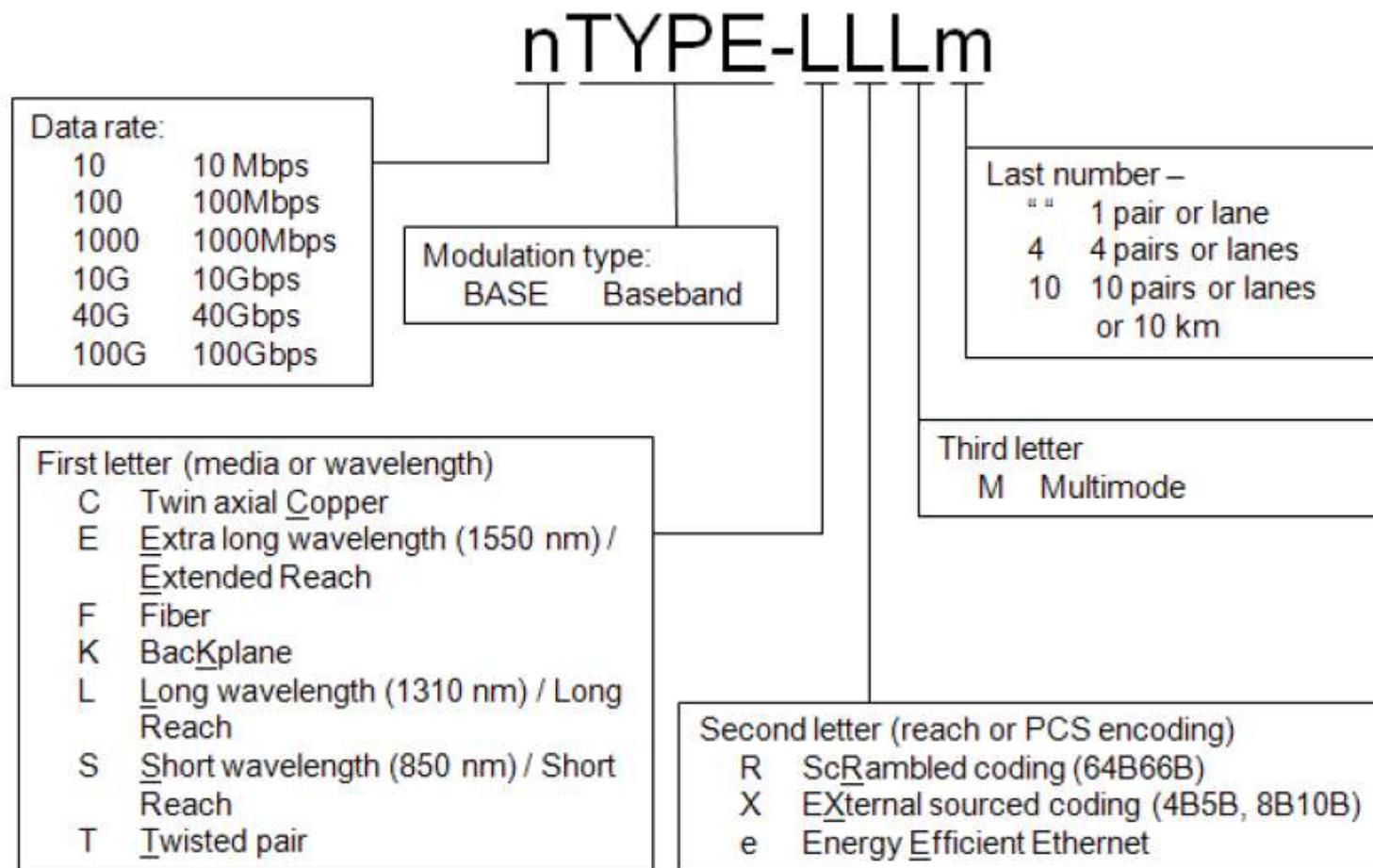
E : SMF 40km

Electrical:

C : Copper 5~7m

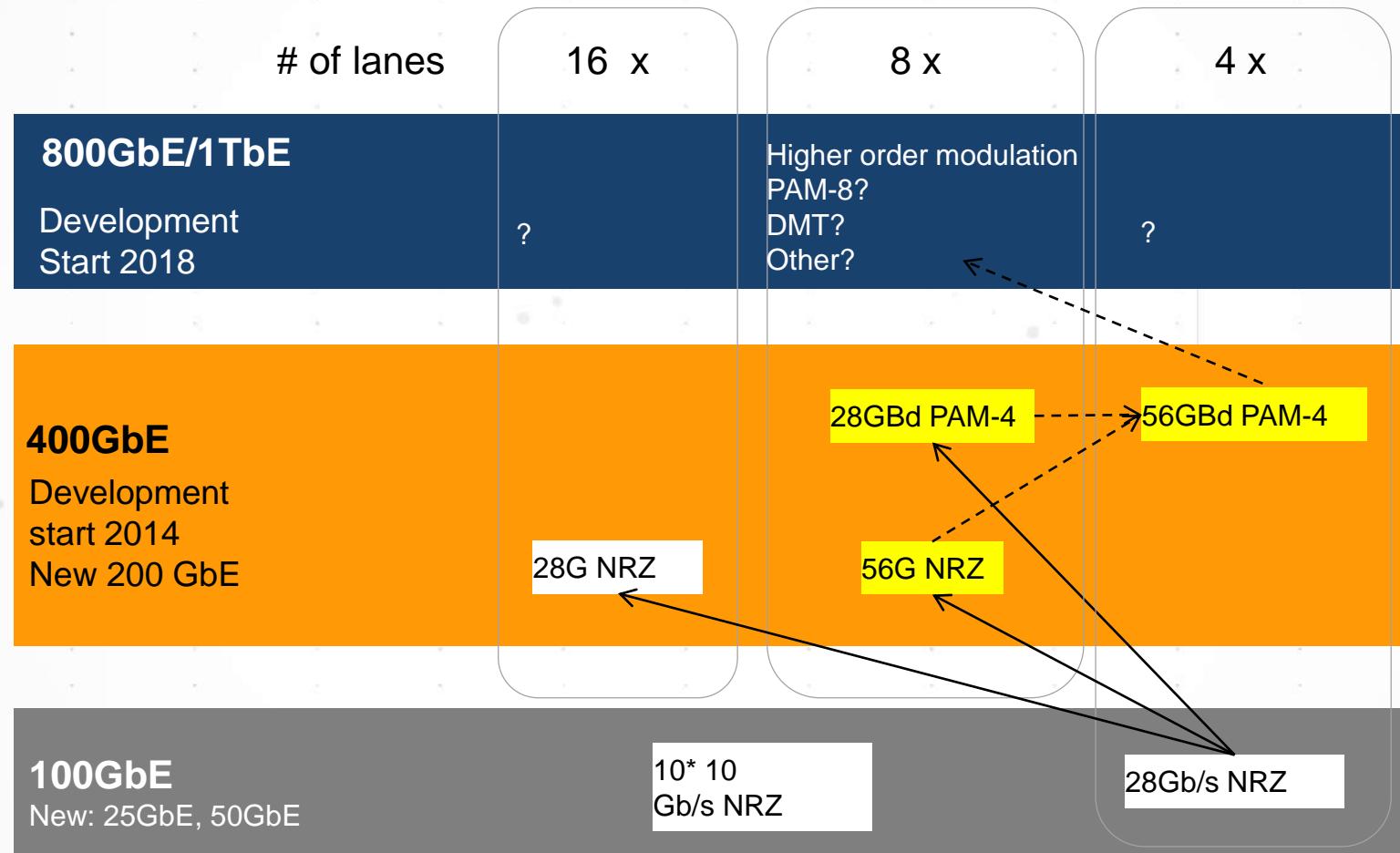
K : Backplane

T : Twist Pair

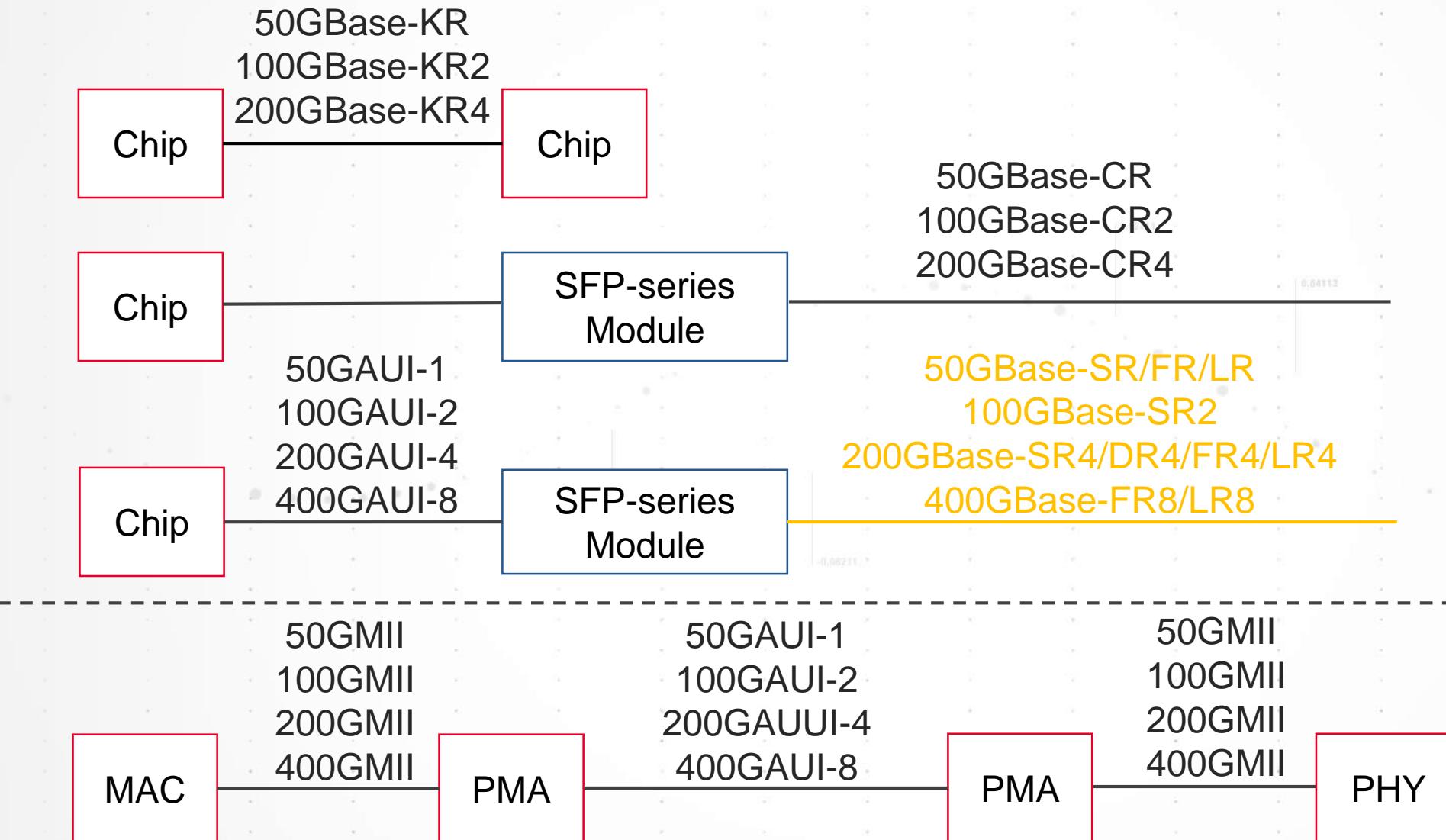


Data Center Standards

MOVING FROM 100G TO 400G - MORE VARIANTS



25G x 1/2/4/8 Lane (PAM4)



PAM4 50/100/200/400G Summary

Name	Clause	Baud	Lanes	Signaling rate per lane	Modulation	Note
200GBase-DR4	121	200	4	26.5625	PAM-4	802.3bs
200GBase-FR4	122	200	4	26.5625		
200GBase-LR4	122	200	4	26.5625		
400GBase-FR8	122	400	8	26.5625		
400GBase-LR8	122	400	8	26.5625		
400GBase-SR16	123	400	16	26.5625		
400GBase-DR4	124	400	4	53.125		
50/100/200GBase-CRx	P136	50/100/200	1/2/4	26.5625	PAM-4	802.3cd
50/100/200GBase-KRx	P137	50/100/200	1/2/4	26.5625		
50/100/200GBase-SRx	P138	50/100/200	1/2/4	26.5625		
50GBase-FR/LR	P139	50	1	26.5625		
100GBase-DR	P140	100	1	53.125		

nPPI/AUI Summary

Name	Clause	Baud	Lanes	Signaling rate per Lane	Modulation	Note
XLAUI C2C/C2M	83A/B	40	4	10.3125	NRZ	802.3bs
CAUI-10 C2C/C2M	83A/B	100	10	10.3125		
CAUI-4 C2C/C2M	83D/E	100	4	25.78125		
XLPPI	86A	40	4	10.3125		
CPPI	86A	100	10	10.3125		
200GAUI-8 C2C/C2M	120B/C	200	8	26.5625		
400GAUI-16 C2C/C2M	120B/C	400	16	26.5625	PAM-4	802.3cd
200GAUI-4 C2C/C2M	120D/E	200	4	26.5625		
400GAUI-8 C2C/C2M	120D/E	400	8	26.5625		
50GAUI-1 C2C/C2M	P135D/E	50	1	26.5625		
100GAUI-2 C2C/C2M	P135D/E	100	2	26.5625	NRZ	802.3cd
50GAUI-2 C2C/C2M	P135F/G	50	2	26.5625		
100GAUI-4 C2C/C2M	P135F/G	100	4	26.5625		
LAUI-2 C2C/C2M	P135B/C	50	2	25.78125		

P802.3cd Summary

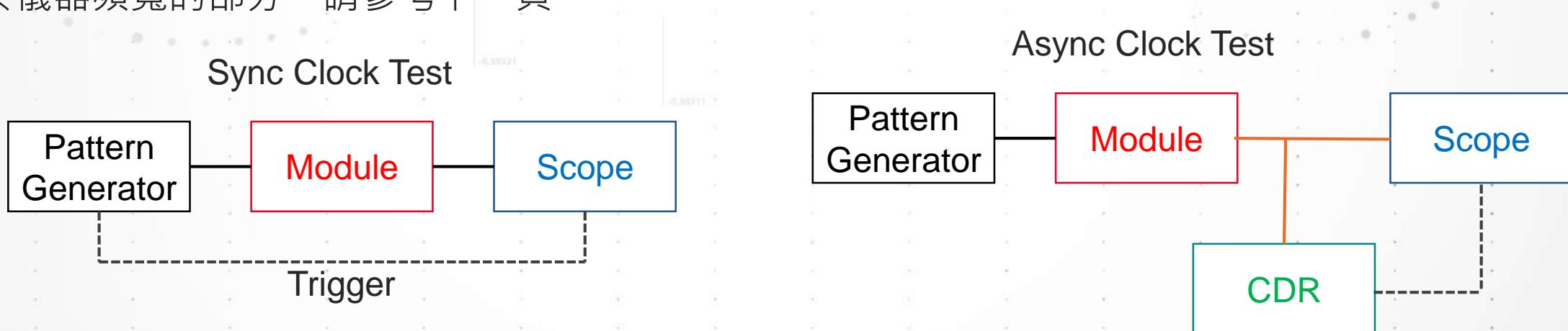
Name	Clause	Baud	Lanes	Signaling rate per lane	Modulation	Note
50GBase-CR	P136	50	1	26.5625	PAM-4	
100GBase-CR2	P136	100	2	26.5625		
200GBase-CR4	P136	200	4	26.5625		
50GBase-KR	P137	50	1	26.5625		
100GBase-KR2	P137	100	2	26.5625		
200GBase-KR4	P137	200	4	26.5625		
50GBase-SR	P138	50	1	26.5625		
100GBase-SR2	P138	100	2	26.5625		
200GBase-SR4	P138	200	4	26.5625		
50GBase-FR	P139	50	1	26.5625		
50GBase-LR	P139	50	1	26.5625		
100GBase-DR	P140	100	1	53.125		
50GAUI-1 C2C/C2M	P135D/E	50	1	26.5625		
100GAUI-2 C2C/C2M	P135D/E	100	2	26.5625		
50GAUI-2 C2C/C2M	P135F/G	50	2	26.5625	NRZ	
100GAUI-4 C2C/C2M	P135F/G	100	4	26.5625		
LAUI-2 C2C/C2M	P135B/C	50	2	25.78125		

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Q: 400G 的測試跟過往的 100G 有什麼主要的不同？

- 第一個主要的差異是 PAM4 的使用，這讓測試增加一些測項，而對儀器的影響就是必須加買 PAM4 相關的 Option。
- 第二個主要差異發生在 CDR 的使用。對於系統廠來說，一直以來的測試都必須要 CDR，所以變化不大，只要確認速率夠用即可。但對於模組廠來說就影響比較大了。因為 100G 之前的模組測試架構上，並不需要 CDR。但到了 400G 之後，因為模組內部很多都採用 DSP 架構，有很大的機會讓模組的輸入與輸出之間速率不同步，因此就必須加買 CDR。
- 至於儀器頻寬的部分，請參考下一頁。



Q: 400G 測試需要多少頻寬的示波器？

- 事實上，400G 只是總資料頻寬，真正影響到示波器頻寬的是 Baud per lane。以 400G-FR8 為例子，它達成 400G 方式是 $25\text{G} \times 2 (\text{PAM4}) \times 8 (\text{Lanes}) = 400$ 。也就是他實際上 Baud per lane 只有 25G，所以在談示波器頻寬的時候，是看這個 25G 來判斷，跟 400G 沒有直接關係，所以測 100G 的設備繼續沿用在 400G 測試是有可能的。

		IEEE	OIF-CEI
	Electrical	Optical	Electrical
<i>Used by 100G</i>	25~28G NRZ	33 GHz	12.6 GHz
<i>Used by 200G/400G now</i>	25~28G PAM4	33 GHz	13.28125 GHz
	53~56G NRZ	-----	-----
<i>Used by 200G/400G next gen</i>	53~56G PAM4	-----	26.5625 GHz
			43 GHz

Q: 為什麼是 25 ~ 28 / 53 ~ 56 GBaud 而非定值？

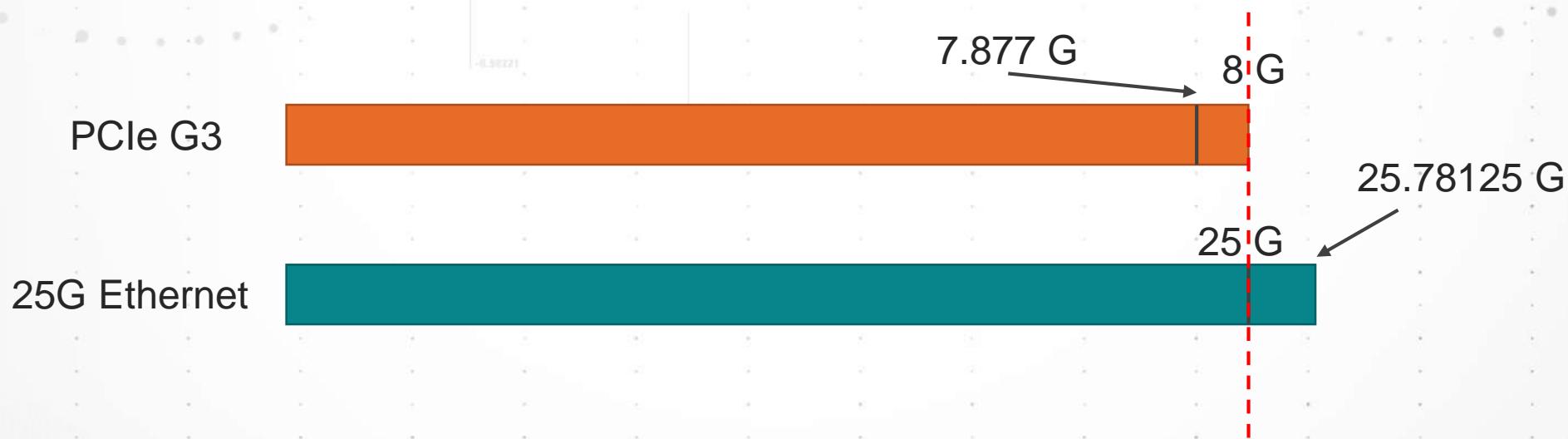
- 在網路通訊的世界，OIF 協會都是走最快的。他會先訂出 CEI 這份標準，其中速率的部分訂一個範圍，讓後面的協會可以自由地根據編碼的形式來選擇最適當的速率。以 IEEE 為例，在 NRZ 的訊號使用 64/66b coding，所以最後的真實速率是：

$$25G \times (66/64) = 25.78125$$

- 而 IEEE PAM4 coding 改為 256/257b，又引入了 RS-FEC 的 coding，所以速率最後變成了

$$25G \times (257/256) \times (544/514) = 26.5625$$

- 所以網路世界的規格跟其他高速數位標準很不同的地方是，他的宣稱速率是不包含 coding overhead 的。



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Transmitter Characterization

OPTICAL TX TEST

Patterns

TEST PATTERNS FOR PAM4 ENCODED SIGNALS DEFINED IN IEEE 802.3BS/CD

- **JP03A** - The JP03A test pattern is a repeating {0,3} sequence (clock)
– [No longer used in 802.3bs/cd](#).
- **JP03B** - The JP03B test pattern is a repeating sequence of {0,3} repeated 15 times followed by {3,0} repeated 16 times (clock with a phase shift)
- [No longer used in 802.3bs/cd](#)
- **PRBS13Q** - The PRBS13Q test pattern is a repeating 8191-symbol sequence formed by Gray coding pairs of bits from two repetitions of the PRBS13 pattern into PAM4 symbols as described in 120.5.7. (Note: PRBS13Q is different from QPRBS13 defined in IEEE 802.3-2015 (bj) Clause 94). Used for victim channel in TX tests.
- **PRBS31Q** - The PRBS31Q test pattern is a repeating $2^{31}-1$ symbol sequence formed by Gray coding pairs of bits from two repetitions of the PRBS31 pattern defined in 49.2.8 into PAM4 symbols as described in 120.5.7. Used for victim channel in RX tests and aggressor lanes in TX/RX tests.
- **SSPRQ** – Short Stress Pattern Random Quaternary.
The SSPRQ pattern is a repeating $2^{16}-1$ PAM4 symbol sequence. Comprised of 4 sequences, each based key “stressors” from PRBS31. Stressful pattern, but short enough to use advanced analysis tools available on today’s T&M tools (e.g. Equalization, Jitter/Noise analysis, etc.). Used for Optical TX test.

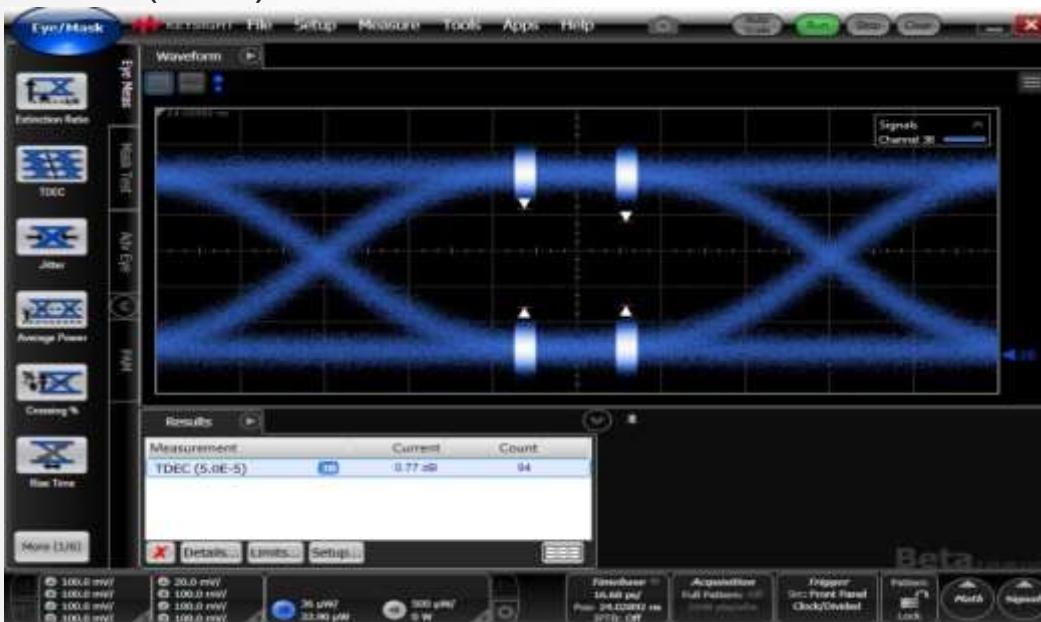
PAM4 Test Patterns		
Pattern	Pattern Description	Defined in Clause
Square Wave	Square wave (8 threes, 8 zeros)	120.5.11.2.4
3	PRBS31Q	120.5.11.2.2
4	PRBS13Q	120.5.11.2.1
5	Scrambled Idle	119.2.4.9
6	SSPRQ	120.5.11.2.3

Optical Measurement Differences: NRZ vs PAM4

USE OF FORWARD ERROR CORRECTION (FEC) RESULTS IN MAJOR CHANGES TO TX TEST

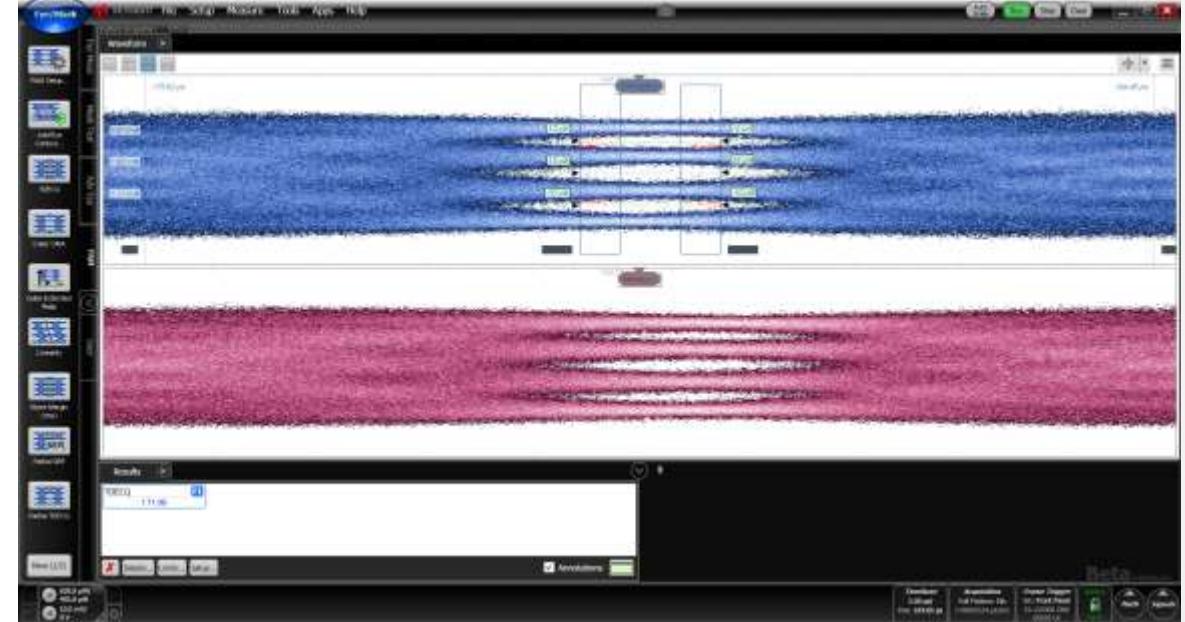
- Primary NRZ transmitter tests:

- OMA (optical modulation amplitude)
- Extinction Ratio (ER)
- Eye-mask
- NEW!: Transmitter Dispersion and Eye Closure (TDEC) replaces Transmitter Dispersion Penalty (TDP) for new 25G and 50G TX



- Primary PAM4 transmitter tests:

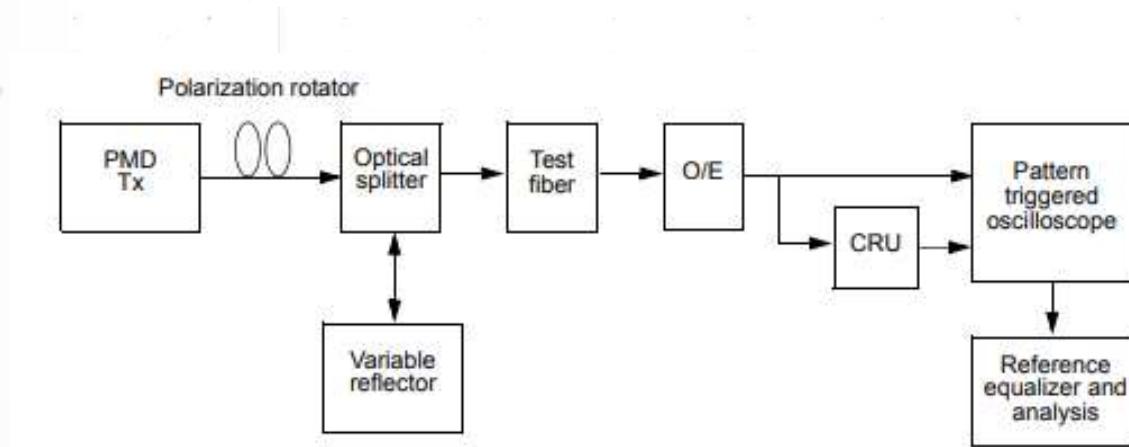
- Outer OMA
- Outer Extinction Ratio
- NEW!: No eye-mask
- NEW!: TDECQ replaces TDP
- NEW! Transition Time (IEEE 802.3cd)



TDECQ

TRANSMITTER DISPERSION AND EYE CLOSURE QUaternary

- Tells you the performance of your transmitter relative to an ideal transmitter
- For NRZ TDP, we literally used a BERT to measure the BER performance of the transmitter compared to an actual (real) golden transmitter
 - Determine how much extra power was required at the receiver to compensate for non-ideal performance
- For TDECQ we indirectly measure SER (symbol error rate) using a scope, no BERT required.



Reference: IEEE P802.3bs™/D3.5, 10th October 2017, Figure 121-4, page 222.

TDECQ measurement process (from IEEE 802.3bs)

- SSPRQ test pattern (~ 2^{16} length)
(Short Stress Pattern Repetitive Quaternary)
- Includes test fiber dispersion
- Oscilloscope noise measured and mathematically ‘backed out’
- Virtual 5 tap, T spaced FFE reference equalizer optimizes eye openings (to minimize TDECQ penalty).
- Histograms constructed to assess eye closure relative to OMA and **compute an effective power penalty in dB. This is the TDECQ result**

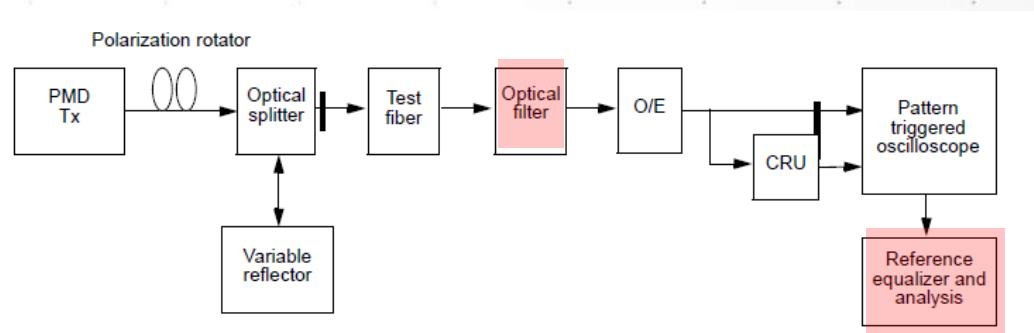


Figure 122-4—TDECQ conformance test block diagram

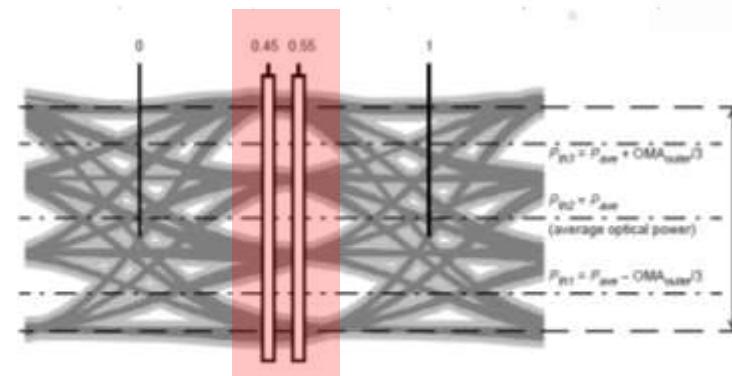
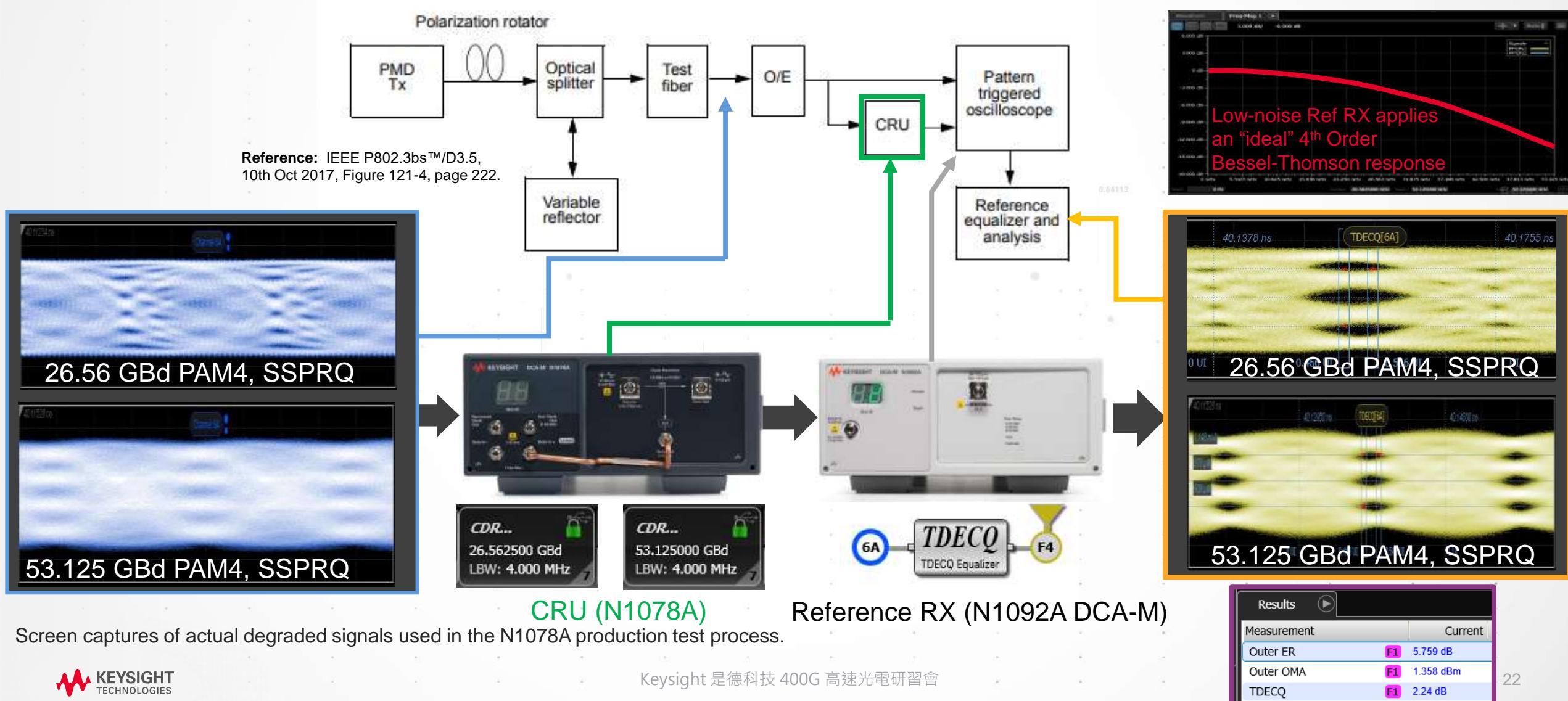


Figure 121-5—Illustration of the TDECQ measurement

Reference: IEEE P802.3bs™/D3.5, 10th October 2017, Figure 121-5, page 222, 224.

TDECQ Measurement Setup

REQUIRES ACCURATE OPTICAL REF RX AND ROBUST CLOCK RECOVERY DESIGN

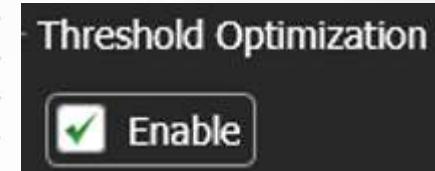


TDECQ: Measurement Tips

CHOOSE A MEASUREMENT SOLUTION THAT IS FAST, FLEXIBLE, AND ACCURATE

- **Compliant TDECQ measurements require:**

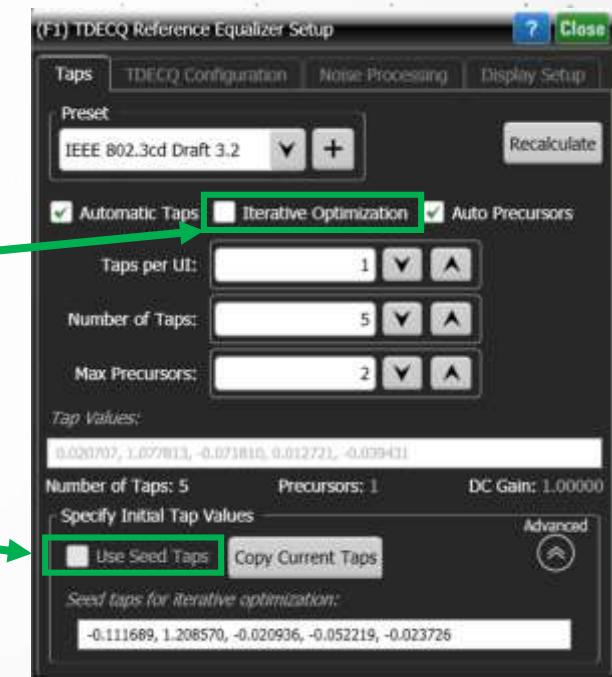
- **Histogram optimization** (adjust left and right)
(IEEE 802.3bs D3.5, IEEE802.3cd D3.2)
- **Threshold optimization** (adjust up and down)
(IEEE 802.3cd D3.4, likely will be added to 802.3bs in a maintenance release)



- **Recommendation:** keep these **enabled at all times** (they have a minimal impact on throughput, but can have a large impact on result).

- **Recommendations for throughput optimization:**

- Iterative “tap” optimization – typically results in a 0.1dB to 0.2dB difference in TDECQ (signal dependent). Consider disabling this feature to increase throughput (e.g. in production test).
- “Seed” equalizer tap values for faster tap optimization
- Consider using a more powerful CPU to perform your TDECQ measurements, especially for parallel TDECQ testing (4 channels)



TDECQ: Does it work as designed?

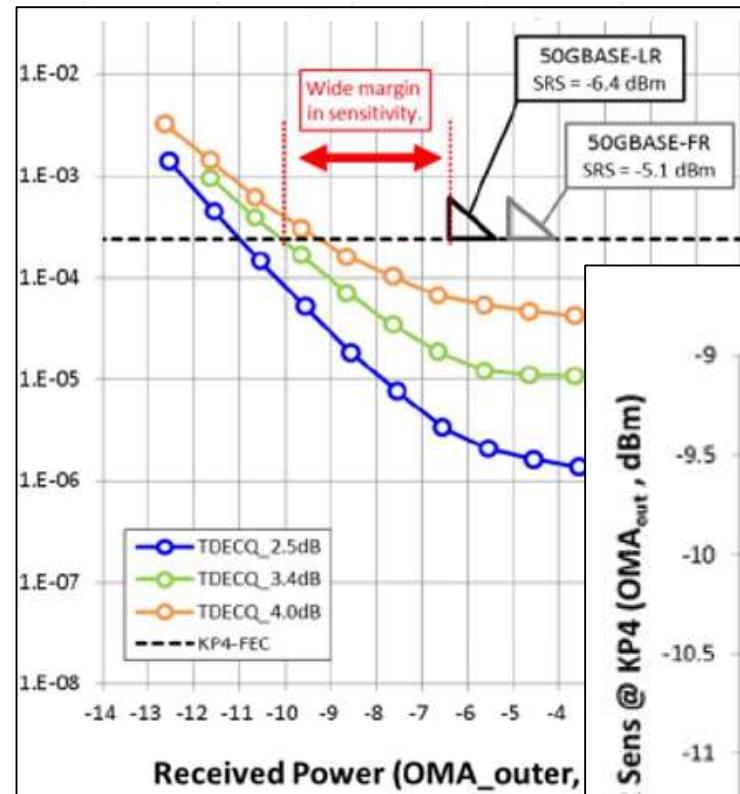
POWER PENALTY VALUES PROVIDED BY THE FINAL IMPLEMENTATION OF TDECQ CORRELATE DIRECTLY TO OBSERVED RECEIVER SENSITIVITY

Consider a typical PAM4 receiver and two transmitters A and B. If the TDECQ of transmitter A is 2 dB and for transmitter B is 3.2 dB, should I be able to make any predictions about the power levels required at the receiver to achieve a specific BER/SER with each transmitter?

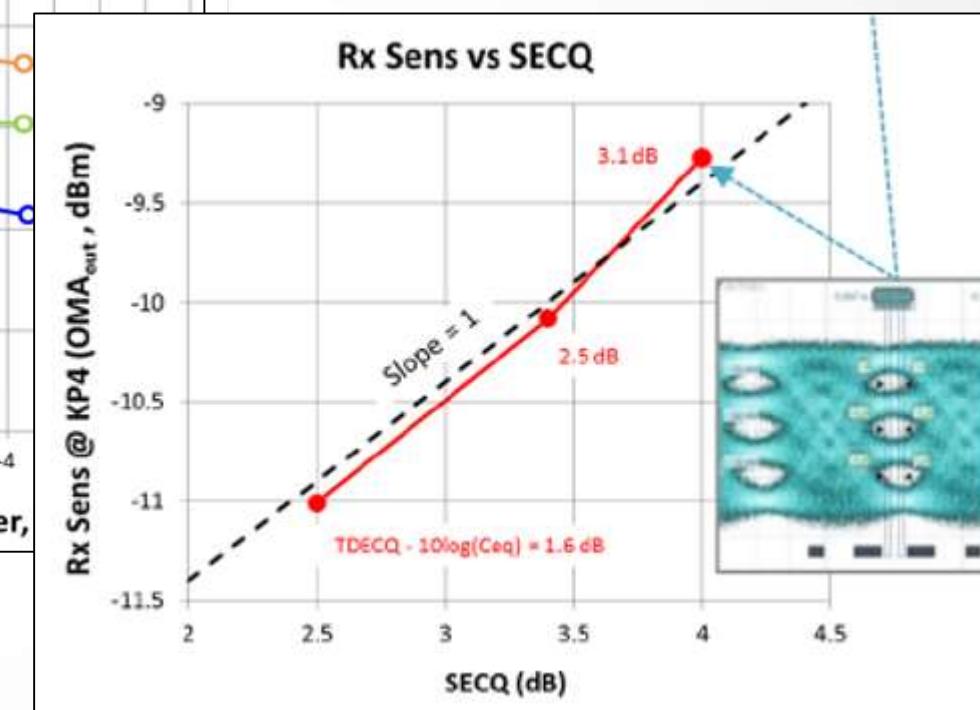
Latest results from IEEE 802.3cd project:

http://grouper.ieee.org/groups/802/3/cd/public/July18/tamura_3cd_01c_0718.pdf

(used with permission from the author)



As the TDECQ receiver definition was refined, excellent correlation is seen with real transceivers.



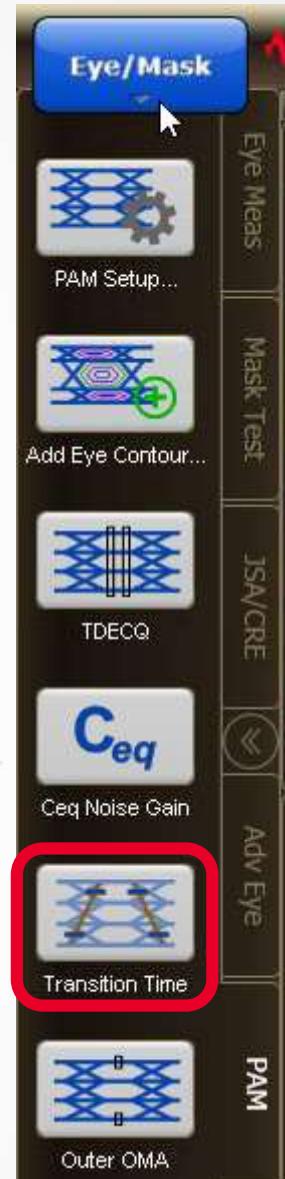
Transmitter Transition Time for Optical PAM4

NEW MEASUREMENTS ADDED TO IEEE 802.3CD

Transmitter transition time is defined as the **slower** of the time interval of the rising/falling transitions of a PAM4 signal.

Test Conditions:

- 20% to 80% of Outer OMA levels
- Measured with Square Wave or SSPRQ pattern.
 - SSPRQ: Use specific symbol sequences
 - 0000033333 (rise time)
 - 33333000000 (fall time)
 - Measured with specific Ref RX BW and 4th Order BT response

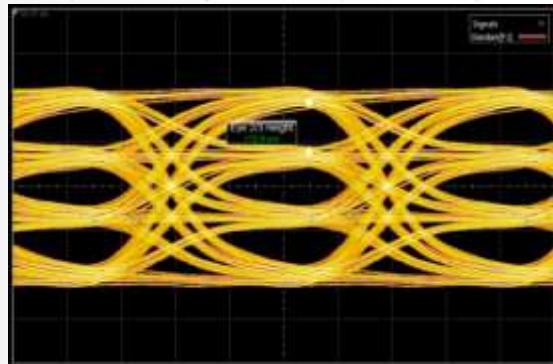


Transmitter Characterization

ELECTRICAL TX TEST

Key PAM4 Measurements for Electrical Transmitters

IEEE 802.3BS & CD



What are the key PAM-4 TX parameters that get measured?

- **xAUI C2C (TP0a) & CR (TP2)**
 - Level Separation Mismatch Ratio
 - Steady State Voltage
 - Linear Fit Pulse Peak
 - Signal-to-noise-and-distortion ratio (SNDR)
 - J4u, Even-Odd Jitter (EOJ)

- **xAUI C2M (TP1a)**
 - ESMW
 - Vertical Eye Closure (VEC)

C2C v.s. C2M

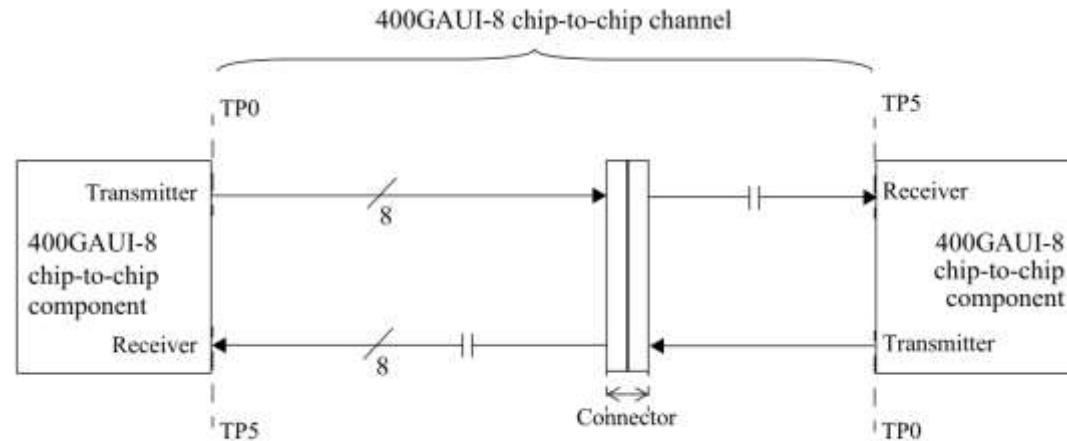
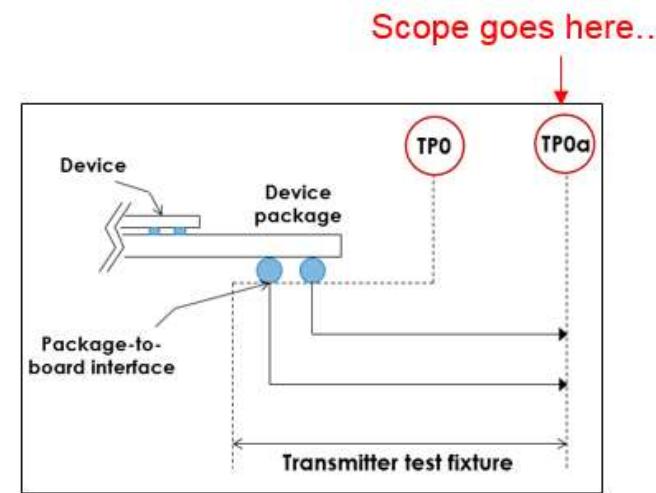


Figure 120D-4—Typical 400GAUI-8 chip-to-chip application



Transmitter compliance measured at TP0a

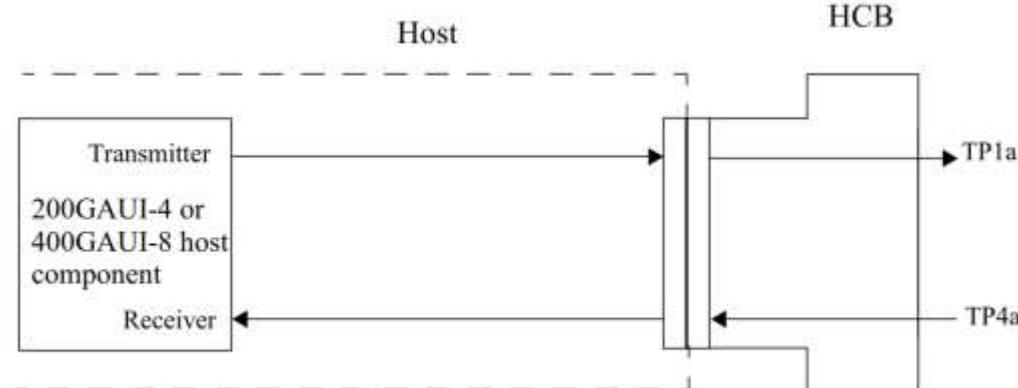


Figure 120E-5—Host 200GAUI-4 or 400GAUI-8 C2M compliance points

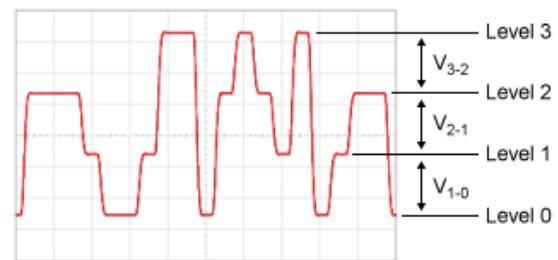
Level separation mismatch ratio (R_{LM})

- PAM *Linearity* measures the linearity R_{LM} (Ratio Level Mismatch) of all four amplitude levels (0, 1, 2, 3) of a PAM4 signal. Linearity is a measure of the variance in amplitude separation (distribution) between the different PAM4 levels. The PAM4 signal must be displayed as a single-valued waveform and all four logic levels should be visible on the display.

Examples of PAM Signal Linearity

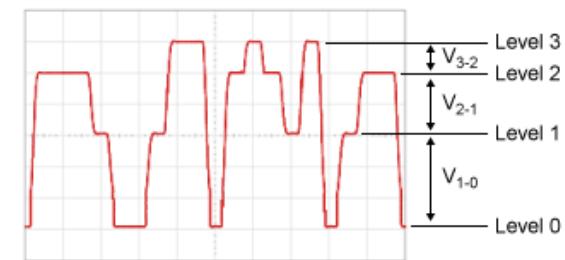
Good Linearity

$$V_{3-2} = V_{2-1} = V_{1-0}$$



Poor Linearity

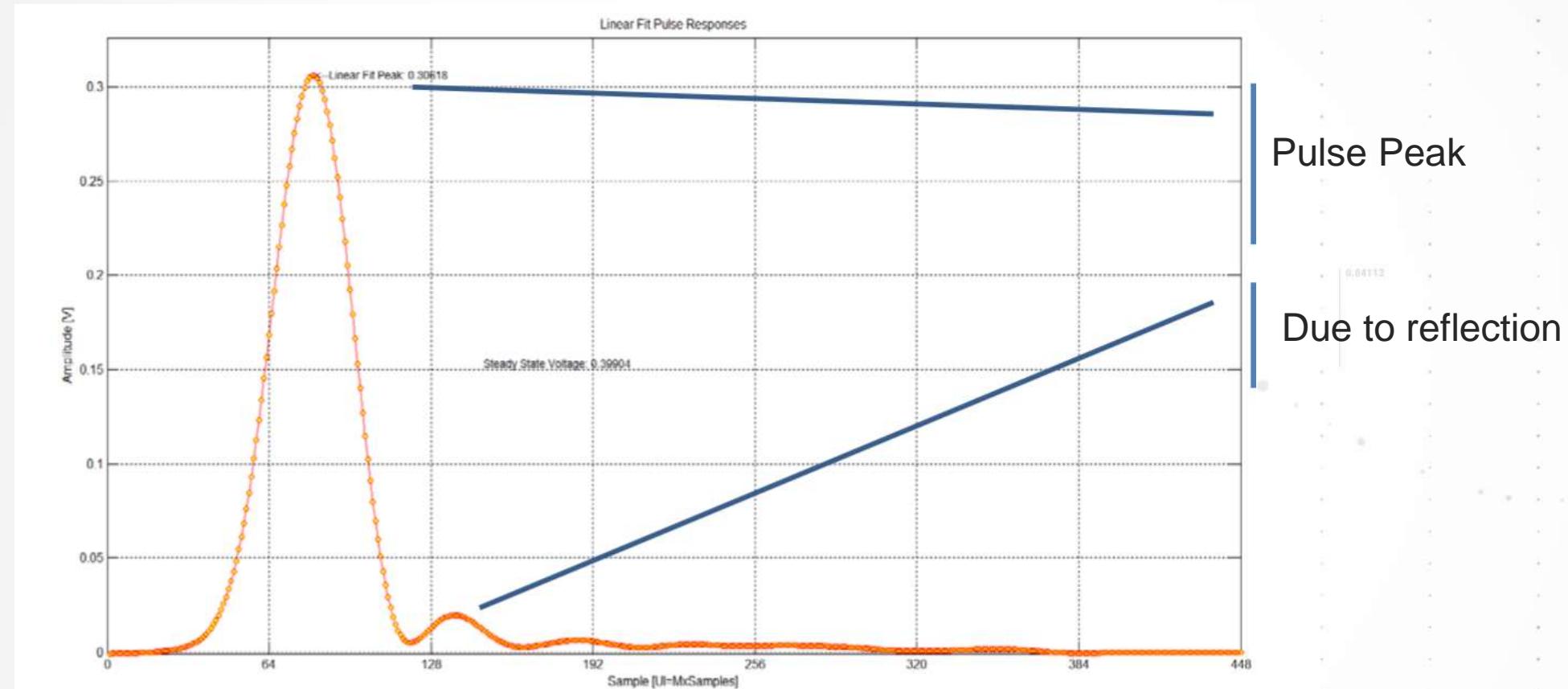
$$V_{3-2} \neq V_{2-1} \neq V_{1-0}$$



Linearity (RLM) = $\frac{\text{smallest separation between adjacent levels}}{\text{ideal separation}}$

$$\text{Linearity (RLM)} = \frac{\min(V_3 - V_2, V_2 - V_1, V_1 - V_0)}{\frac{V_3 - V_0}{3}}$$

Linear fit pulse peak and Steady State Voltage



The waveform shall be captured with an effective sample rate that is M times the signaling rate of the transmitter under test. The value of M shall be an integer not less than 7. **The steady-state voltage v_f is defined to be the sum of the linear fit pulse $p(k)$ divided by M.**

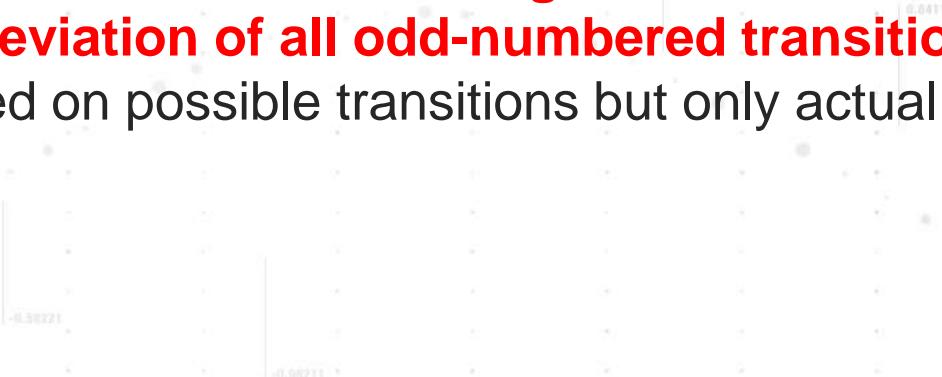
SNDR

- In an SNDR model, the degree that the actual pulse response matches a linear fit model is the main consideration. The ISI jitter/noise is 100% compensable by equalizers and of no real consequence to the system performance (assuming the equalizers can be implemented in the system). The residue from the linear fit is called distortion. The ratio between the signal from linear fit and distortion-plus-noise projects the system performance with equalizers. **The standard deviation of the error in this model fit is called distortion, the s_e parameter in the SNDR expression.** For each of the four symbol levels, the vertical signal noise is determined at a fixed low-slope point in a long consecutive run of identical PAM4 symbols. **The noise parameter s_n is the average of the standard deviations of these four symbol measurements. P_{max} is the peak amplitude of the pulse response from the linear fit.**

$$SNDR = 10\log_{10}\left(\frac{P_{max}^2}{\sigma_e^2 + \sigma_n^2}\right)$$

Even-odd Jitter

- Even-odd jitter is measured using two repetitions of a PRBS9 pattern. The deviation of the time of each transition from an ideal clock at the signaling rate is measured. **Even-odd jitter is defined as the magnitude of the difference between the average deviation of all even-numbered transitions and the average deviation of all odd-numbered transitions**, where determining if a transition is even or odd is based on possible transitions but only actual transitions are measured and averaged.



Output Jitter (J3u/J4u, J_{RMS} , and EOJ)

NEW MEASUREMENTS PERFORMED ON 12 SPECIFIC EDGES OF A PRBS13Q PATTERN

- J3u/J4u, J_{RMS} , and Even-Odd Jitter (EOJ)...
you may recognize some of these acronyms from
other (older) Standards
- So they should be pretty straight forward to measure,
right?
- While the IEEE Output Jitter names may sound
familiar, they are measured very differently!
 - Traditional J_n (e.g. J_5 , J_9) and EOJ parameters were
measured using all edges of an NRZ pattern.
 - IEEE 802.3bs/cd now measure J3u (802.3cd) and
 J_{RMS} , and EOJ on 12 specific edges of
a PRBS13Q (PAM4) pattern!

Table 120D-4—PRBS13Q pattern symbols used for jitter measurement

Label	Description	Gray coded PAM4 symbols	Index of first symbol	Index transition begins	Index transition ends	Index of last symbol	Threshold level
REF	Reference for symbol index	3333333	1	—	—	7	—
R03	0 to 3 rise	10000 330	1830	1834	1835	1837	$(V_0+V_3)/2$
F30	3 to 0 fall	23333 001	1269	1273	1274	1276	
R12	1 to 2 rise	0111111 2222221	3638	3644	3645	3651	$(V_1+V_2)/2$
F21	2 to 1 fall	022222 113	1198	1203	1204	1206	
R01	0 to 1 rise	100000 113	6835	6840	6841	6843	$(V_0+V_1)/2$
F10	1 to 0 fall	21111 003	2992	2996	2997	2999	
R23	2 to 3 rise	32222 330	6824	6828	6829	6831	$(V_2+V_3)/2$
F32	3 to 2 fall	033333 2222223	7734	7739	7740	7746	
R02	0 to 2 rise	10000 223	3266	3270	3271	3273	$(V_0+V_2)/2$
F20	2 to 0 fall	122222 0000002	7282	7287	7288	7294	
R13	1 to 3 rise	011111 331	133	138	139	141	$(V_1+V_3)/2$
F31	3 to 1 fall	23333 112	7905	7909	7910	7912	

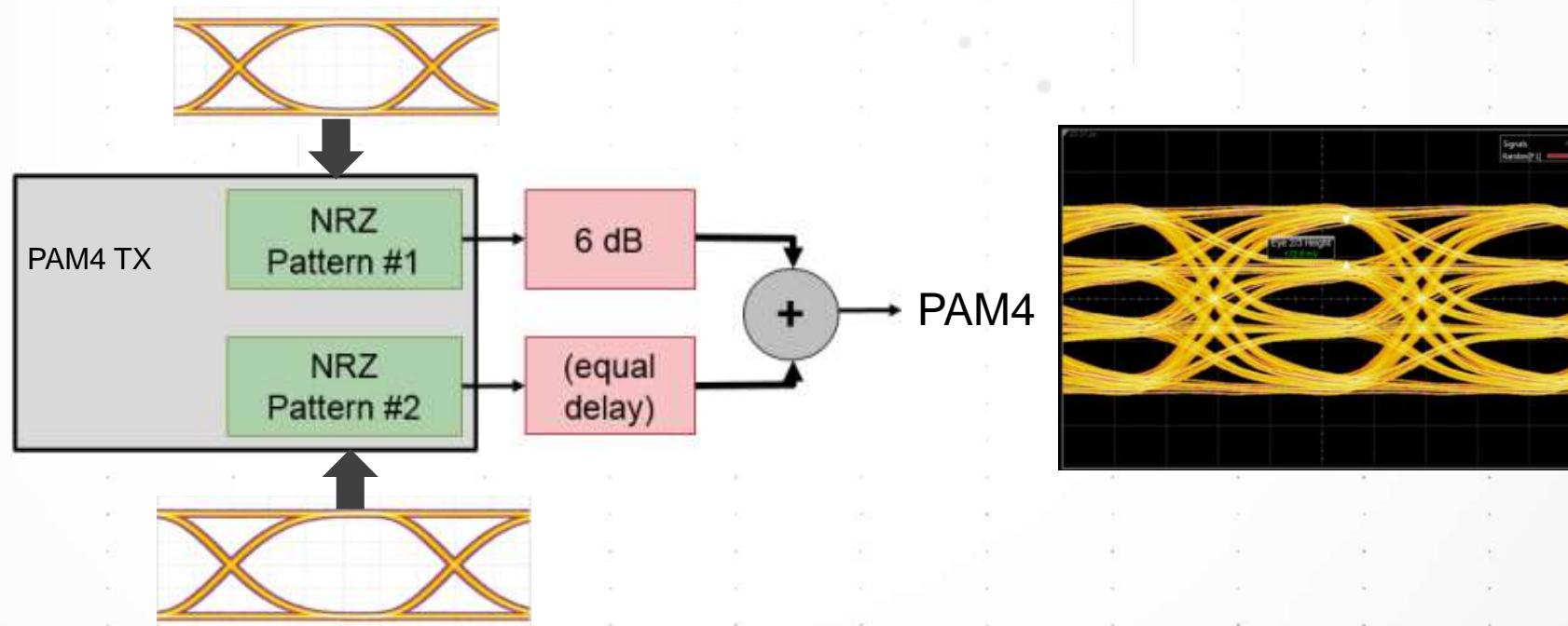
Reference: IEEE P802.3bs™/D3.5, 10th October 2017, page 357.

So don't just pull out your scope and press the J_n (J_2 , J_5 , J_9) or EOJ button in Jitter Mode!

Why did the PAM4 jitter measurement methodology change?

NEW METHOD IMPLEMENTED IN IEEE 802.3BS/CD AND CEI-56G-MR/LR-PAM4

- Different TX Architectures are used to generate PAM4 signals
- Some TX designs may use different clock buffers for MSB and LSB; this can result in different uncorrelated jitter appearing on different edges.
- Measuring jitter only on JP03 (clock) patterns (original method) could miss potential issues.



Measure Output Jitter at TP0a

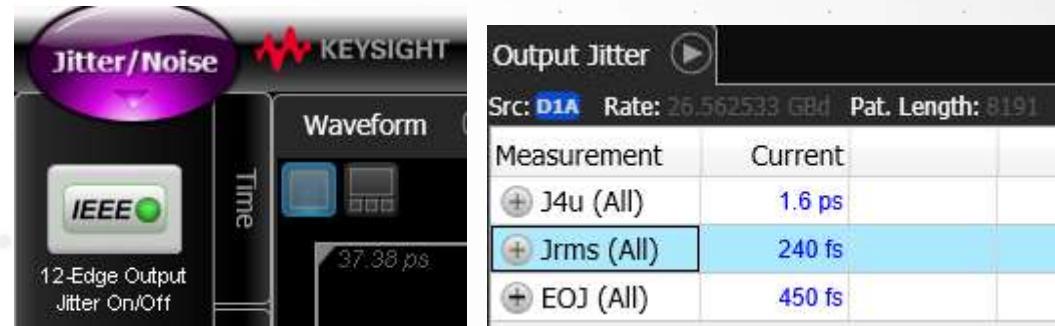
“12-EDGE” OUTPUT JITTER MEASURED ON KEYSIGHT DCA AND RT SCOPES

New “12 edge” jitter method in FlexDCA reduced test time from hours to < 1 minute.

- **J3u/J4u and JRMS jitter**
 - Measure RJ/PJ on 12 specific transitions using a PRBS13Q pattern (exclude correlated jitter).
 - Data from all edges is combined and analyzed
- **Even-Odd Jitter (EOJ)**
 - Measured on PRBS13Q (3 repeats)
 - Max from measurements on all 12 edges
- **Keysight DCA and RT Scopes report:**
 - J3u/J4u, J_{RMS} , EOJ “ALL” measurement (per the Standard)
 - FlexDCA also reports individual results for each of the 12 edges
 - Rise: 0 to 3, 1 to 2, 0 to 1, 2 to 3, 0 to 2, 1 to 3
 - Fall: 3 to 0, 2 to 1, 1 to 0, 3 to 2, 2 to 0, 3 to 1

Measurement Setup:

- Receiver: 4th Order Bessel-Thomson low-pass filter with 33 GHz BW
- CR PLL BW 4 MHz and a slope of 20 dB/decade



The screenshot shows a table titled 'FlexDCA DCA Results' with the following data:

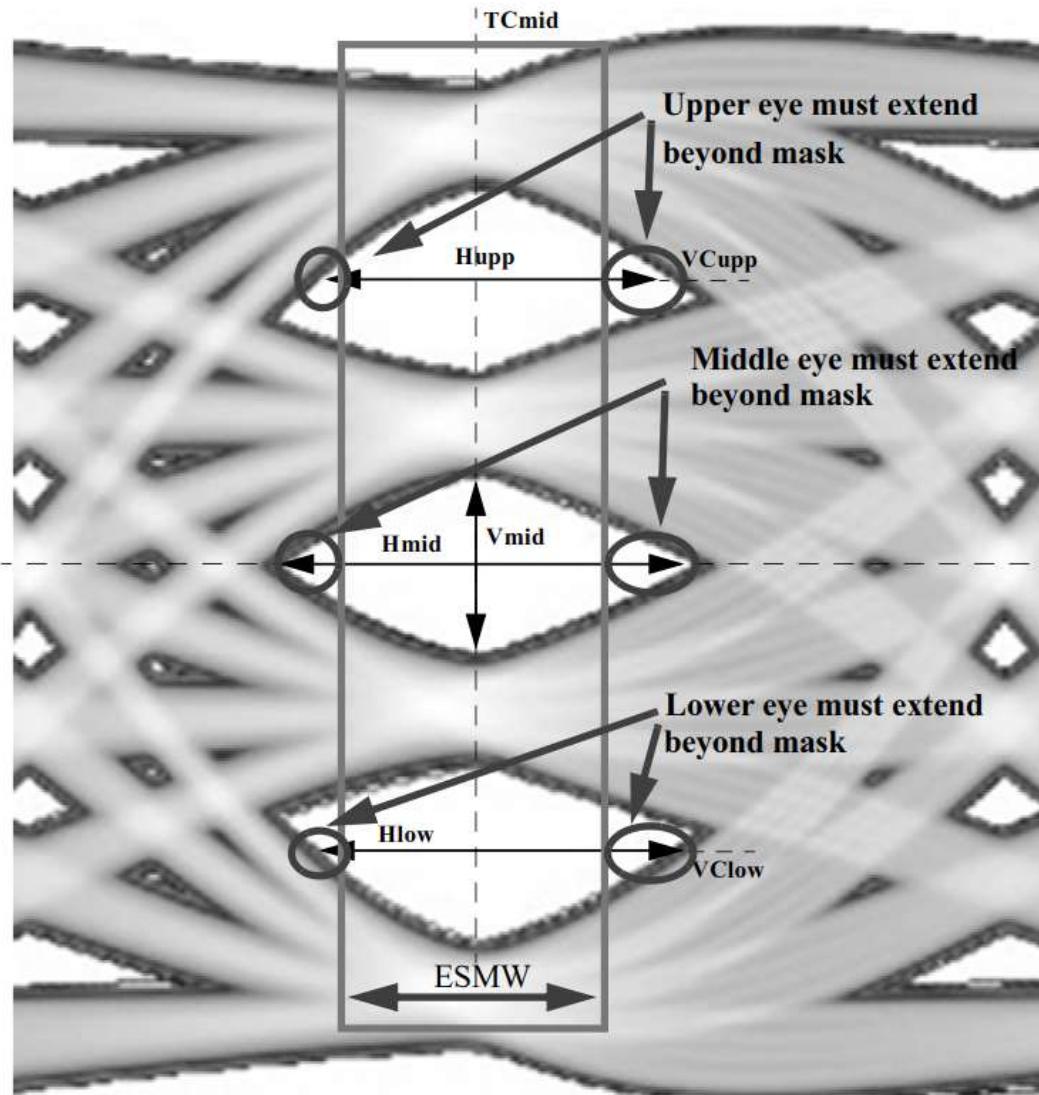
Measurement	To L0	To L1	To L2	To L3
J4u (All)	1.968 ps			
From L3	1.709 ps	1.754 ps	2.052 ps	—
From L2	1.781 ps	2.026 ps	—	2.032 ps
From L1	2.078 ps	—	2.056 ps	1.762 ps
From L0	—	2.028 ps	1.762 ps	1.739 ps

The screenshot shows a table titled 'Results: Measurements' with the following data:

Measurement
PRBS13Q Jrms(1-3)
PRBS13Q EOJ(1-3)
PRBS13Q J4u(1-3)

RT Scope Results

ESMW (Eye Symmetry Mask Width)



VEC (Vertical Eye Closure)

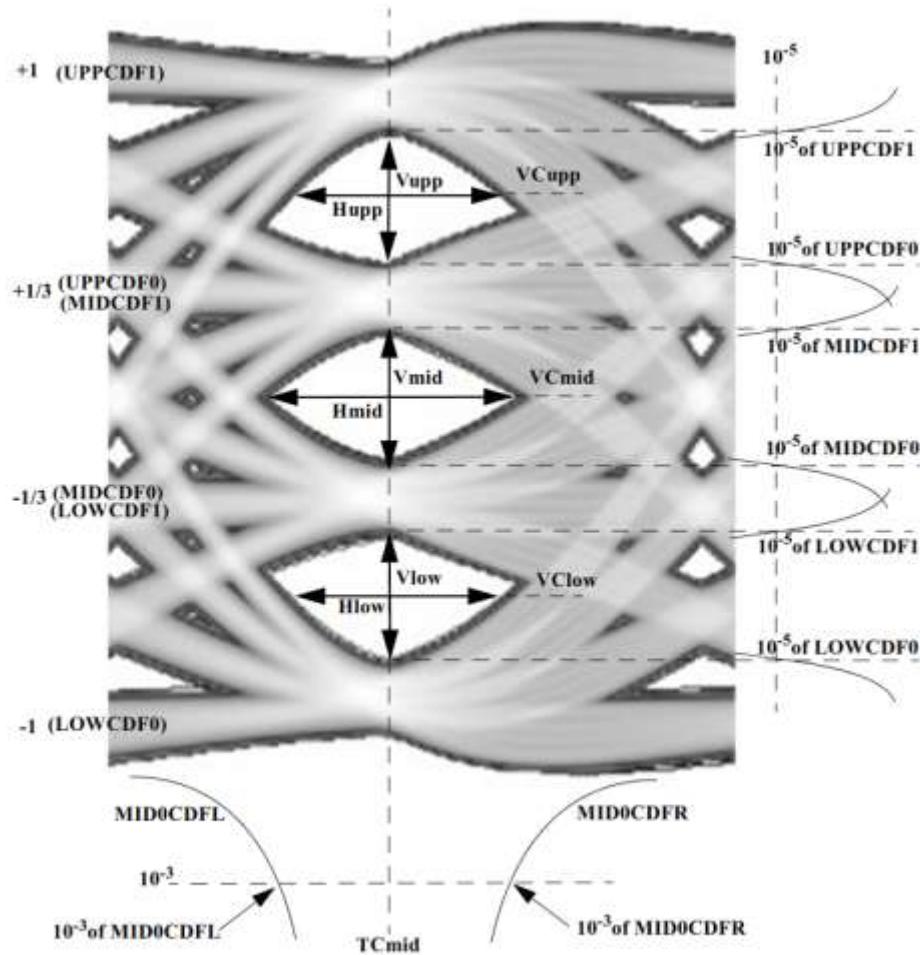


Figure 120E-13—PAM4 eye measurements

Vertical eye closure is defined by Equation (120E-4) for a PRBS13Q differential equalized signal captured and processed according to 120E.4.2.

$$VEC = 20\log_{10}\left(\max\left(\frac{AV_{upp}}{V_{upp}}, \frac{AV_{mid}}{V_{mid}}, \frac{AV_{low}}{V_{low}}\right)\right) \text{ (dB)} \quad (120E-4)$$

where

VEC is the vertical eye closure, in dB

V_{upp} is the 10^{-5} upper eye height per 120E.4.2

V_{mid} is the 10^{-5} middle eye height per 120E.4.2

V_{low} is the 10^{-5} lower eye height per 120E.4.2

AV_{upp} is the amplitude of the upper eye (AV_{upp}), equal to $VM3 - VM2$

AV_{mid} is the amplitude of the middle eye (AV_{mid}), equal to $VM2 - VM1$

AV_{low} is the amplitude of the lower eye (AV_{low}), equal to $VM1 - VM0$

$VM3$ is the mean of the differential equalized signal above $VCupp$ within 0.025 UI of $TCmid$

$VM2$ is the mean of the differential equalized signal between $VCupp$ and $VCmid$ within 0.025 UI of $TCmid$

$VM1$ is the mean of the differential equalized signal between $VCmid$ and $VClow$ within 0.025 UI of $TCmid$

$VM0$ is the mean of the differential equalized signal below $VClow$ within 0.025 UI of $TCmid$

$VCupp$ is the voltage center of the upper eye per 120E.4.2

$VCmid$ is the voltage center of the middle eye per 1120E.4.2

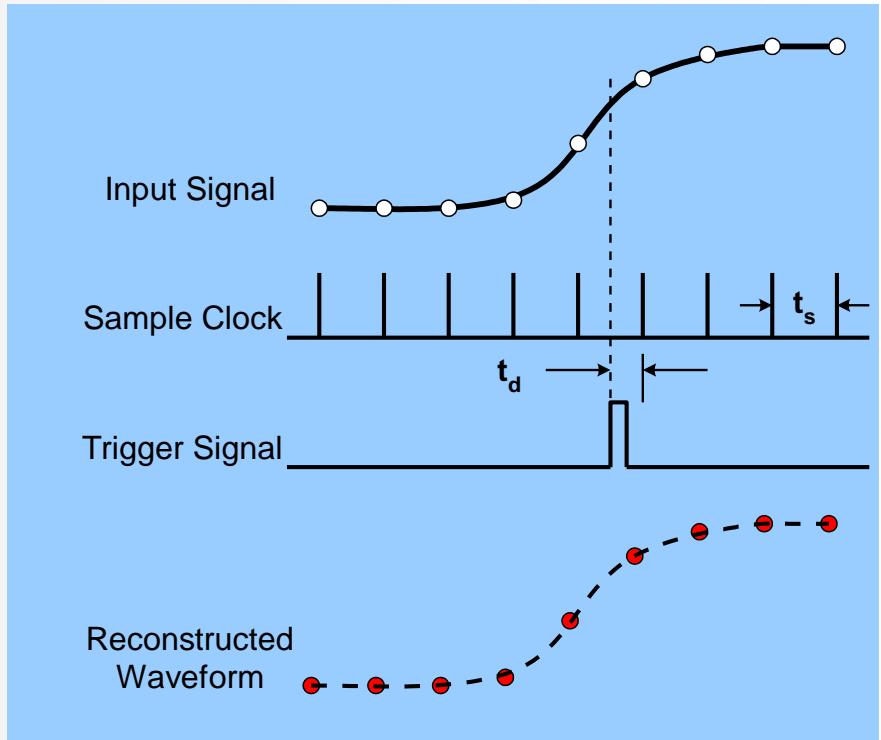
$VClow$ is the voltage center of the lower eye per 120E.4.2

$TCmid$ is the time center of the middle eye width per 120E.4.2

Agenda

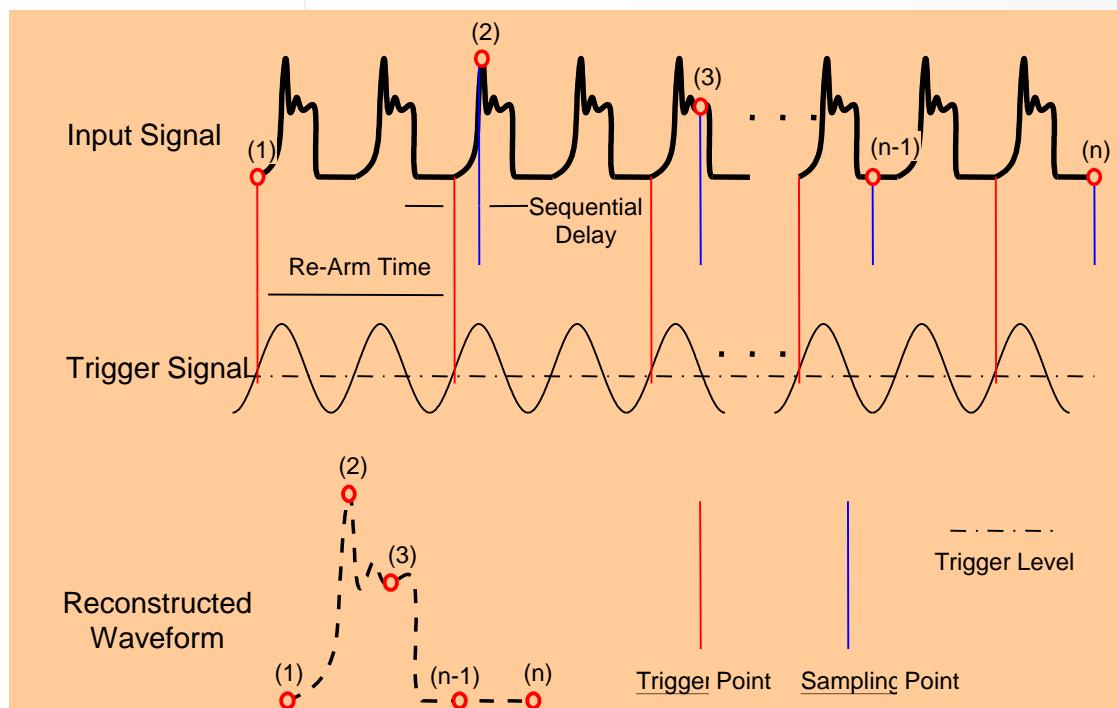
- High Speed Network Overview
- FAQ
- 400G Network Test discussion
- **Sampling Scope And CDR Basic**

Real Time V.S. Sampling

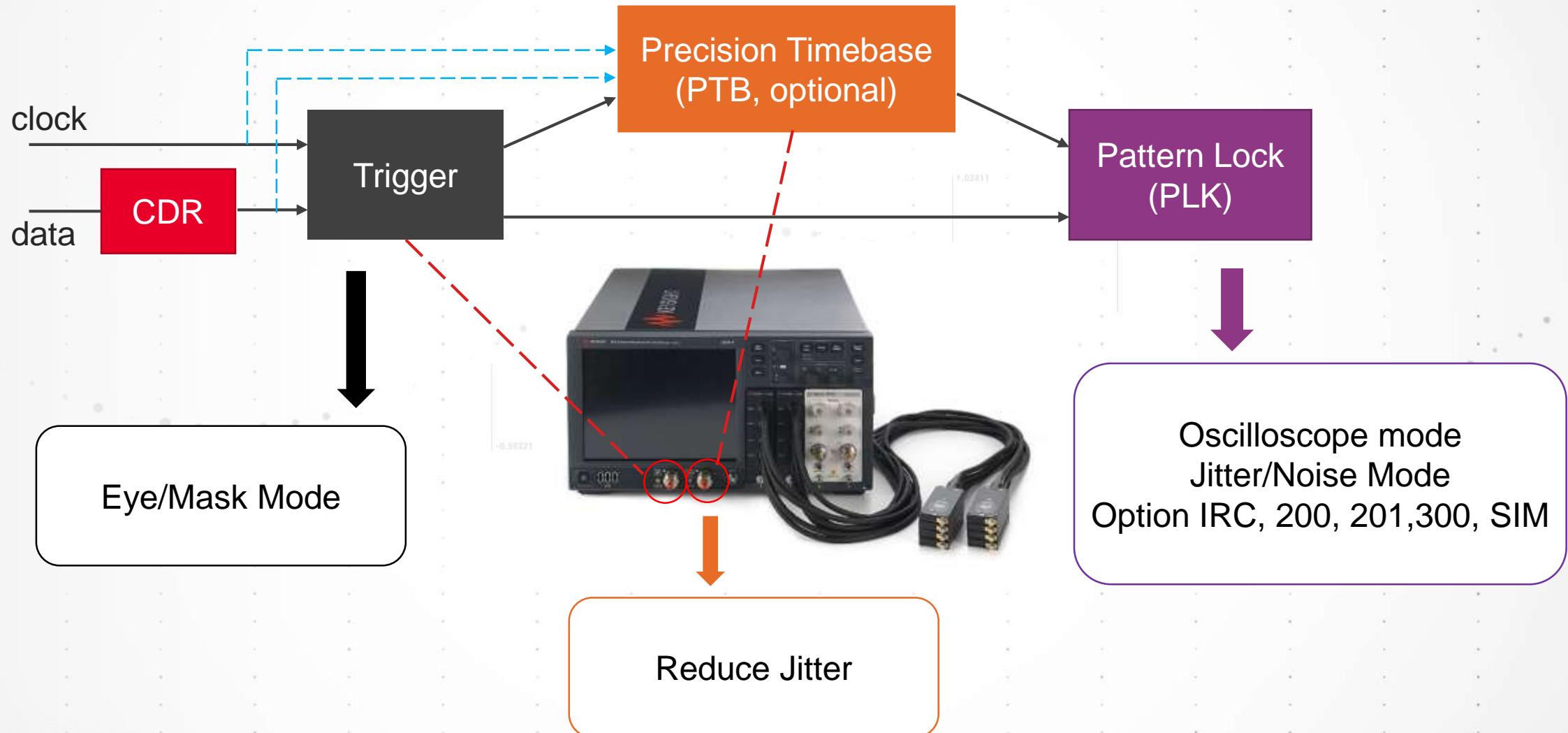


Sampling Oscilloscope
(Keysight DCA Series)

Real-Time Scope
(Keysight Infiniium Series)

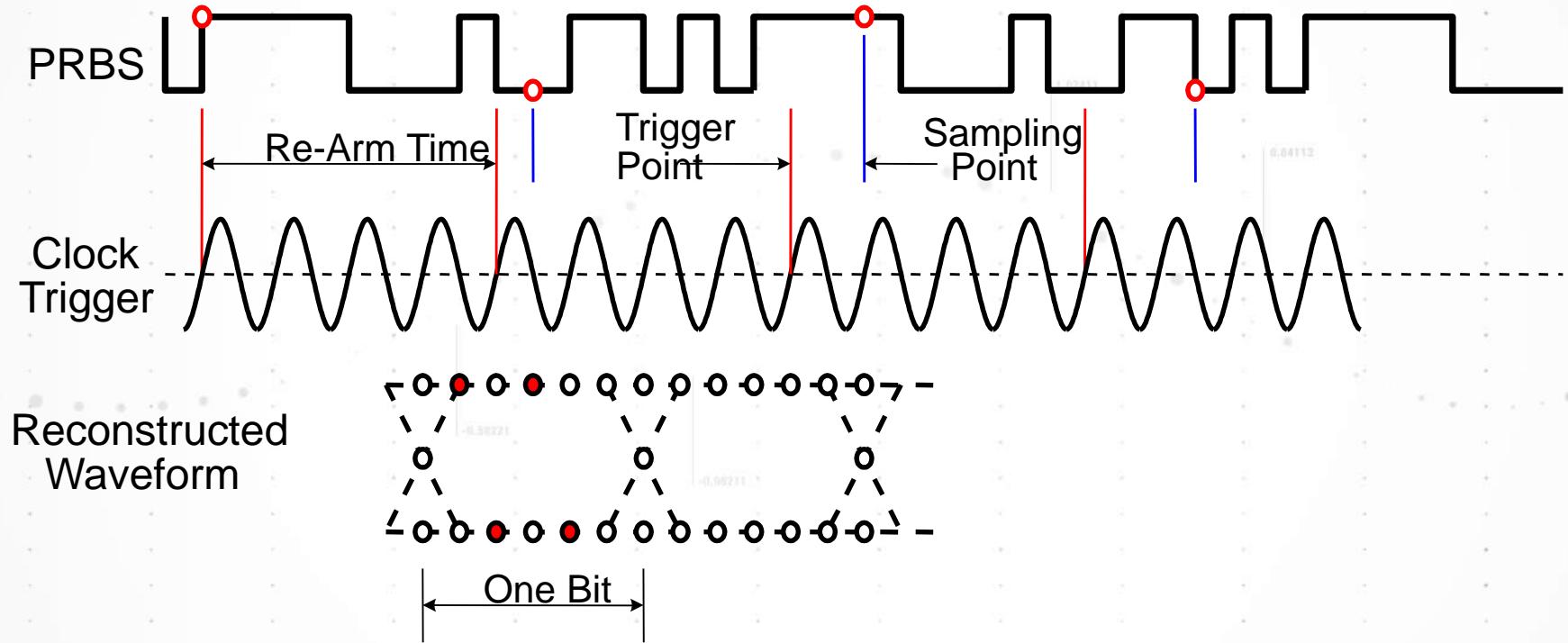


Trigger, PTB and Pattern Lock



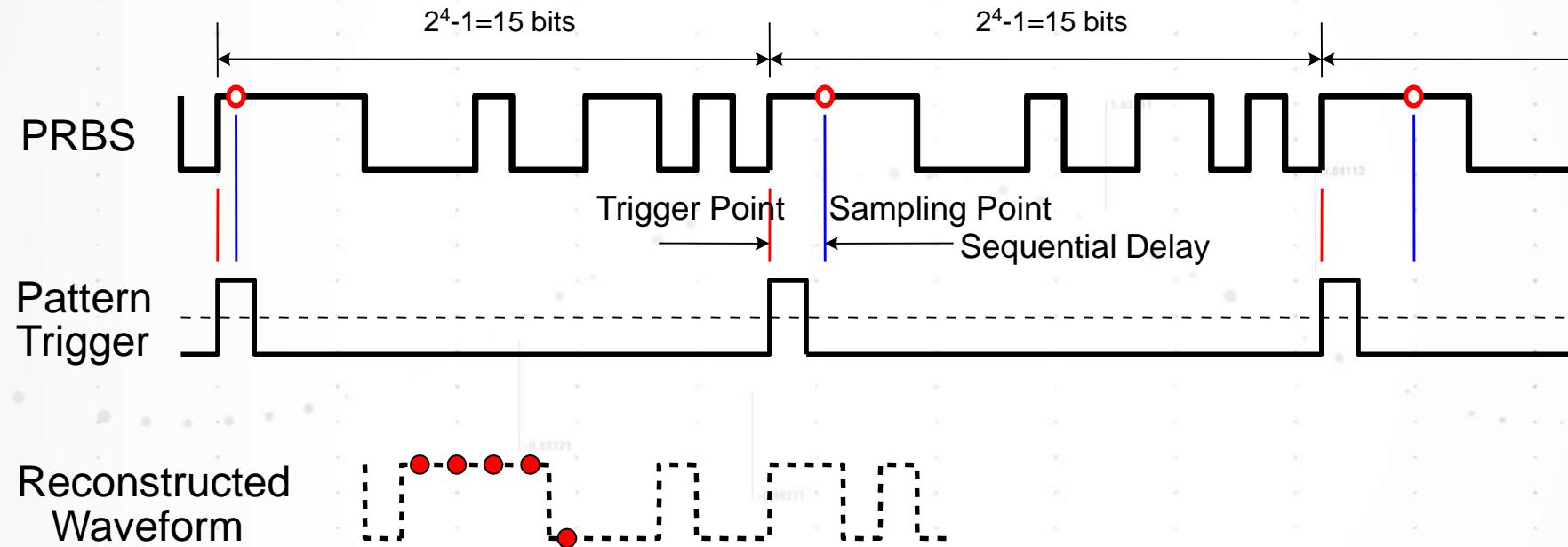
Acquiring Data – Clock Trigger

EYE DIAGRAM MODE



Acquiring Data –Pattern Lock

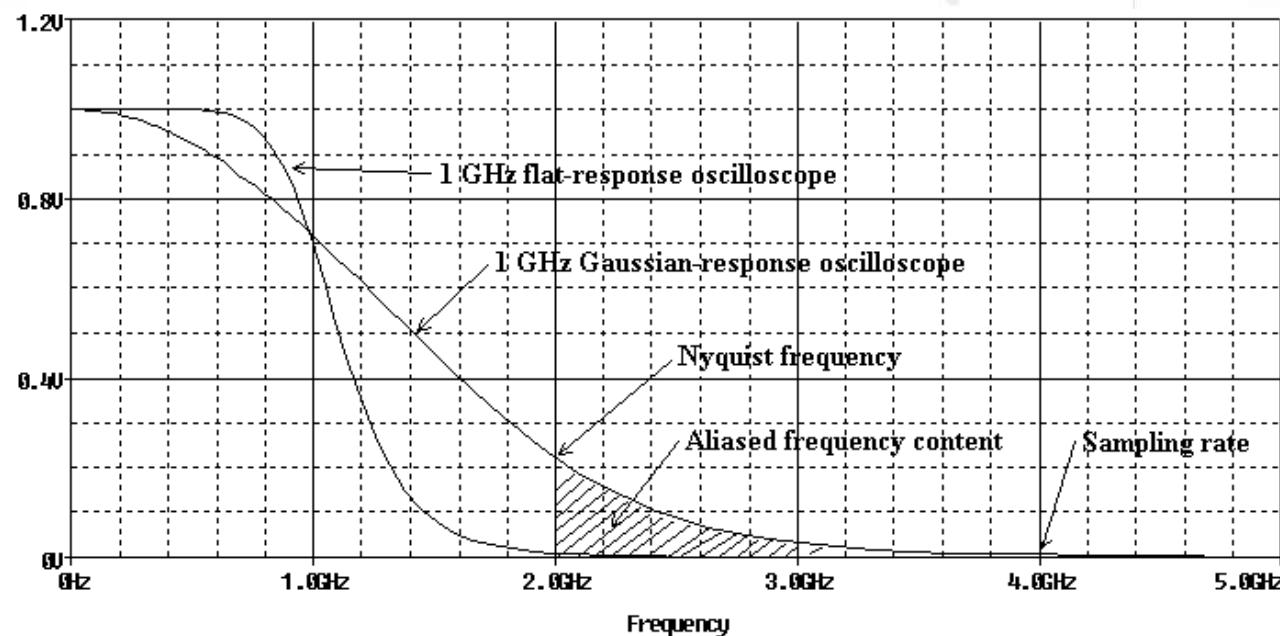
OSCILLOSCOPE / JITTER MODE



$$\text{Sequential Delay} = \frac{\text{Full - Screen Sweep Time}}{\text{Number of Trace Points}}$$

Q: SIRC (option -IRC)是做什麼用的？

- 一般高速數位訊號的測試，在定義示波器頻寬時僅定義3dB頻寬。但光通訊的測試，是連頻寬的 profile 都有明確定義為 4th Bessel-Thomson low-pass response。所以示波器這邊，特別是光的部分，需要一個符合標準的濾波器來搭配測試。而這個濾波器可以是硬體的，那就是在選購光模組的時候的 option。但如果有硬體濾波器以外的需求，可以用軟體的濾波器來做，這個就是 SIRC。SIRC 使用的時候會需要 Pattern Lock，而且SIRC的修正是針對每一顆模組，而不是同一型號共享，所以使用時一定要去官網下載對應的 SIRC 修正參數。



Time resolution

DCA time scale resolution

Mainframe specifications

Horizontal system (time base)	
Scale factor (full scale is ten divisions)	
Minimum	2 ps/div (with 86107A: 500fs/div)
Maximum	1 s/div
Delays ¹	
Minimum	24 ns
Maximum	1000 screen diameters or 10 s whichever is smaller
Time interval accuracy ²	1 ps + 1.0% of Δ time reading ³ or 8 ps, whichever is smaller
Jitter mode operation ⁴	Time interval accuracy - jitter mode operation 1 ps
Time interval resolution	≤ (screen diameter)/(record length) or 62.5 fs, whichever is larger

Sampling Scope: 16000GSa
Real time scope: 80GSa/s

The Sampling Scope can have more points on screen in one time interval (2ps/div) as example. And it's not limited by modules.

Infiniium time scale resolution

Acquisition

Maximum real-time sample rate	91304A	91604A	92004A	92504A	92804A	93204A
(2 channels)	80 GSa/s					
(4 Channels)	40 GSa/s					

Vertical noise floor

DCA RMS noise (86108B as example)

Dual electrical channel modules		86108A	86108B-LBW	86108B-HBW
RMS noise				
Characteristic	(Low / High BW Setting)	240 µV/420 µV	300 µV/500 µV	600 µV/750 µV
Maximum	(Low / High BW Setting)	350 µV/700 µV	350 µV/700 µV	800 µV/980 µV

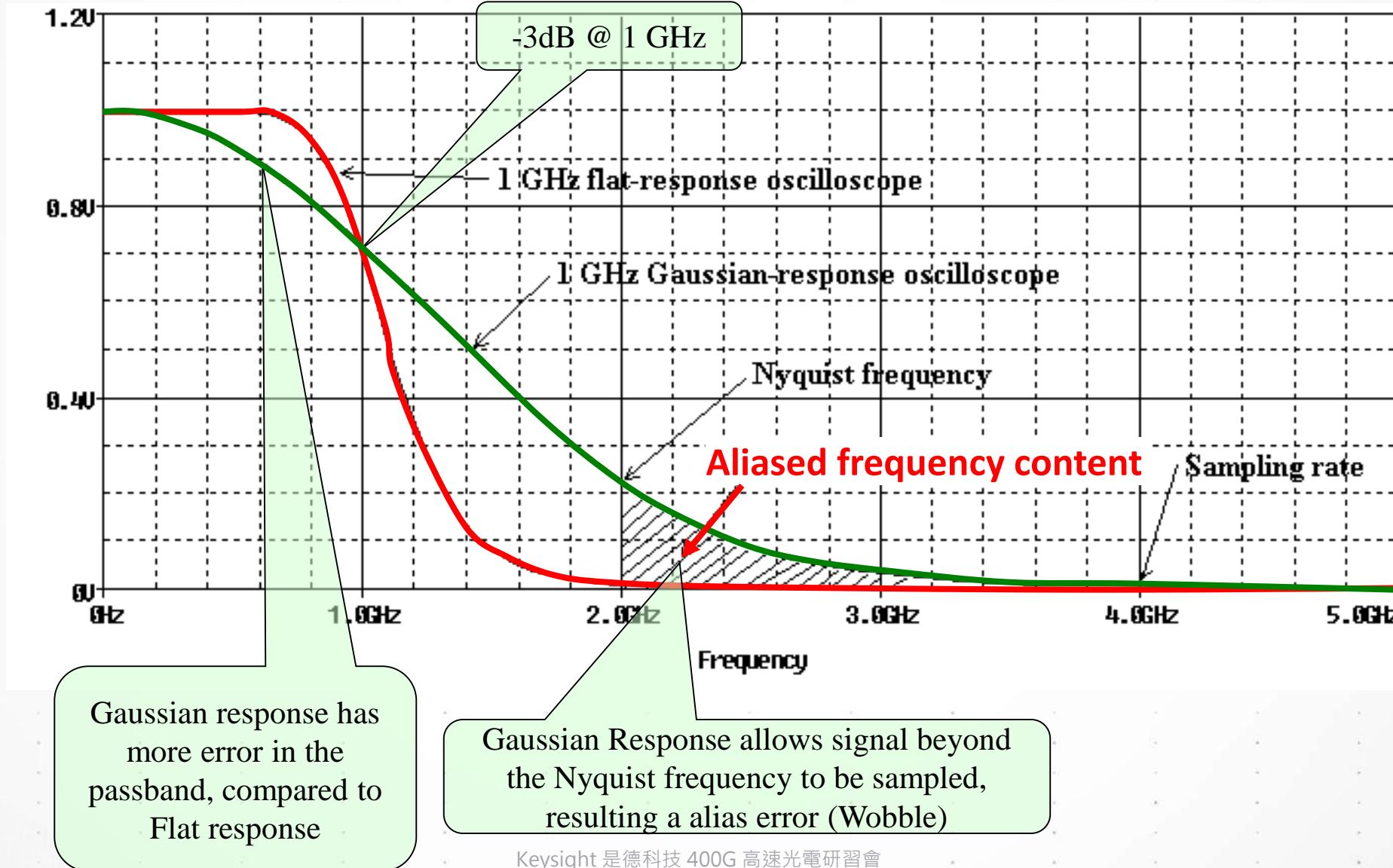
Infiniium RMS noise specification

RMS noise floor (scope only)						
Volts/div (mVrms)	91304A	91604A	92004A	92504A	92804A	93204A
10 mV	0.28	0.35	0.43	0.50	0.53	0.60
50 mV	1.10	1.34	1.53	1.76	1.86	2.10
100 mV	2.30	2.63	3.02	3.39	3.62	3.98
1 V	21.2	26.65	30.05	34.15	36.57	39.92

	13 GHz	16 GHz	20 GHz	25 GHz	28 GHz	33 GHz
%FS Noise @ 50mV/div	0.295%	0.335%	0.383%	0.440%	0.465%	0.525%

SS noise floor is better than RS is because 14bits V.S. 8 bits

Bandwidth compare



Compliance Frequency Response

REFERENCE RECEIVER

To provide more consistency, several standards now specify BW and shape.

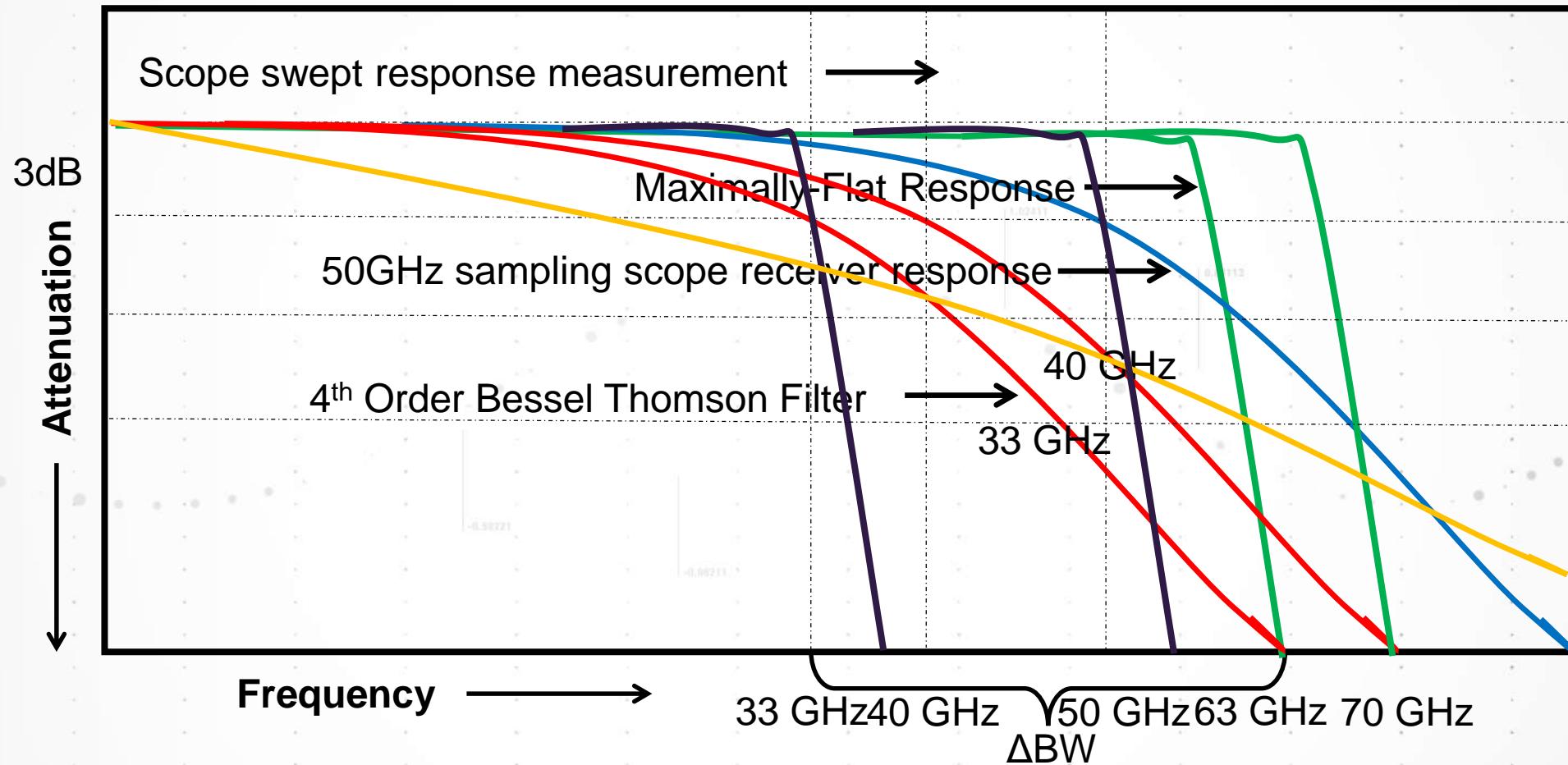
- IEEE P802.3bj™/D3.2, 11th April 2014 Section 92.8 100GBASE-CR4 Electrical Characteristics:

"A test system with **a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth** is to be used for all transmitter signal measurements, unless otherwise specified."

- Implementation Agreement OIF-CEI-03.1 13.3.10 Transition Time

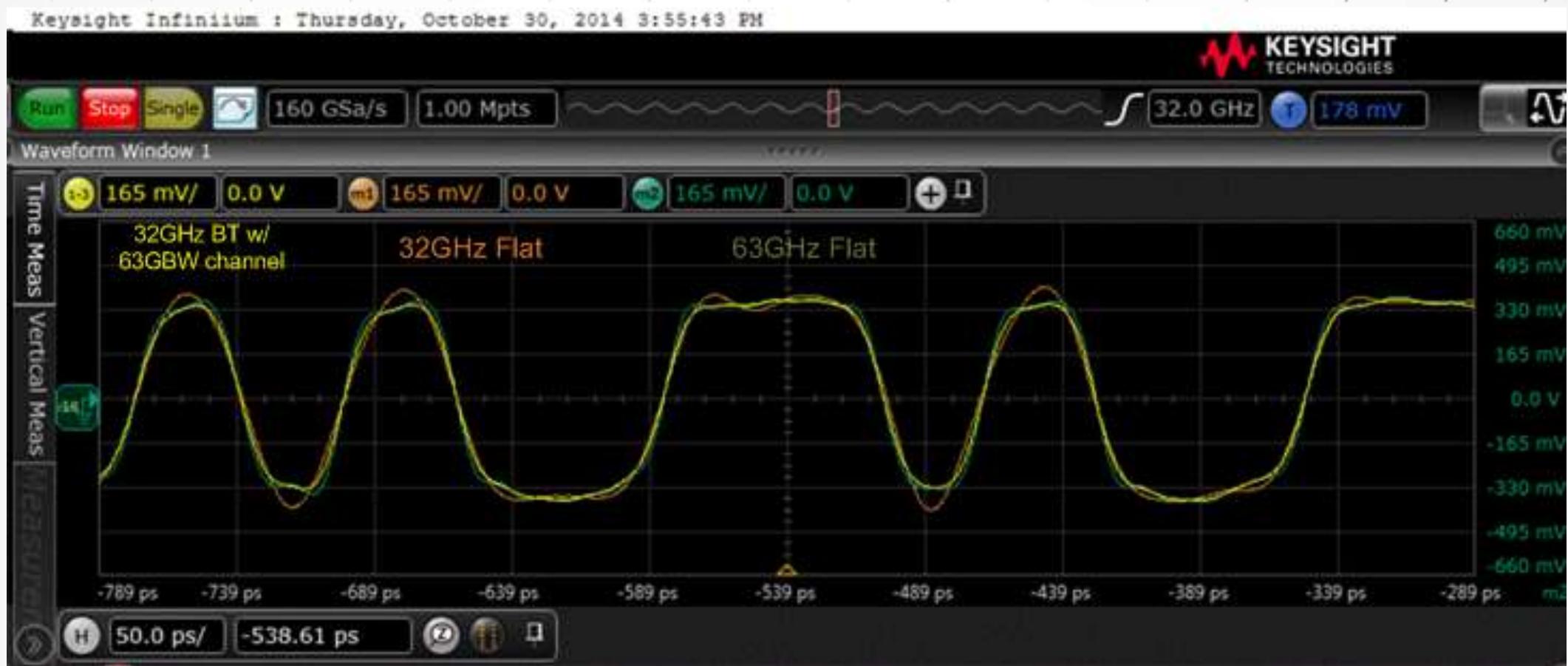
"The waveform is observed through **a fourth-order Bessel-Thomson response with a bandwidth of 40 GHz.**"

Effects of 4th Order Bessel-Thomson low pass filter



There is a compromise between the flat response with higher bandwidth and the 4th Order Bessel Thomson Filter response that has less bandwidth but a smoother roll off.

Different Waveform Response



Frequency Response



Tan – 33GHz Flat

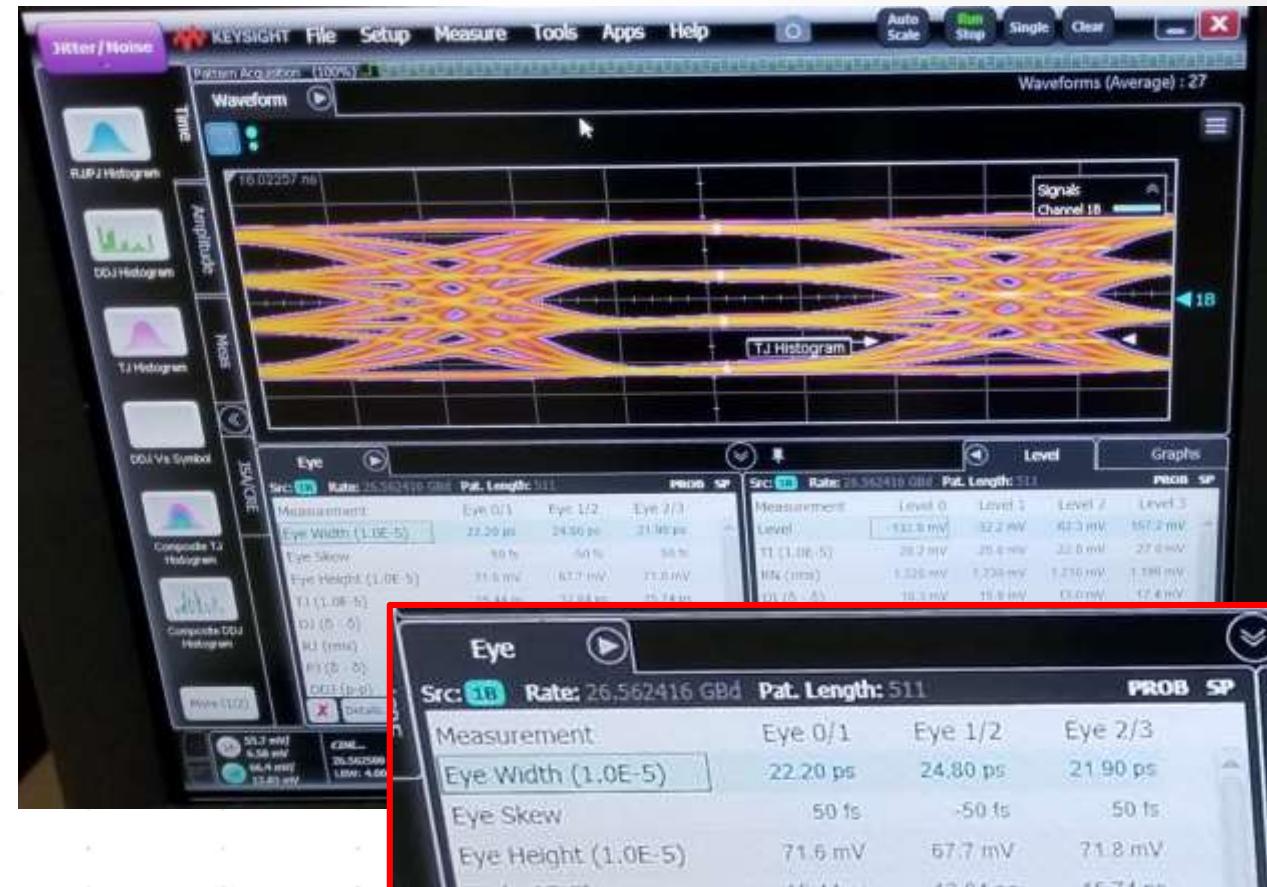
Green – 33Ghz BT

Orange – 63 GHz flat

- As we can see we need the full 63GHz BW in order to capture the entire Bessel Thomson frequency response.
- Note that we can not use the standard (as opposed to real edge) channels as they do not have enough bandwidth to apply the BT filter.

28 GBd Comparison

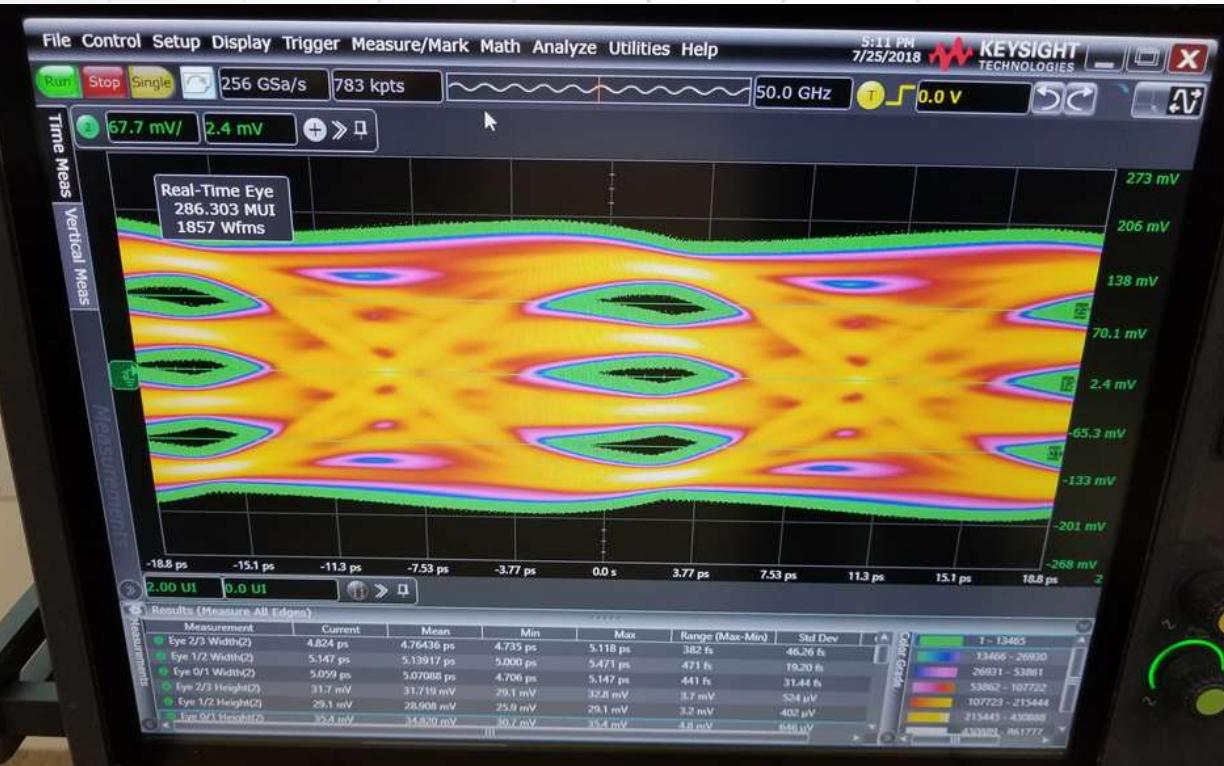
BEST OF BOTH WORLDS (REAL-TIME AND EQUIVALENT-TIME OSCILLOSCOPES)



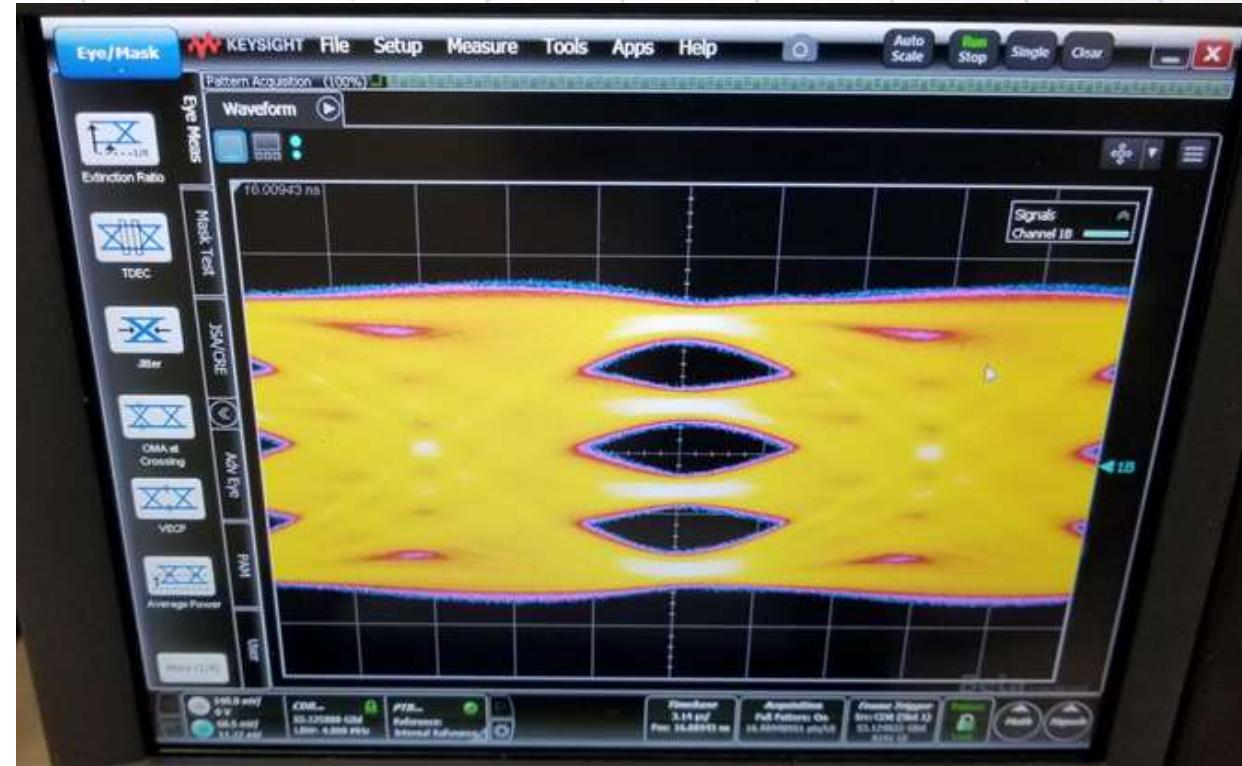
- Excellent correlation on EW measurements (22ps, 24ps, 22ps)
- DCA had more margin on EH measurement (lower intrinsic noise), ~56 mV vs ~70 mV

53 GBd Comparison

BEST OF BOTH WORLDS (REAL-TIME AND EQUIVALENT-TIME OSCILLOSCOPES)



UXR – Series
(N1040A PG Source: 53 GBd, PRBS13Q)



N1060A MegaModule
(N1040A PG Source: 53 GBd, PRBS13Q)

Real and Sampling Time Oscilloscopes

Sampling Scope

- Cost
- Time base resolution
- Lower noise
- Lower Jitter

Real Time Scope

- Fast Acquisition
- Single Event capture
- HW CDR is not required
- Pattern is not required

DCA Hardware option

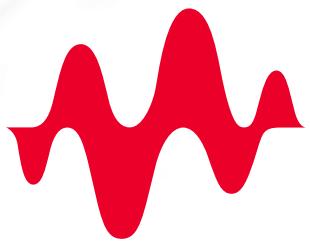
- **ETR** – Enhanced Trigger (*86100D*)
 - Support > 13GHz 的 trigger，並且增加了pattern 相關分析的能力 (= PLK option)
- **LOJ** – Low Jitter Timebase (*N1000A, N109x*)
 - 降低儀器的 Jitter 至 200fs
- **PTB** – Precision Timebase (*86100D, N1000A, 86108B, N1060A*)
 - 降低儀器的 Jitter 至 70fs
- **PLK** – Pattern Lock Trigger Hardware (*N1000A, N109x*)
 - 可鎖定 Pattern 後作 Jitter / Scope 的分析，也是 SIRC / CTLE 等訊號處理之必須要件。
- **IRC** – Impulse Response Correction (*86105C/D, 86115D, 86116C, N1090A, N1092x*)
 - 針對個別光模組硬體作頻率響應之校驗，以用來補償並提供理想的頻率響應來符合各標準之要求
- **FS1** – Fast Sampling (*N1092x, N1094x*)
 - 將 Sample rate 從 100KSa/s 提升至 250KSa/s
- **GPI** – GPIB Card Interface (*86100D / N1000A*)

DCA Software option (I)

- **200** – Enhance Jitter Analysis
 - 具備完整 jitter 分析的能力，包括 TJ/RJ/DJ/PJ/ISI/DDC/UJ/J2/J5/J9/DDPWS/BUJ 等
- **201** – Advanced Waveform Analysis
 - LFE/FFE/DFE/CLTE, Deep memory up to 2^{23} bits, MATLAB 分析
- **202** – Enhanced Impedance and S-Parameter Software
 - 將 TDR 量測之參數轉換成 S 參數。
- **300** – Advanced Amplitude Analysis / Rin / Q-Factor (**Bundled in option 200**)
 - 針對 Amplitude 的部分類似 Jitter 形式的雜訊分析
- **401** - Advanced Eye Analysis
 - 可以分析長週期的訊號 (2^{23} , 2^{31} 或是 live traffic)
 - 直接在 jitter mode 進行 jitter 分析 TJ/RJ/DJ/J2/J9/DDPWS 等等
- **500** – Productivity Package
 - 增加量測速度，增加 TDEC 量測

DCA Software option (II)

- **SIM** – InfiniiSim-DCA Waveform Transformation (86100D / N1000A / N1010A)
 - Embedding，即可以把一段channel或是其他的電路效應apply到量測的訊號
 - De-embedding，即可以把治具或是其他不想要的電路效應移除
- **EFP** – Flex Eye - Independent Channel Acquisition and Control
 - 可讓多通道之儀器在各通道獨立抓取眼圖。
- **9FP** – PAM-N analysis software
 - 可以進行PAM-4的完整分析，協助完成IEEE400G相關測試
- **BFP** – Automatic Fixture Removal in TDR Mode
 - AFR 功能 (TDR 模組用)
- **TFP** – IEEE TDECQ analysis
 - 使用相容於 IEEE 之 TDECQ 量測



KEYSIGHT
TECHNOLOGIES