Be prepared to test next-gen Type-C Technologies

Jit Lim, Keysight Type-C Strategic Planner

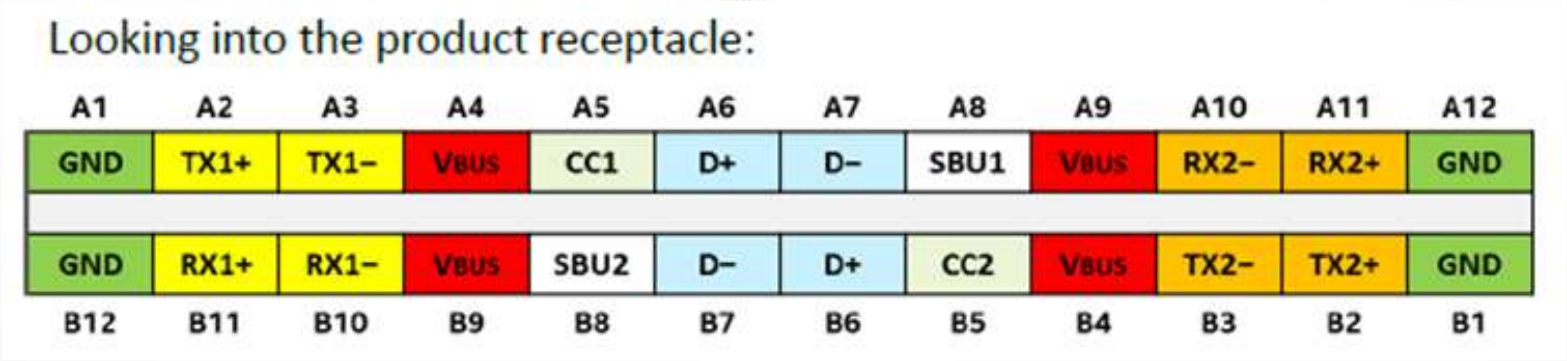
Agenda

- Technology Waves
- Fundamental Challenges
- USB 3.2 Retimer
- USB 3.2 Redriver
- USB 3.2 x2
- USB4
- DP 2.0
- What happens after USB4?
- eUSB2
- Summary
- Q&A

Publicly Announced Technology Waves

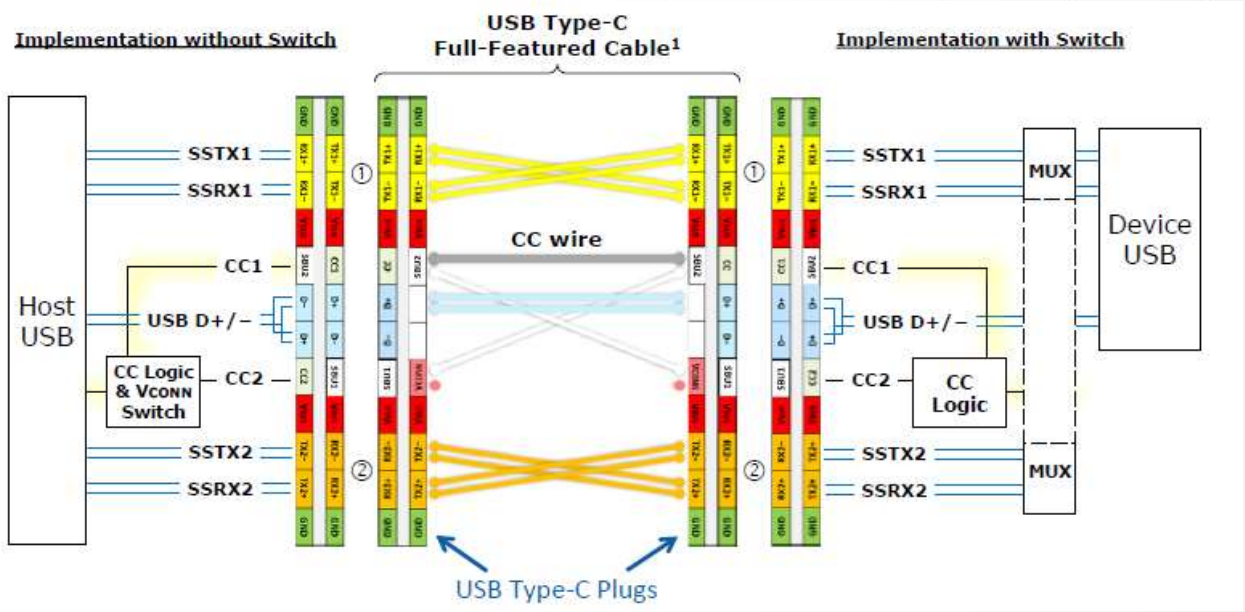
- USB-IF releases USB 3.2 x2 and Retimer Specification
- Ice Lake processor will be first to integrate Thunderbolt 3: https://newsroom.intel.com/news/intel-takes-steps-enable-thunderbolt-3-everywhere-releases-protocol/#gs.b2jb5k
- USB-IF proposing Redriver Test Specification
- USB-IF announces USB4:

https://usb.org/sites/default/files/2019-03/USB_PG_USB4_DevUpdate_Announcement_FINAL_20190226.pdf



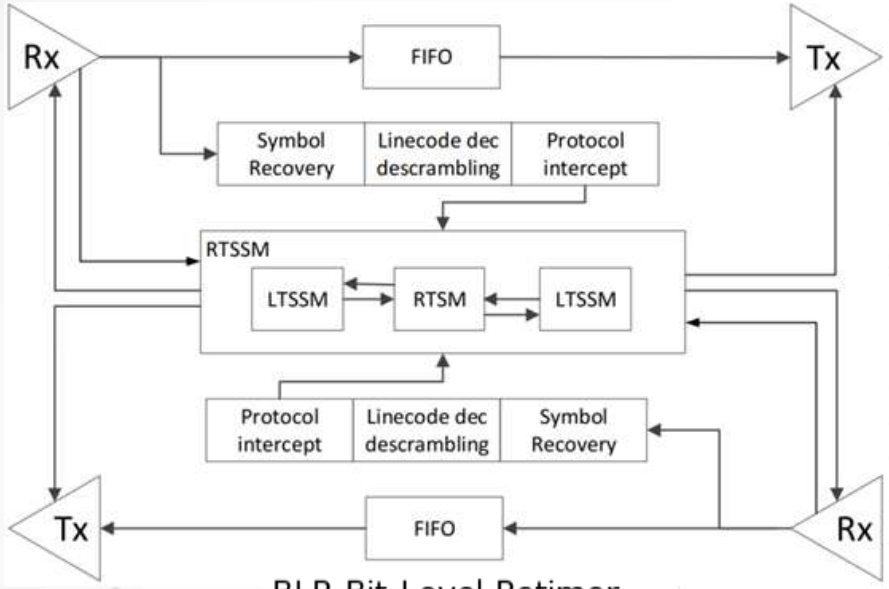
Fundamental Challenges

- Thunderbolt integrated CPU
  - Channel lengths for 10/20 Gbps signaling will be much longer.
- X2 mode
  - Comprehend crosstalk
- Repeater
  - SRIS retimer
  - BLR retimer
  - Redrivers
  - Optical cable

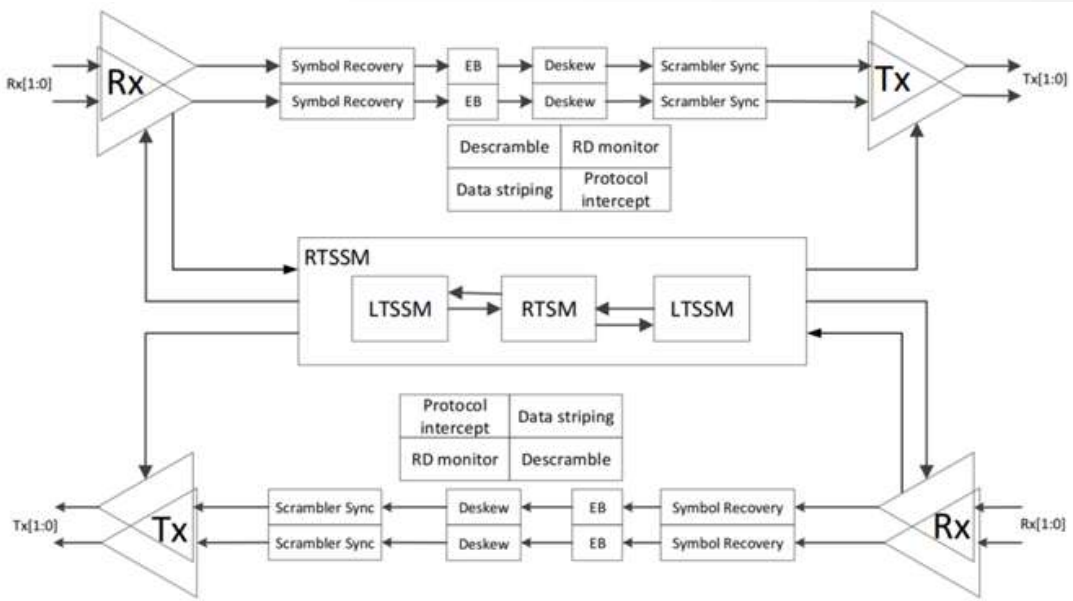


- USB4 Open Spec
  - PHY rate doubled to 20 Gbps, x2 mode doubles that to 40Gbps

USB 3.2 SRIS and BLR Retimer Overview



BLR Bit Level Retimer



SRIS

Separate Reference clock

Independent SSC Retimer

- Bit Level Retimer
  - TX Clock derived from incoming Clock Data Recovery
- Separate Reference Clock Independent Spread
  - Clock offset compensation via Elastic Buffer

USB 3.2 SRIS and BLR TX Testing

- Component
- Embedded
- BLR Compliance Mode
- PassThrough Loopback Mode
- SKP OS CPx Toggle
- Dual PG for Compliance Mode Entry and CPx Toggle
- Stressed LTSSM propagation and signaling
- Clock Switch dF/dt test
- Jitter Transfer Function test

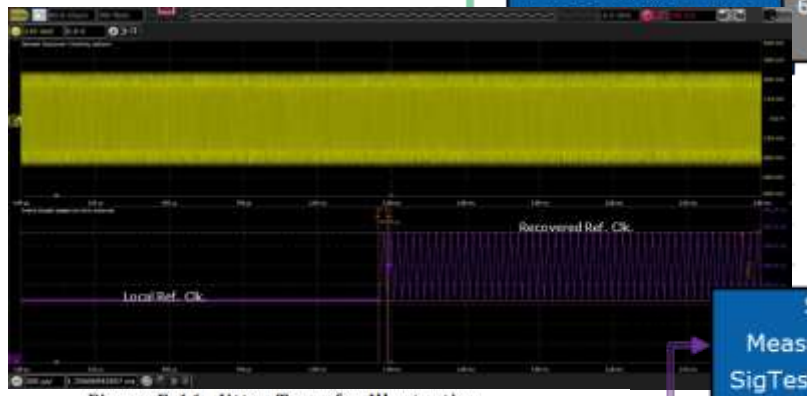


Figure E-16. Jitter Transfer Illustration

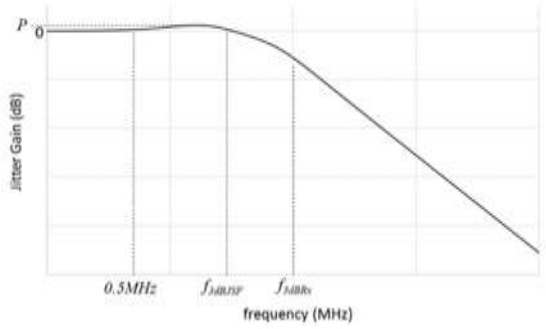
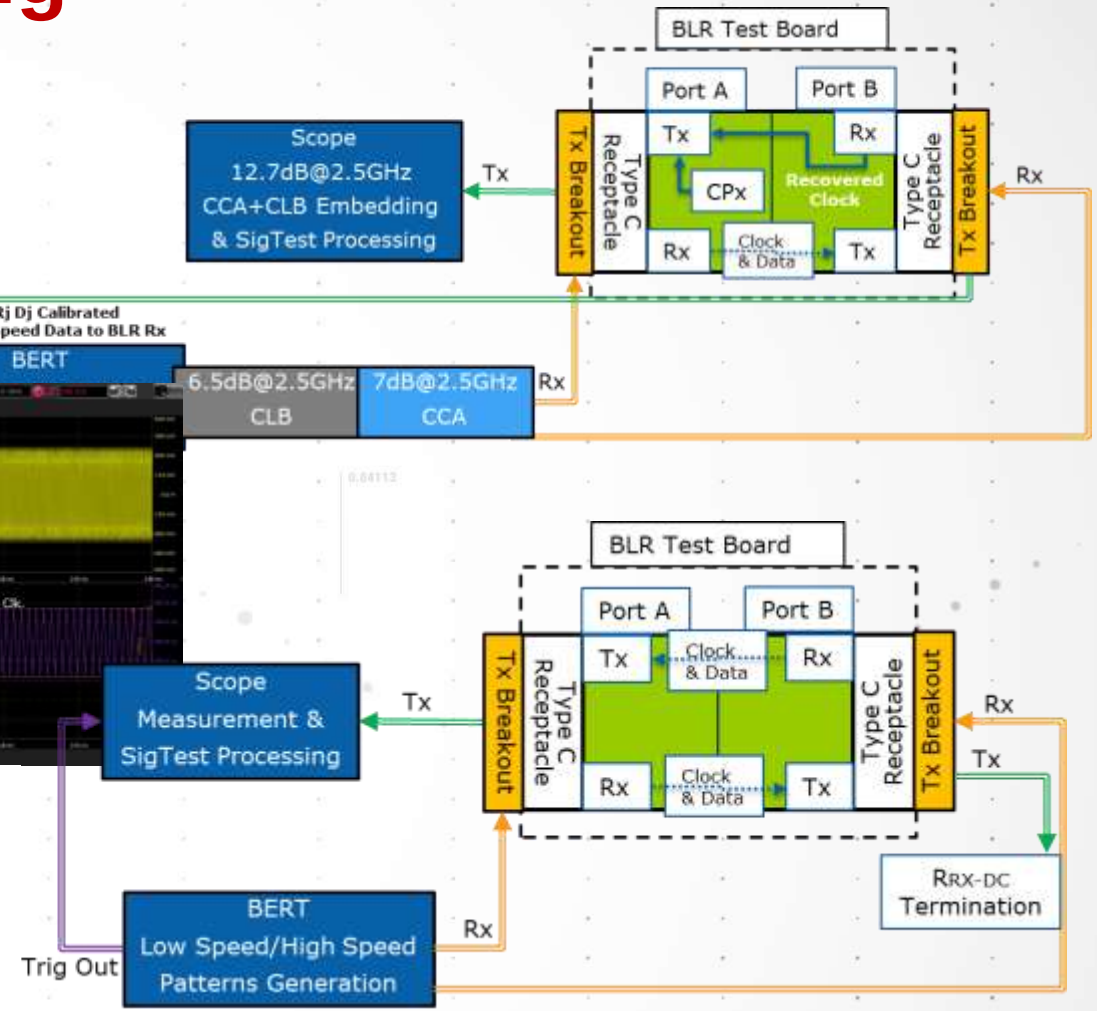


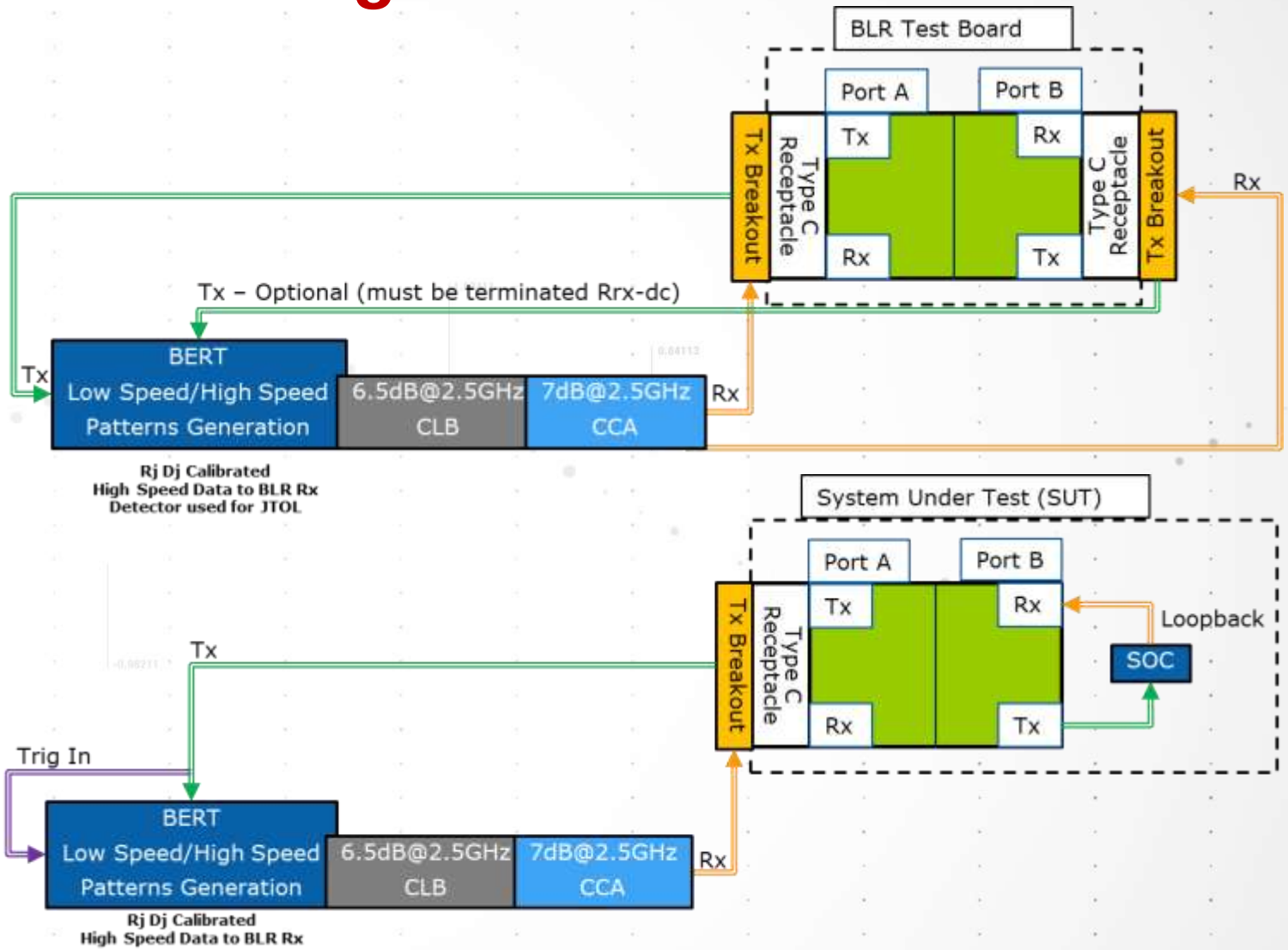
Table E-3. Bit-Level Re-timer Jitter Transfer Function Requirements

Term	Gen 1x1	Notes
Jitter Gain for f<500kHz	0.1dB (max)	Normative requirement.
Jitter Gain for f>500kHz	0.0dB (max)	Normative requirement.



USB 3.2 BLR and SRIS RX Testing

- Component
- Embedded
- Pass-through loopback
- Dual-lane symmetrical testing



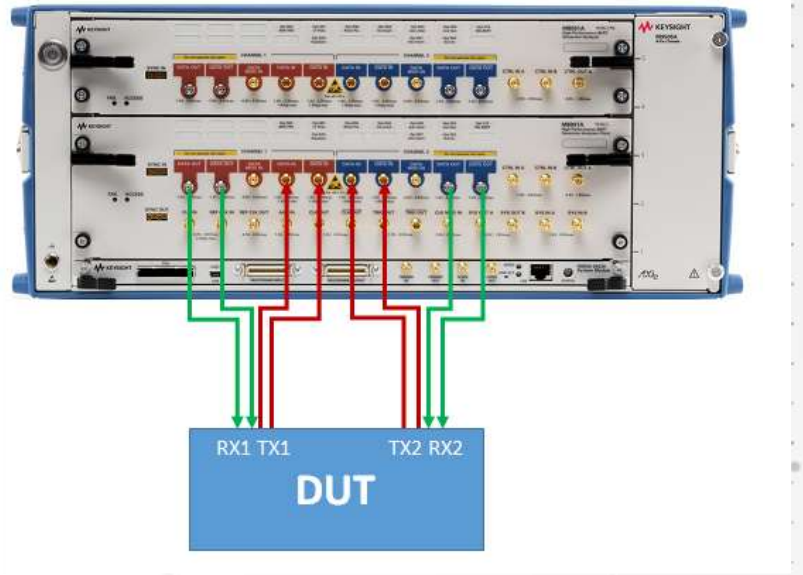
USB 3.2 x2 Test Considerations

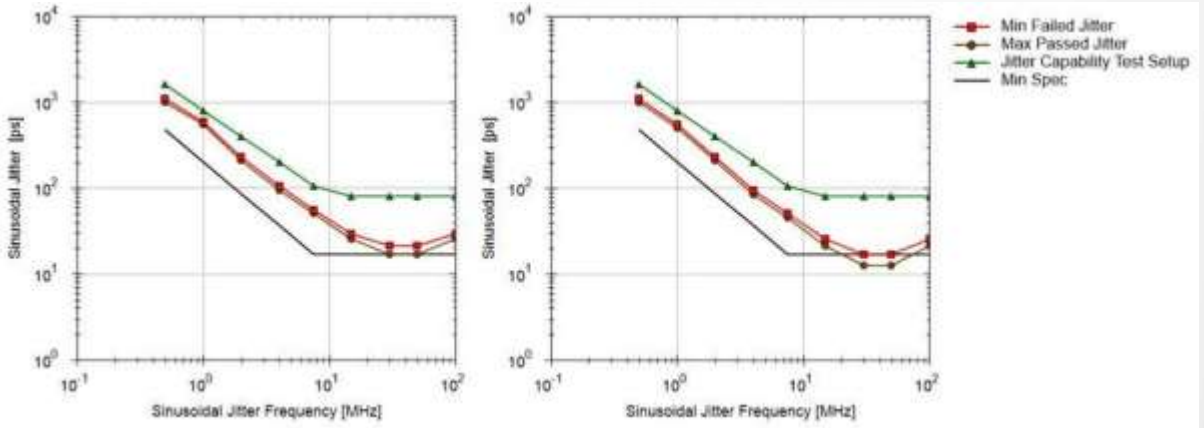
Transmitter

- Sufficient bandwidth required on all 4 channels to comprehend crosstalk
- Sufficient bandwidth required on all 4 channels to analyze rise-time and skew
- Updated SW to latest Compliance Test Spec
- Dependencies when coupled with x2 retimers
- Protocol Decode

Receiver

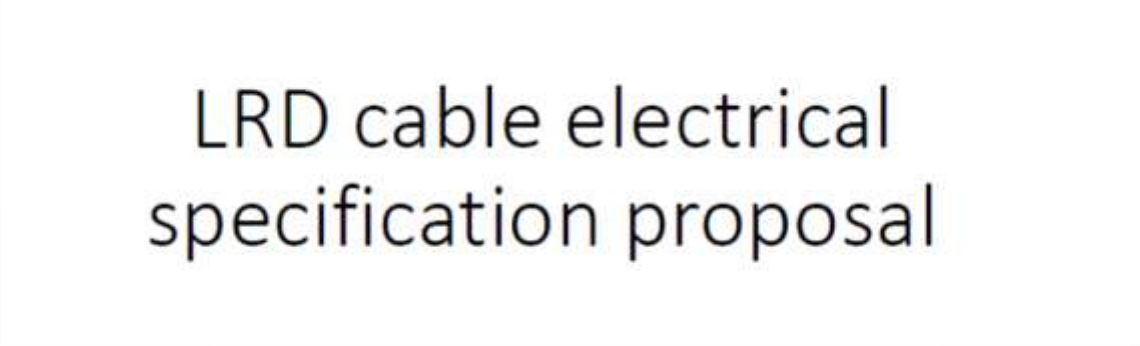
- Dual channel Pattern Generator/Error Detector testing JTOL on both lanes in parallel to comprehend crosstalk
- Updated SW to calibrate and test dual channel mode





USB 3.2 Redriver Test Proposal

- Testing as a captive or embedded product
- USB-IF proposing new testing methodology
- Based on Ethernet COM approach
- Requires a Scope, BERT, and ENA



USB4 Overview

- Announced by USB-IF in Q1 2019
- Open standard and potentially integrated in CPU
- Based on the Thunderbolt 3 protocol
- Uses the Type-C connector
- Tunnels USB, DP, and PCIe
- Channel aggregation: two independent 20Gbps bonded into one logical 40Gbps link
- Supports other standards through ALT mode
- Keysight can help test with early adopter Protocol Decode, TX, RX, and Return Loss

Universal Serial Bus 4 (USB4)
Specification

USB4 Electrical Testing Methodology

- PHY testing approach will be similar to Thunderbolt 3
  - Tx, Rx, and Return Loss
  - Active and Passive Cable Test

  Plus
  - Type-C Power Delivery
  - DP, USB over Type-C

Universal Serial Bus 4 (USB Type-C)
Electrical Compliance Test Specification

Proposed differences between testing USB 3.2 x1 vs USB4

- Return Loss TX and RX
- Transmitter Equalization is not fixed and requires calibration
- Receiver Equalization is much more complex and requires calibration
- PHY bit rate doubles from 10 Gbps to 20 Gbps
- Signaling on all 4 Type-C high-speed pairs
- De-Embedding of Test Cables
- New IL budgets for 10G/20G
- Retimer specific measurements
- Cross-talk Generation
- New Jitter Measurements
- New Phase and Slew Rate Measurements
- Added Skew Measurements
- Common Mode Interference
- Separate Jitter Cocktails for 10G/20G/TP2/TP3
- Link Optimization prior to BER test
- Built in Error Detector

DP 2.0

transfer without compromising display performance. DP 2.0 leverages the Thunderbolt™ 3 physical interface (PHY) layer while maintaining the flexibility of DP protocol in order to

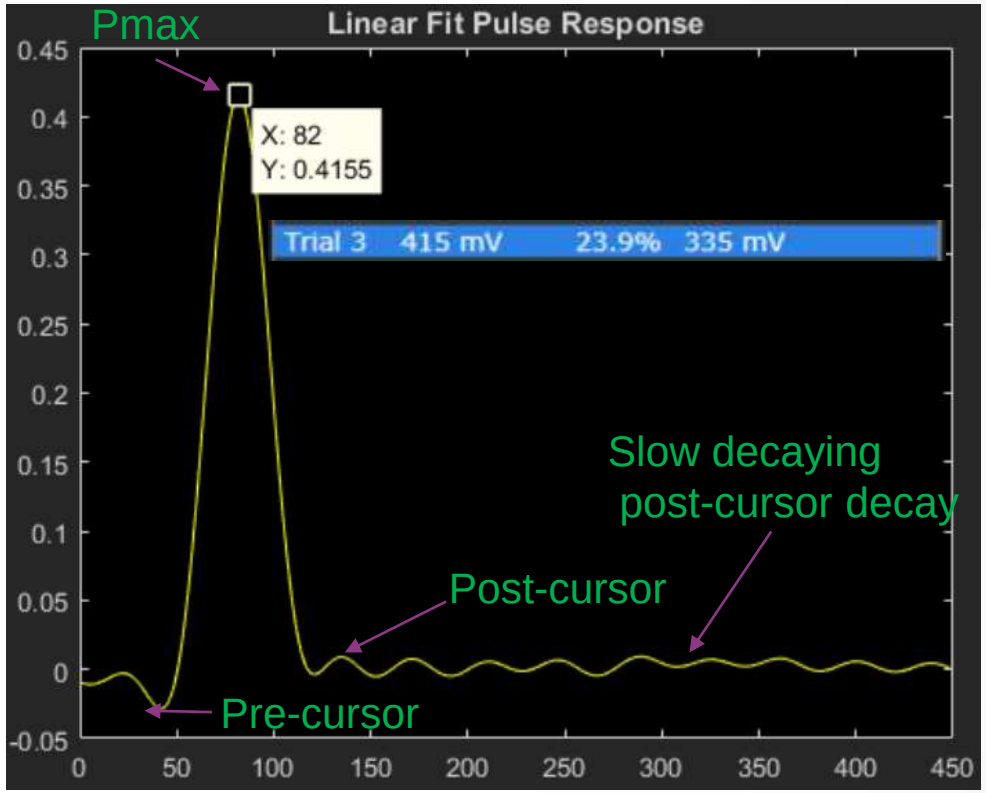
"Intel's contribution of the Thunderbolt™ PHY layer specification to VESA for use in DP 2.0 is a significant milestone making today's simplest and most versatile port also the highest performing for display," said Jason Ziller, General Manager, Client Connectivity Division at Intel. "By collaborating with VESA, we're enabling common building block technologies to come together across a wide range of

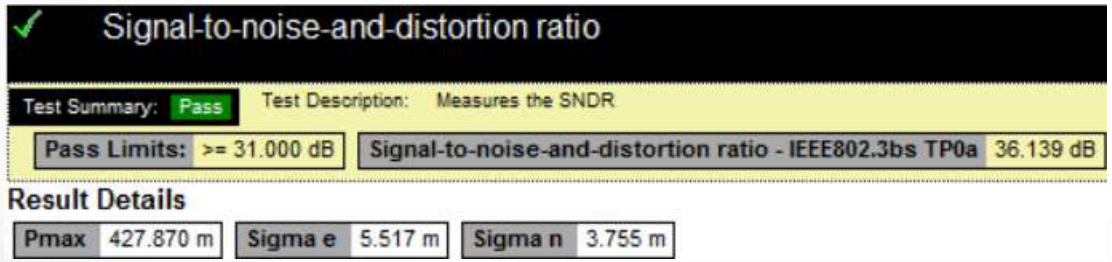
link rate of 8.1 Gbps/lane. With 8b/10b channel coding, that equates to a maximum payload of 25.92 Gbps. DP 2.0 increases the maximum link rate to up to 20 Gbps/lane and features more efficient 128b/132b channel coding, delivering a maximum payload of 77.37 Gbps – up to a three-fold increase compared to DP 1.4a. This means that DP 2.0 is the first standard to support 8K resolution (7680 x

Testing Next-Gen Type-C Standards after USB4 – PAM-4?

PAM-4 Linear Fit Pulse Response and SNDR

- Signal-to-Noise and Distortion Ratio (SNDR)
- P_{max}^2 = Linear Fit Pulse
- σ_e^2 - standard deviation of error
- σ_n^2 - standard deviation of noise
- Peak level is equal to the highest point on the x-axis.
- FIR to address Pre-cursor ISI
- DFE can help post-cursor issues





$$SNDR = 10\log_{10}\left(\frac{p_{\max}^2}{\sigma_e^2 + \sigma_n^2}\right)$$

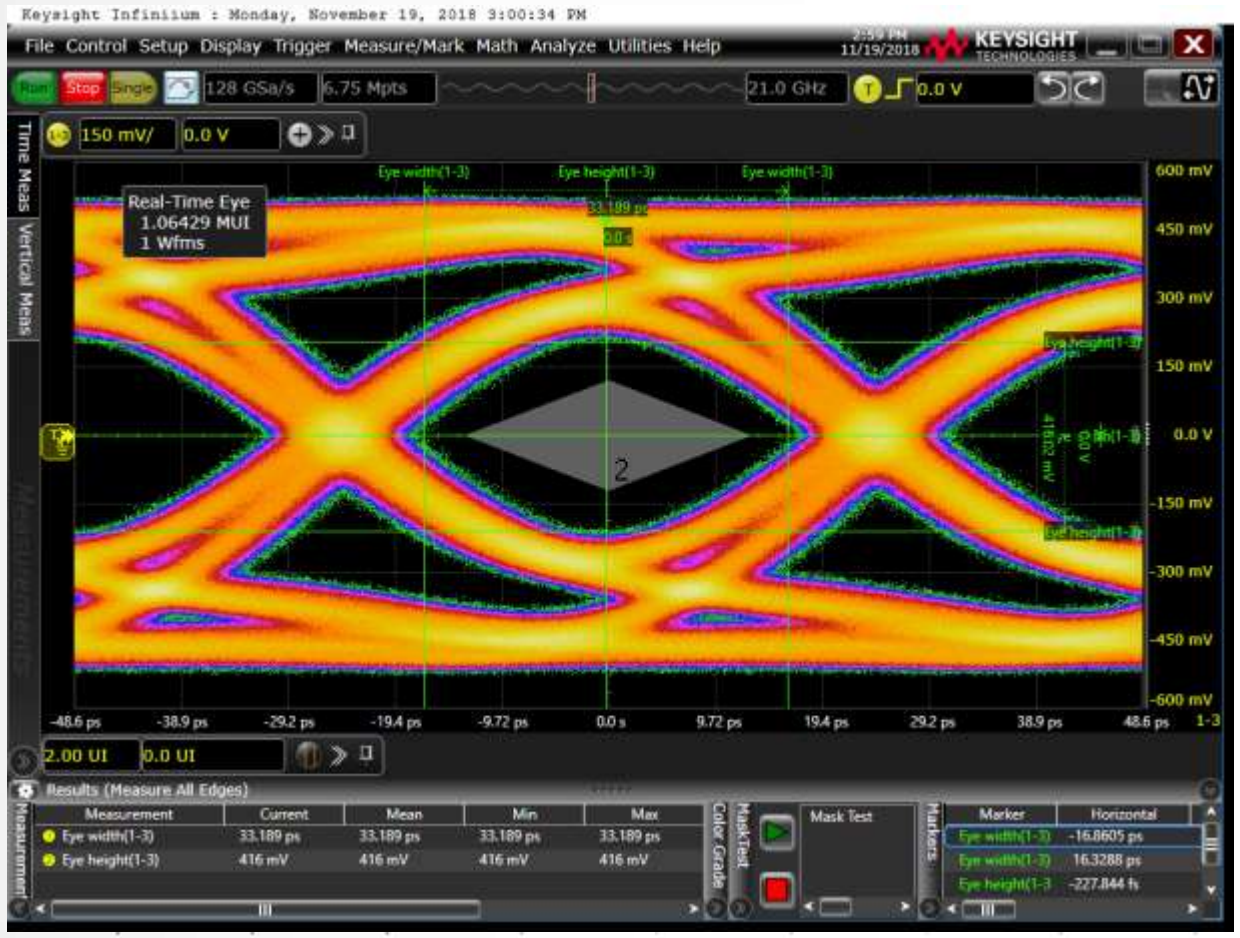
The Industry's Best Signal Integrity

- **Lowest noise**
  - < 900 µV rms @ 110 GHz
  - < 500 µV rms @ 70 GHz
  - < 300 µV rms @ 33 GHz
- **Lowest intrinsic jitter**
  - 20 fs rms
- **Lowest inter-channel jitter**
  - 10 fs rms
- **Highest ENOB**
  - > 5.0 bits @ 110 GHz
  - > 5.4 bits @ 70 GHz
  - > 5.9 bits @ 33 GHz
- **Best EVM**
  - 1.22% for 802.11ay at 61.5 GHz

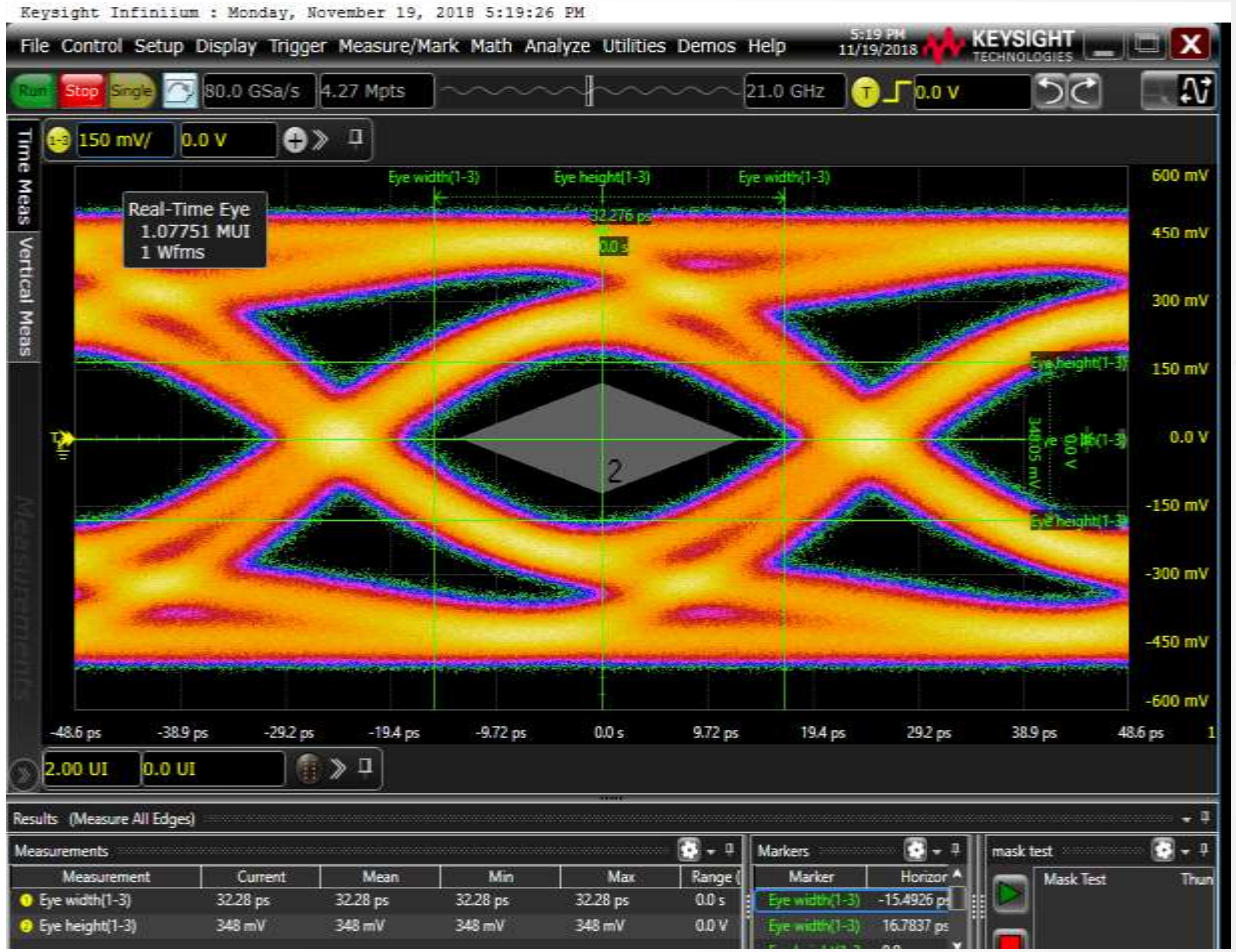
KEYSIGHT TECHNOLOGIES

TBT3/USB4/DP2 Eye (no cable model, no EQ)

UXR series



V series

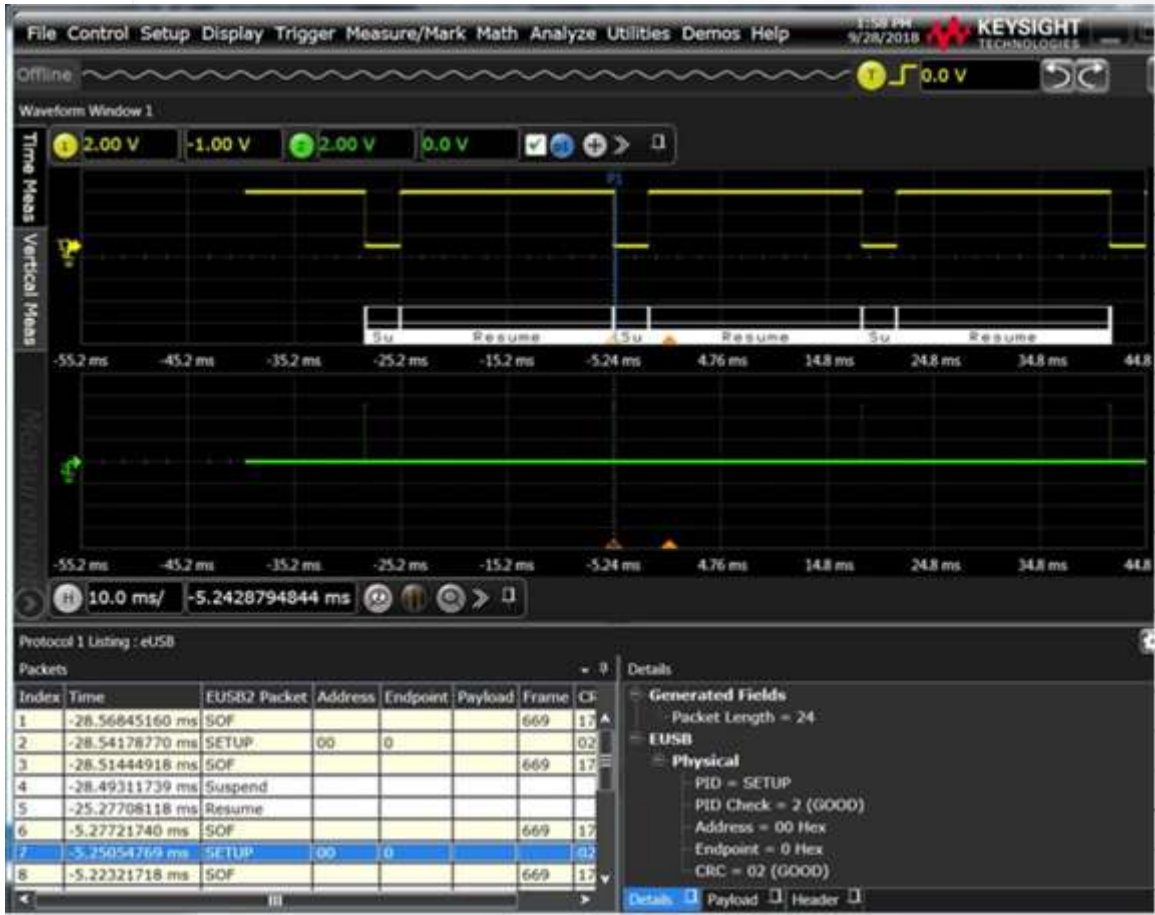


Eye width = 33.1 ps
Eye height = 416 mV

Eye width = 32.2 ps
Eye height = 348 mV

eUSB2 Solutions Overview

- Protocol decode/trigger/search (D9010EMBP) for eUSB2 supports the same features as USB2 decode/trigger/search. Can show eUSB2 and USB2 in parallel on both sides of system or repeater.
- Pattern Generator (81160A) can be programmed to generate eUSB2 or USB2 traffic into system or repeater.
- Scope can be used with custom masks to electrical test eUSB2 embedded (probes or SMA).
- Existing N5416A/B USB2 compliance app can test electrical eUSB2 at connector port. Modifications required to USB-IF USBET20 tool.



Type-C Test Solution

Design Simulation, Protocol Decode, USB-PD, RF, Channel Characterization, SBU, Thunderbolt, DP

SW

HW

Fixture

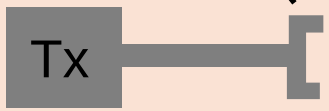
DUT

Transmitter Test
Active Cable Test

Automated Standards Test Software

UXR Infiniium Scope <1mV RMS <25fs RMS

Tx Test Fixture



Interconnect Test
Return Loss Test

E5080B ENA with S96011A Enhanced TDR software

Cable/Connector Test Fixture

Cable

Receiver Test
Active Cable Test

Automated Standards Test Software

M8000 Integrated Protocol J-BERT <200fs RMS

Test Fixture