



**KEYSIGHT
WORLD 2020**

Improve Device Performance Using Power Integrity Test Tools

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Sr. Application Engineer / Keysight Technologies

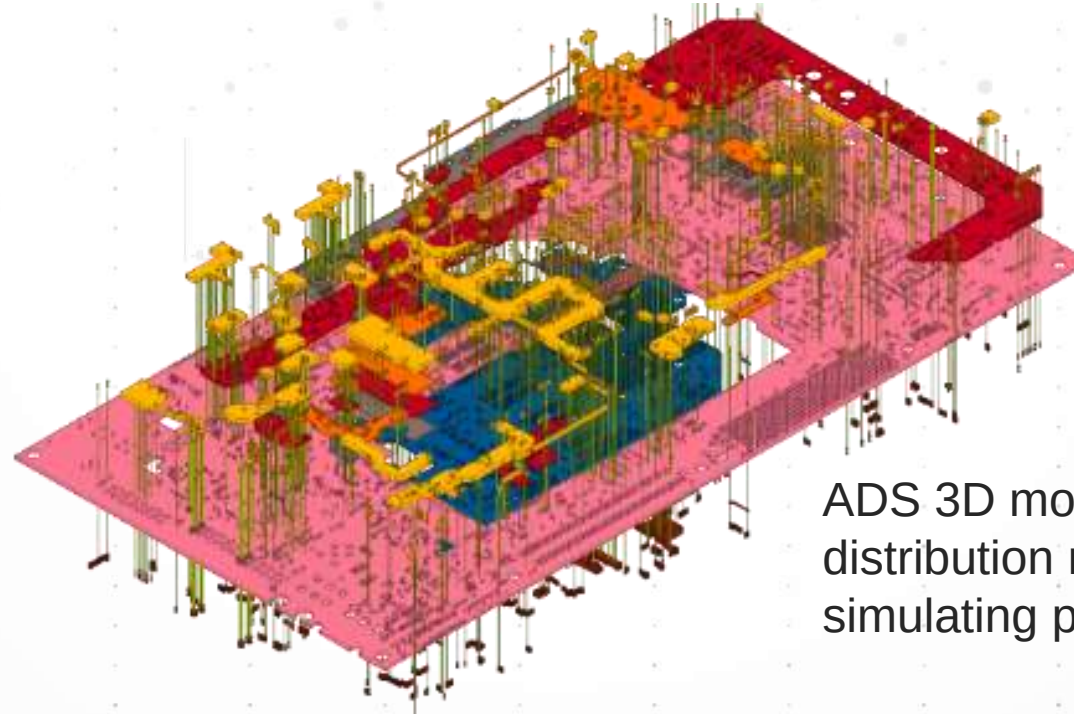


Power Integrity (PI)

WHAT ARE WE TALKING ABOUT

Power Integrity: The study of the conversion, delivery and consumption of DC power in an electronic system. *Kenny Johnson, Keysight*

Product Functional Reliability $\propto$ Quality of the system power



ADS 3D model of power distribution network (PDN) for simulating power integrity

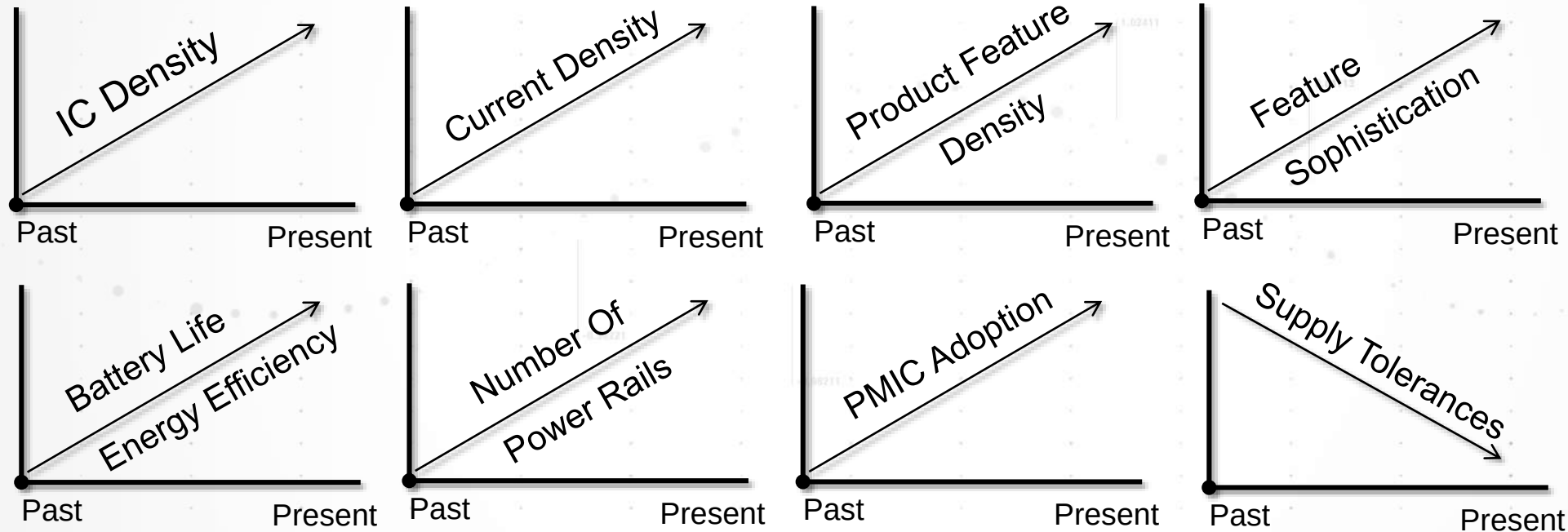
Why is Power Integrity critical to your design



Power Integrity

WHY?

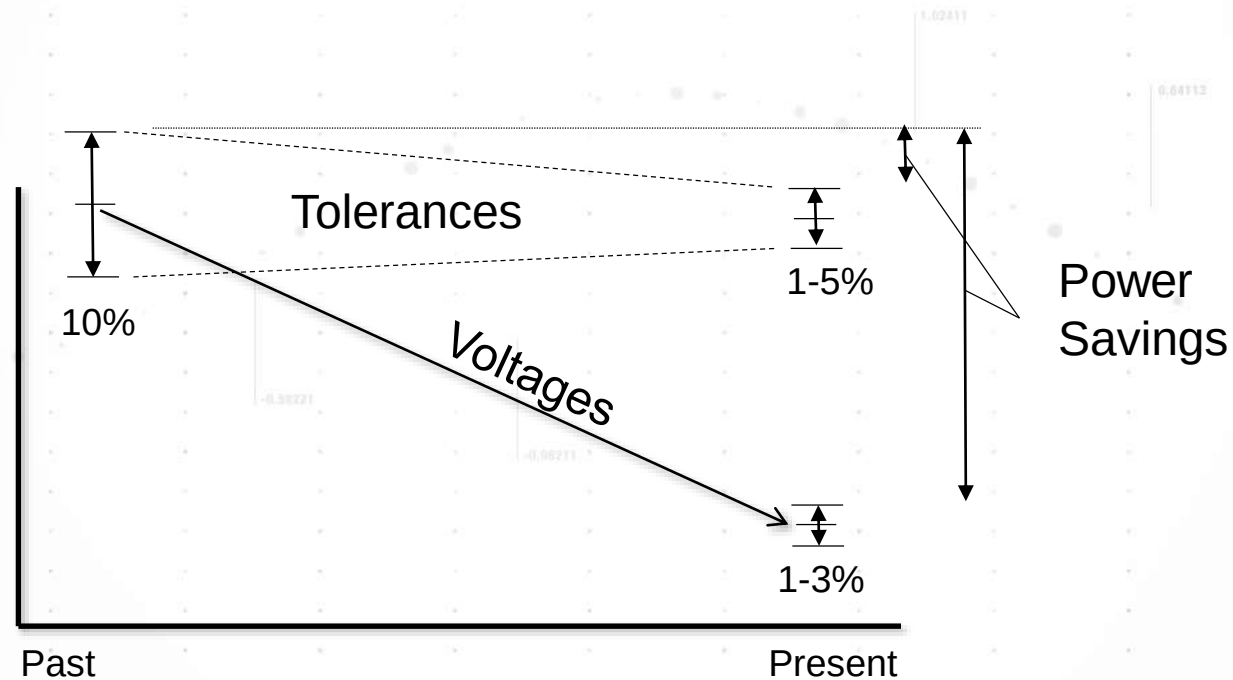
- Moore's Law: transistors on an integrated circuit will double every two years.



Power Integrity

WHY? POWER AND CURRENT DENSITY

- Operating voltages are decreasing to reduce power and/or in support of finer pitch IC processes.

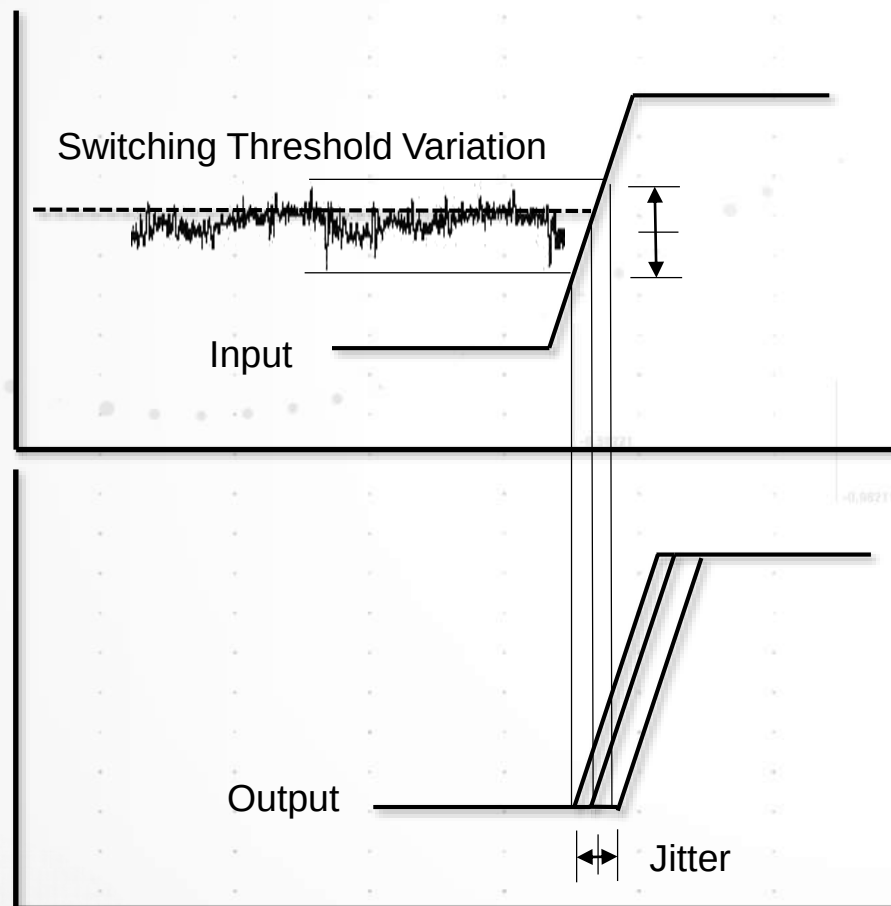


Power Integrity

WHY? POWER SUPPLY INDUCED JITTER (PSIJ)

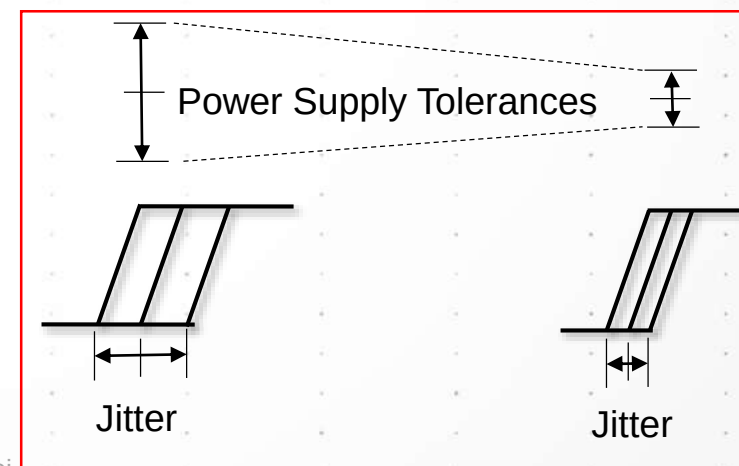
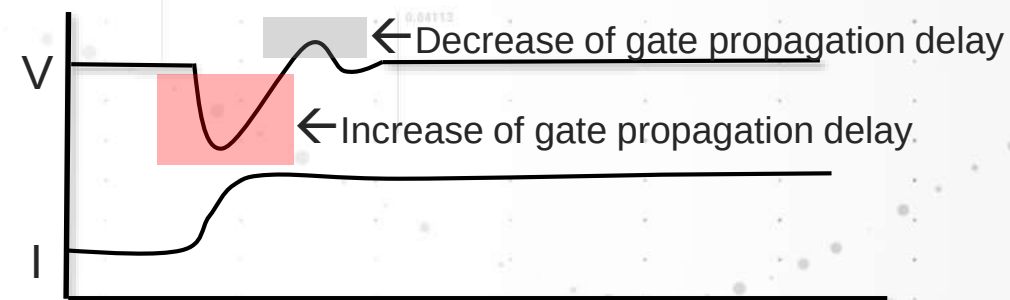
- Power supply noise causes clock/data jitter

Example 1:



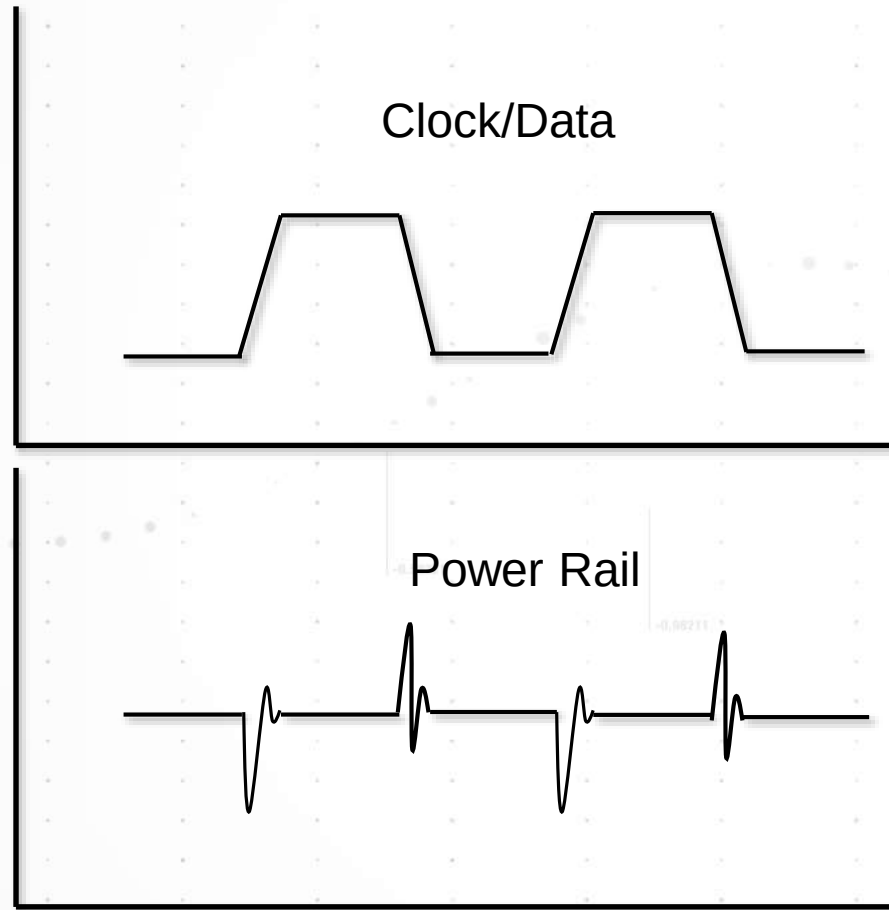
Example 2: CPU/APU/ μ

Variations in core voltages cause variations in propagation delay through the gates of the processor.



Power Integrity

NOT JUST DC: SWITCHING LOADS

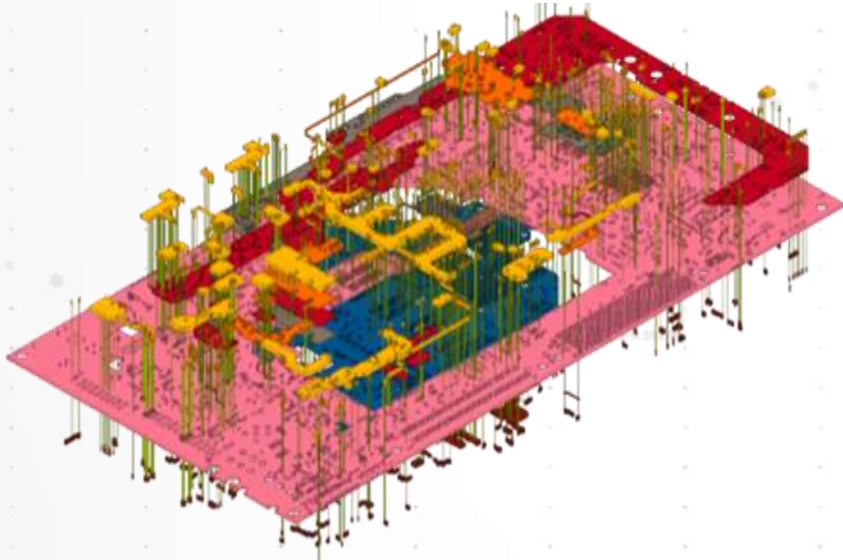


Switching loads can cause high frequency supply noise with content easily exceeding 1GHz

Power rails must be stable from DC to the BW of the switching current

Power Integrity

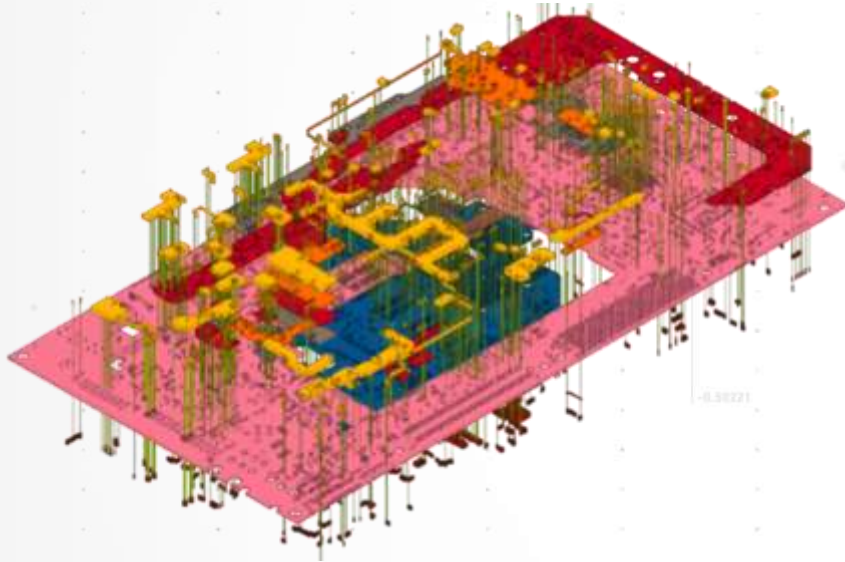
WHY? EMI



- PDN is likely to be the biggest conducting structure.
- PDN is likely to carry high current.
- PDN is likely to have high frequency noise.

Power Integrity

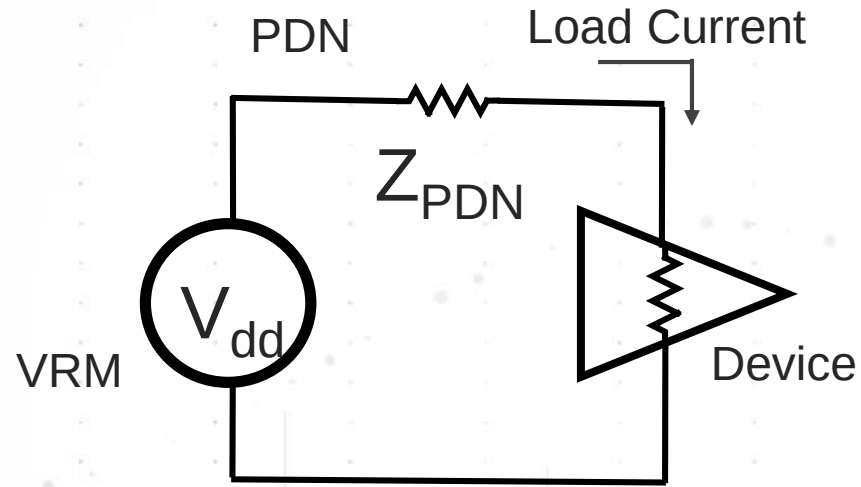
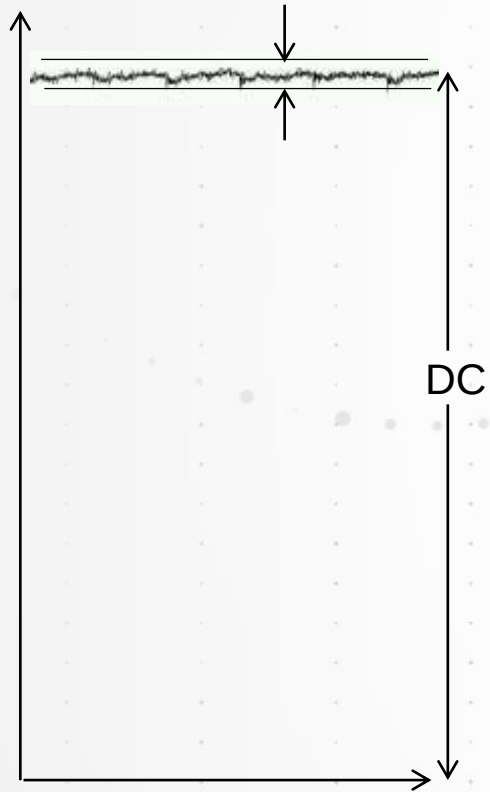
A WELL DESIGNED PDN



- A well designed PDN will maintain a stable voltage (within tolerance) from DC to the bandwidth of the switching current (typically above 1GHz).
- This will help:
 - Optimize power consumption
 - Minimize switching noise (SSN—simultaneous switching noise)
 - PSIJ (dropped bits, missed clock ...)
 - Minimize EMI problems
- Therefore, one the primary validation tasks is measuring power rail quality.

Power Integrity

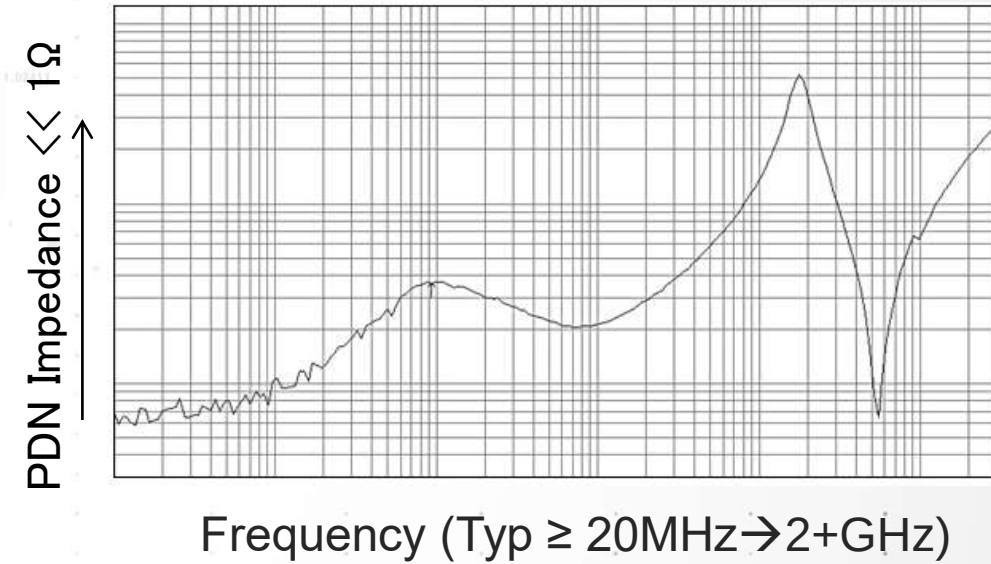
PDN THEORY AND MODELING



$$Z_{\text{target}}(f) = Z_{PDN}(f) < \frac{V_{\text{Ripple}}}{I(f)}$$

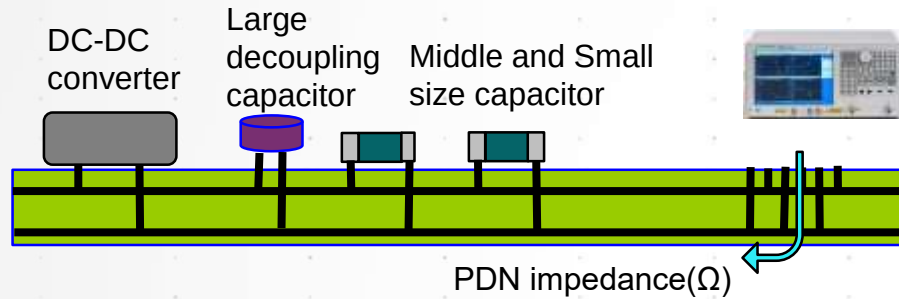
$$I_{\text{transient}} \sim (1/2) * I_{\text{max}}$$

$$I_{\text{peak}} = P_{\text{max}} / V_{dd} \rightarrow Z_{\text{target}}(f) = \frac{2 * (V_{dd})^2 * (\text{ripple}\%)}{P_{\text{max}}}$$



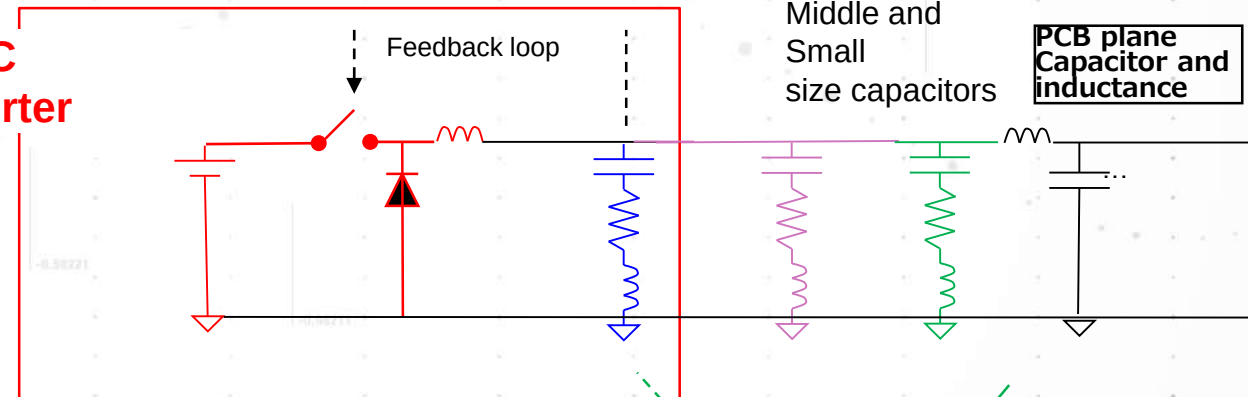
Power Integrity

PDN IMPEDANCE

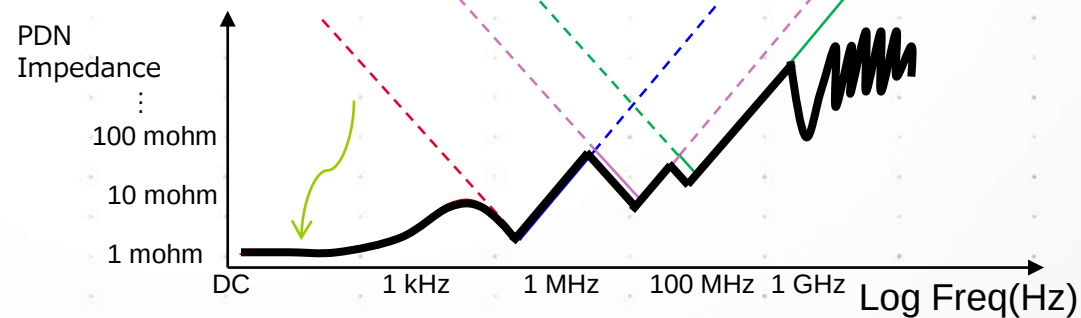


PDN impedance measurement at IC position.

DC-DC converter

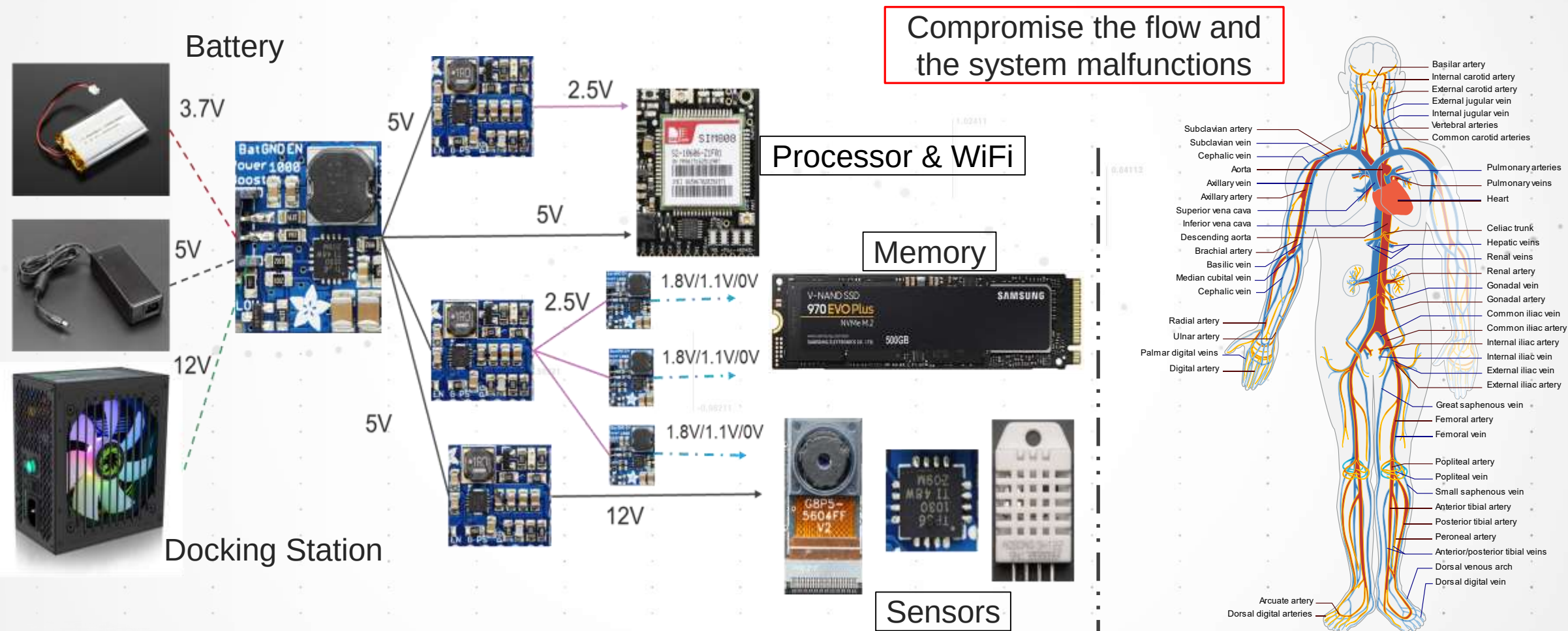


PDN impedance measurement at IC position.



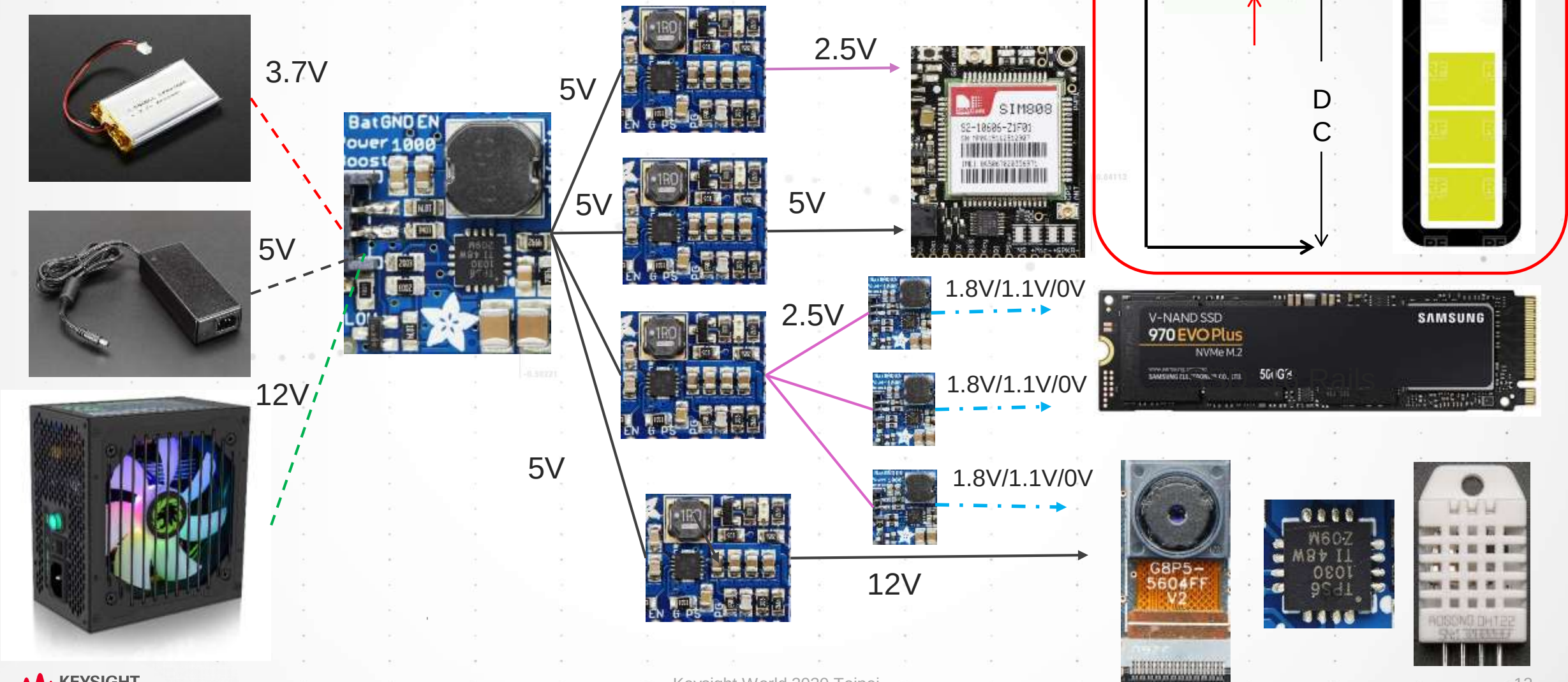
Power Integrity (PI)

SIGNIFICANCE OF DC POWER



Power Integrity (PI)

JOB OF PI ENGINEER



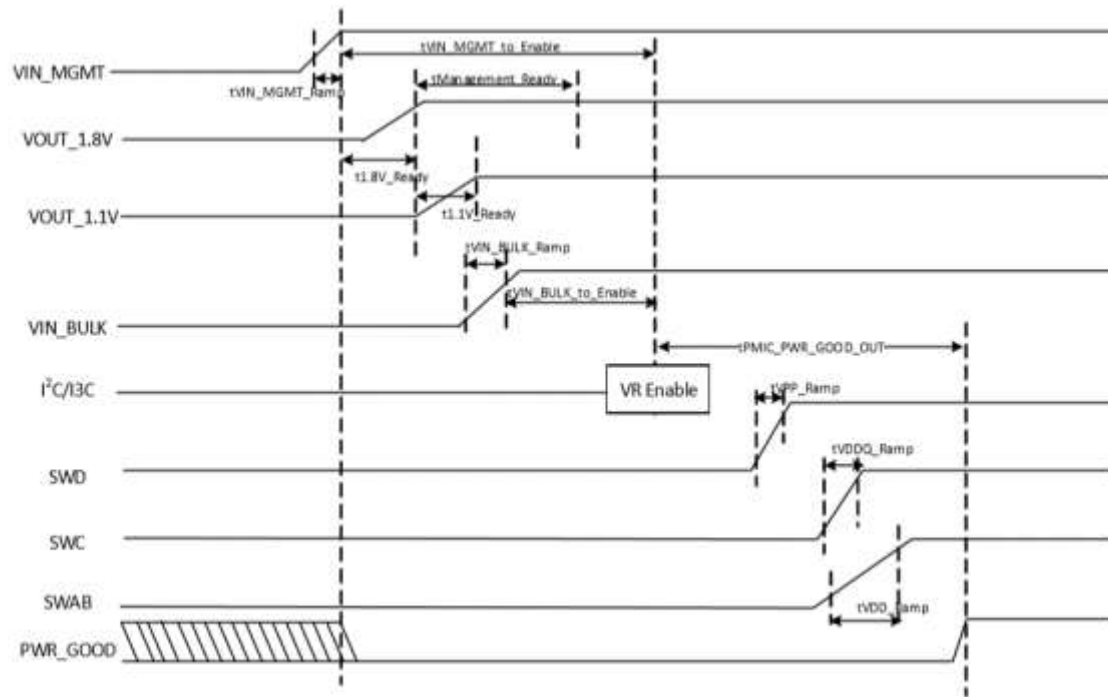
Power Sequencing



Power Integrity (PI)

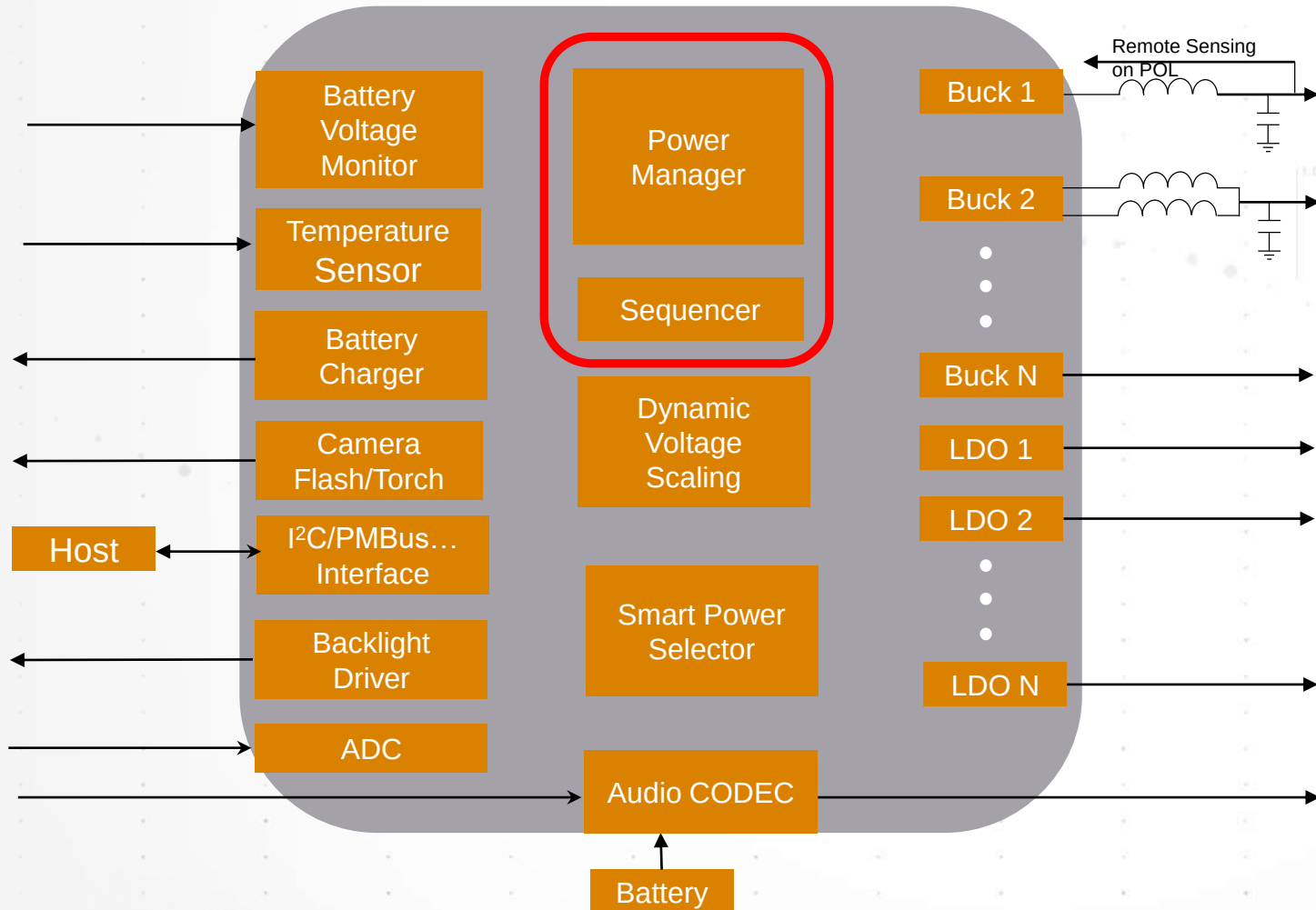
ADDED COMPLEXITY—POWER SEQUENCING

Power Sequence Specification



Power Integrity (PI)

POWER MANAGEMENT IC (PMIC)



Power Integrity (PI)

PMIC IS THE TRAFFIC OFFICER



3.7V



5V



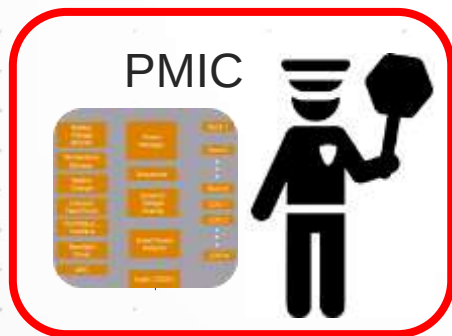
12V



5V

5V

5V



PMIC



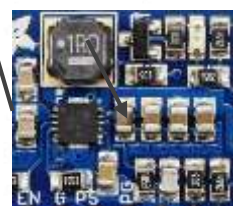
2.5V



5V



2.5V



12V



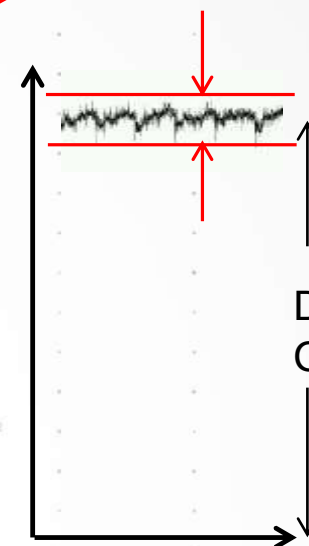
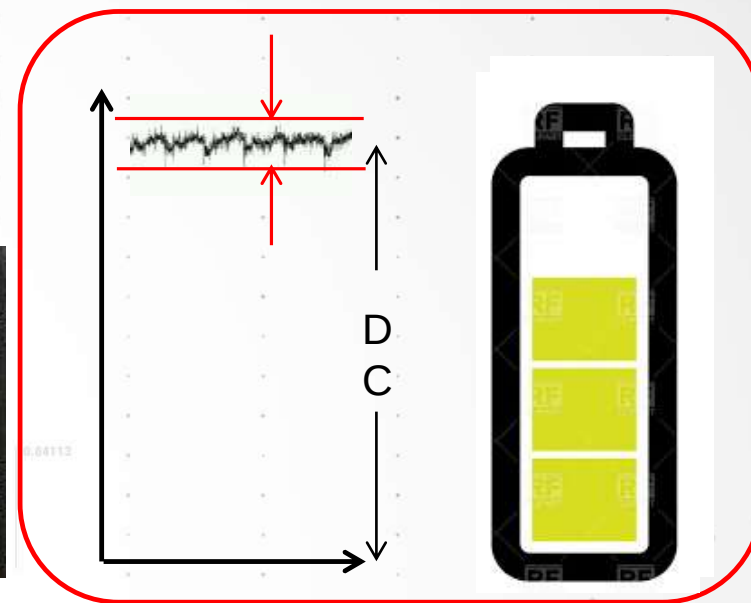
1.8V/1.1V/0V



1.8V/1.1V/0V



1.8V/1.1V/0V



DC

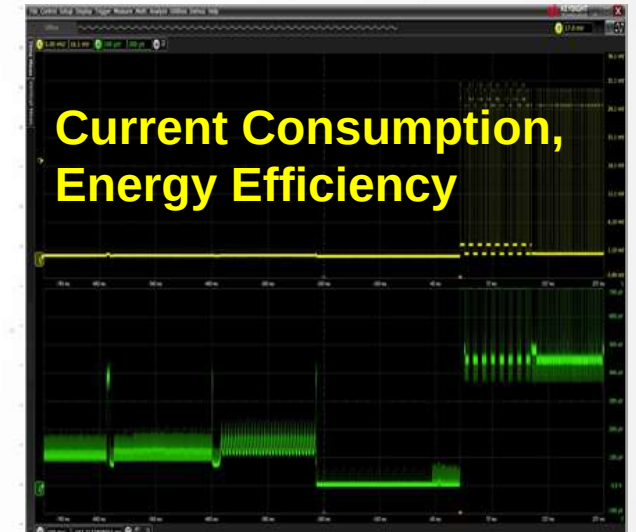
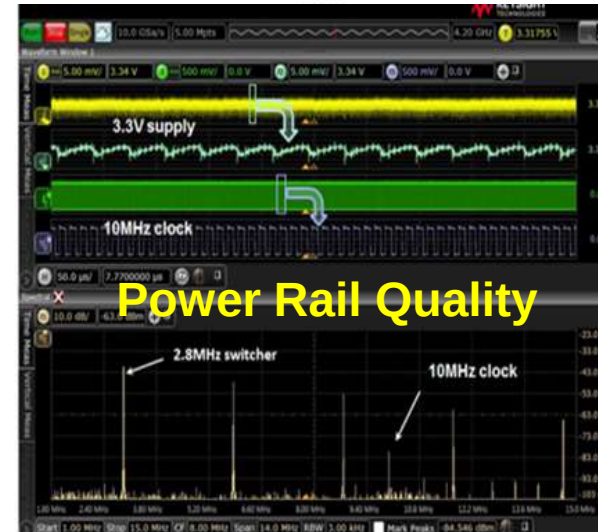
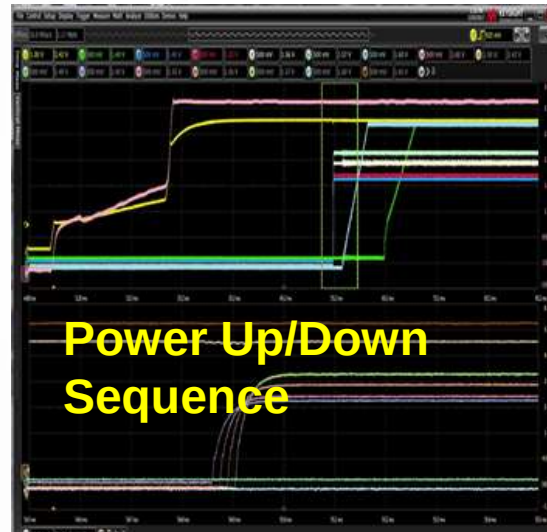


Power Integrity Test Flow



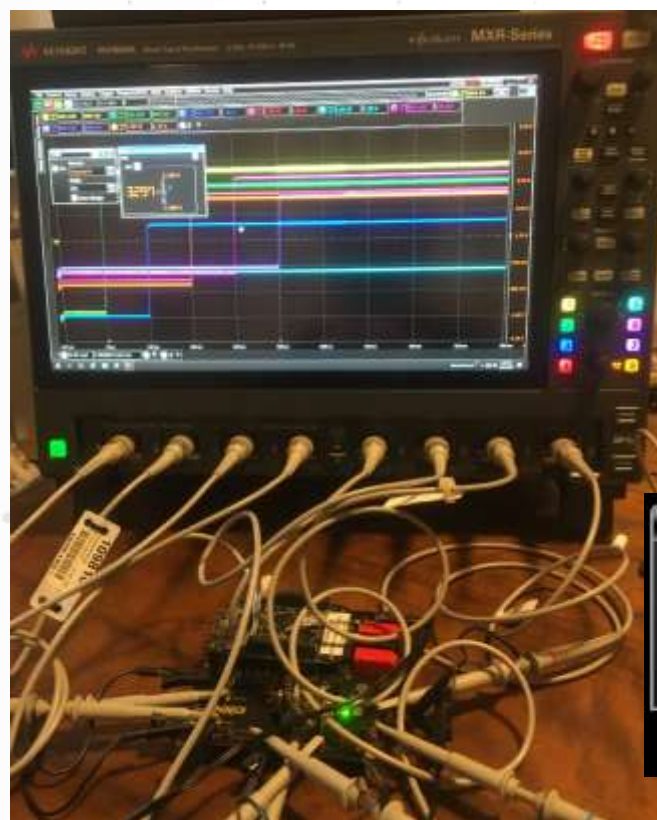
Power Integrity (PI)

TYPICAL TEST FLOW



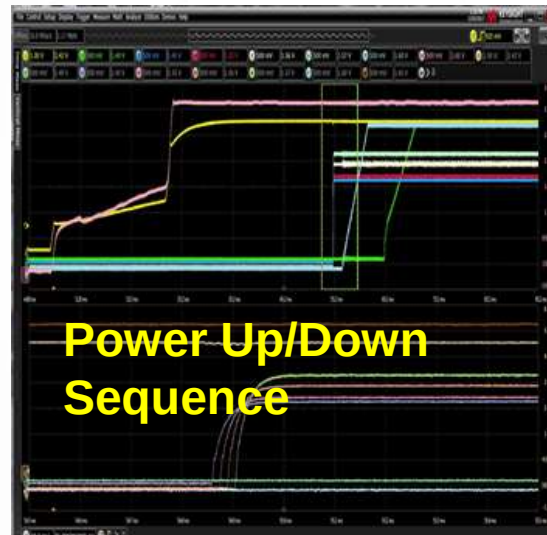
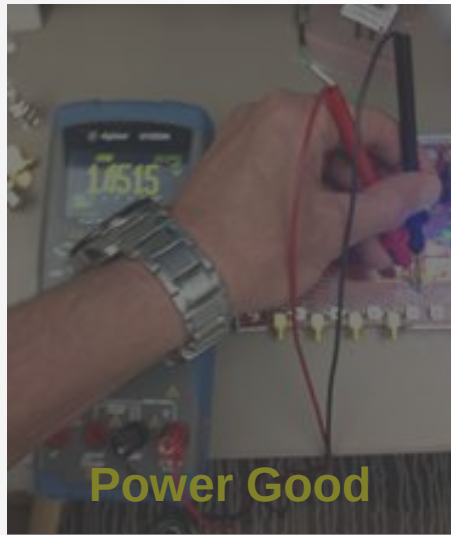
Power Integrity

POWER-GOOD USING MXR DVM



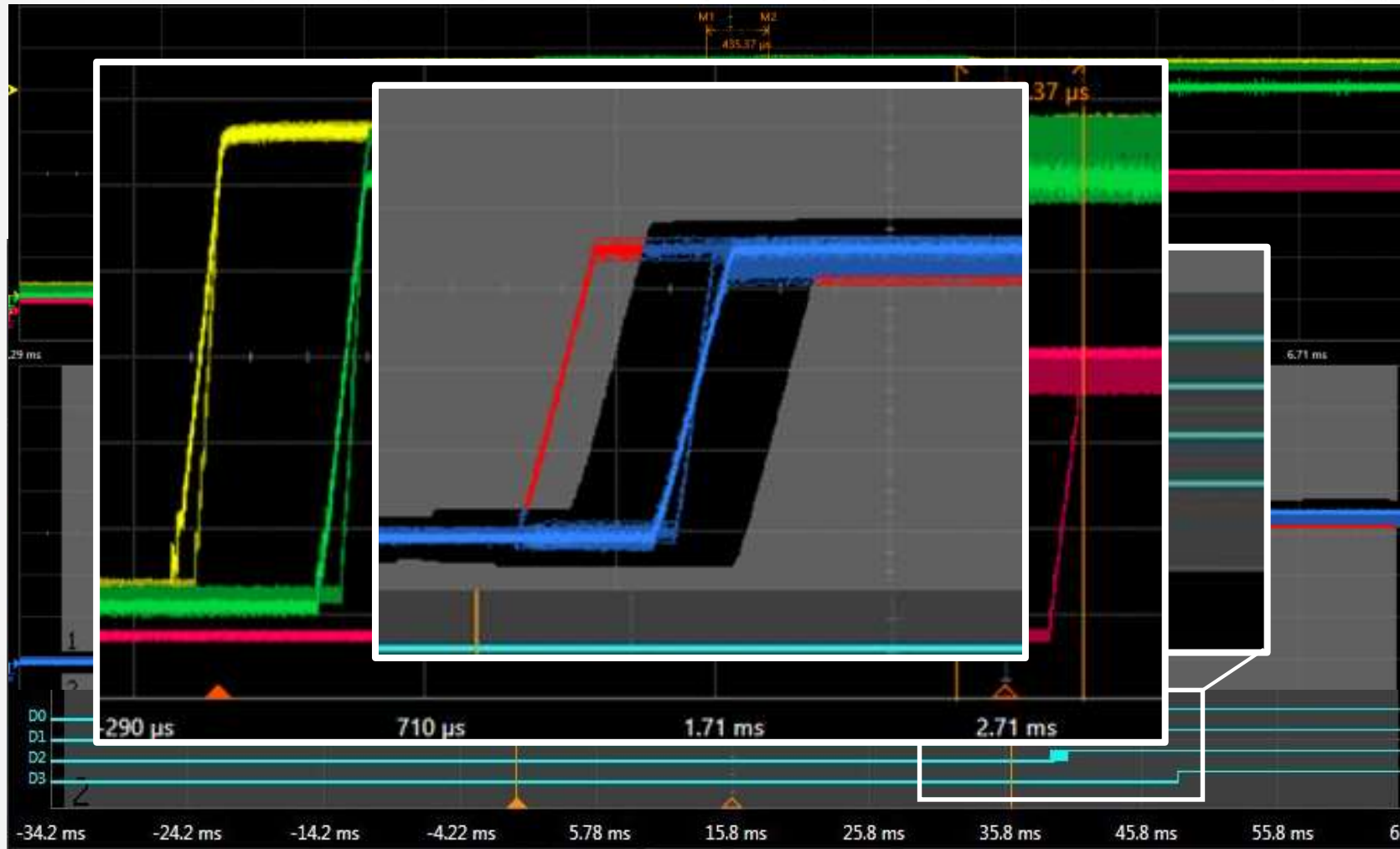
Power Integrity (PI)

TYPICAL TEST FLOW



PMIC Testing

POWER SEQ.—EX. 8 RAILS, PERSISTENCE & DIGITAL



Digital Persistence

- Not hard to generate
- Non-invasive (runners to
- Variables pass/fail measured

Issues

- Specificity
- Time consuming
- Not repeatable/human

Issues

- Only one mask available

PMIC Testing

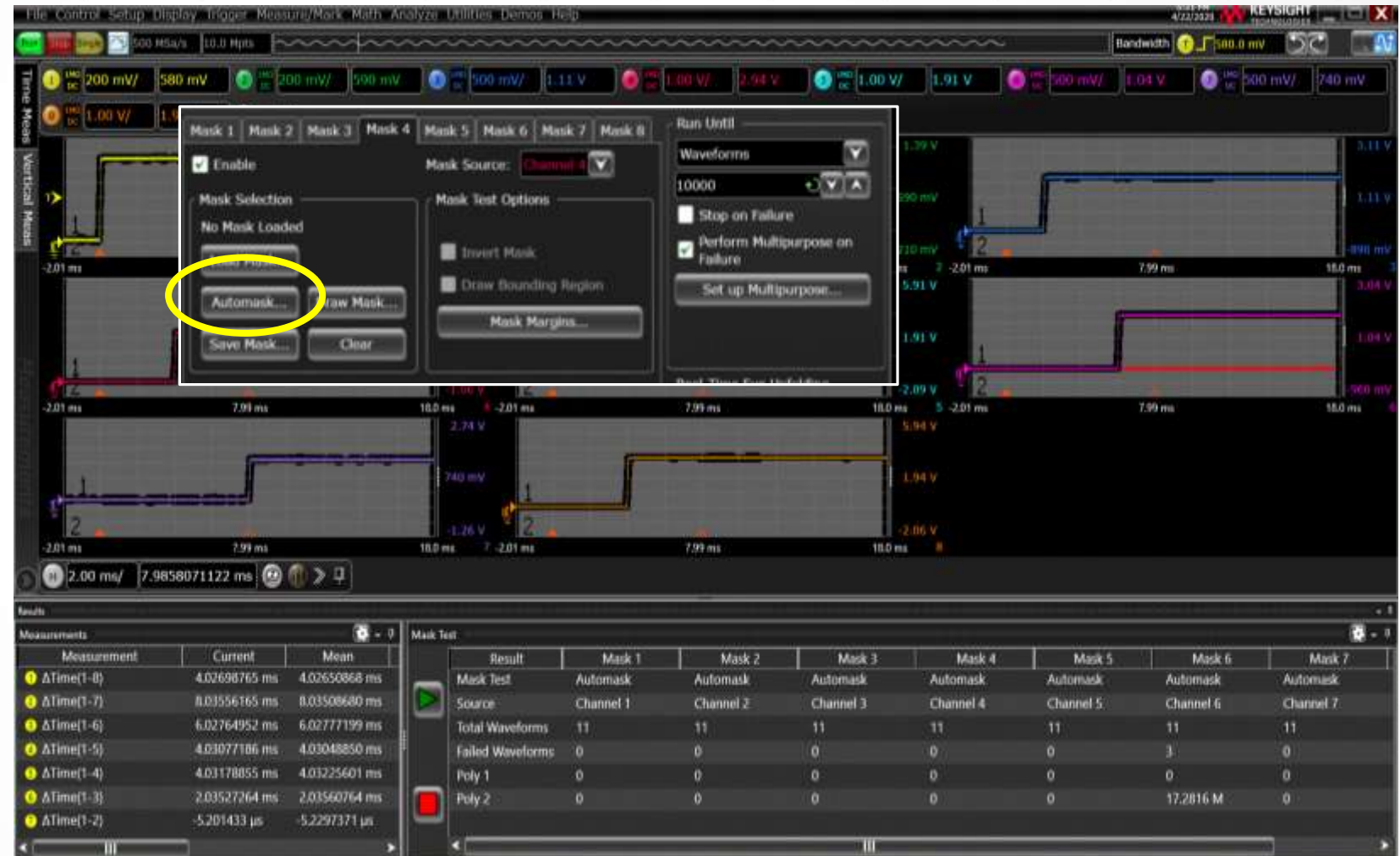
POWER SEQUENCE TESTING—MASK ON EVERY CH.

Mask for every channel

- Saves time
- Eliminates uncertainty
- Complete test report in one screen shot

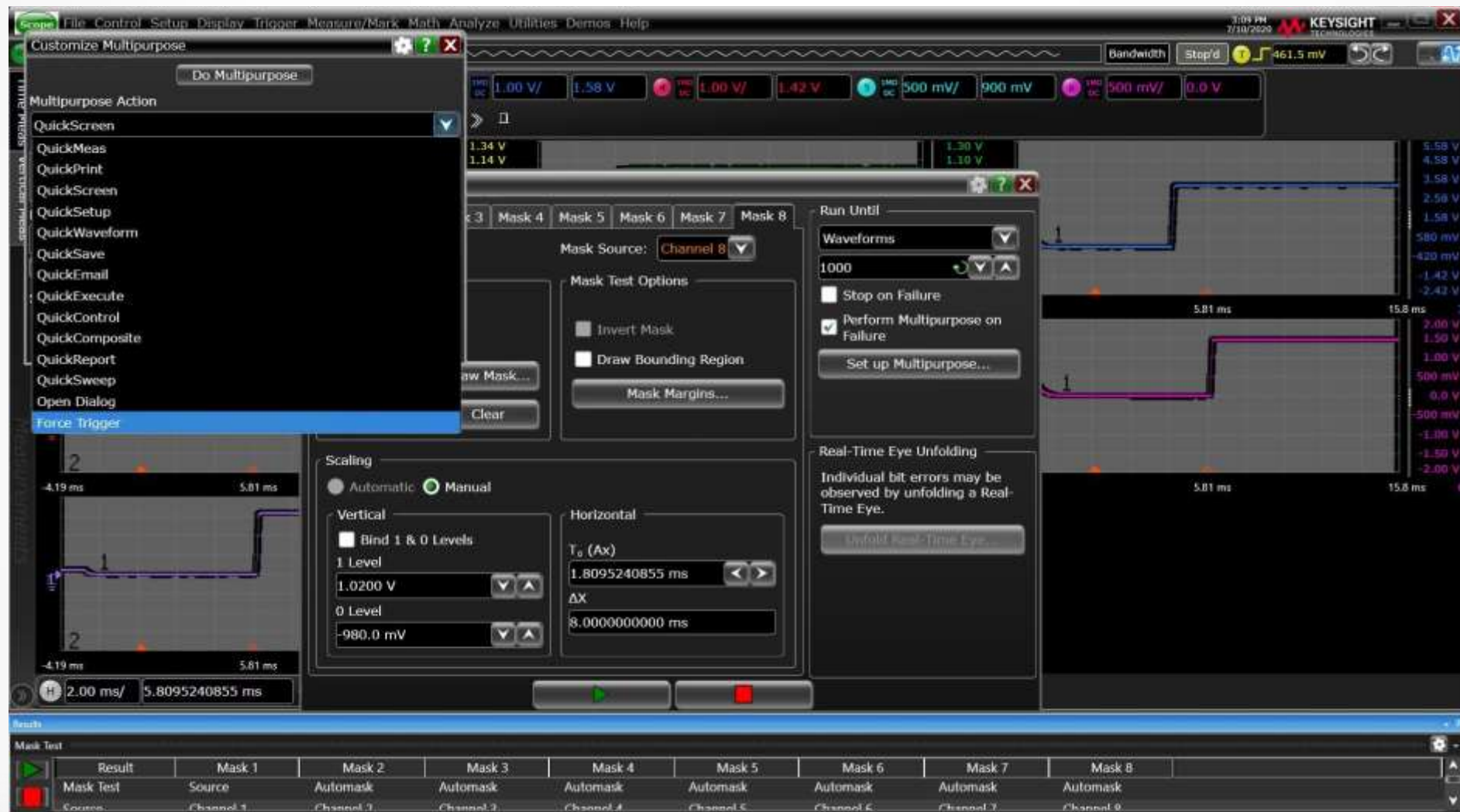
Automask

- Saves time
- Simple and easy mask setup



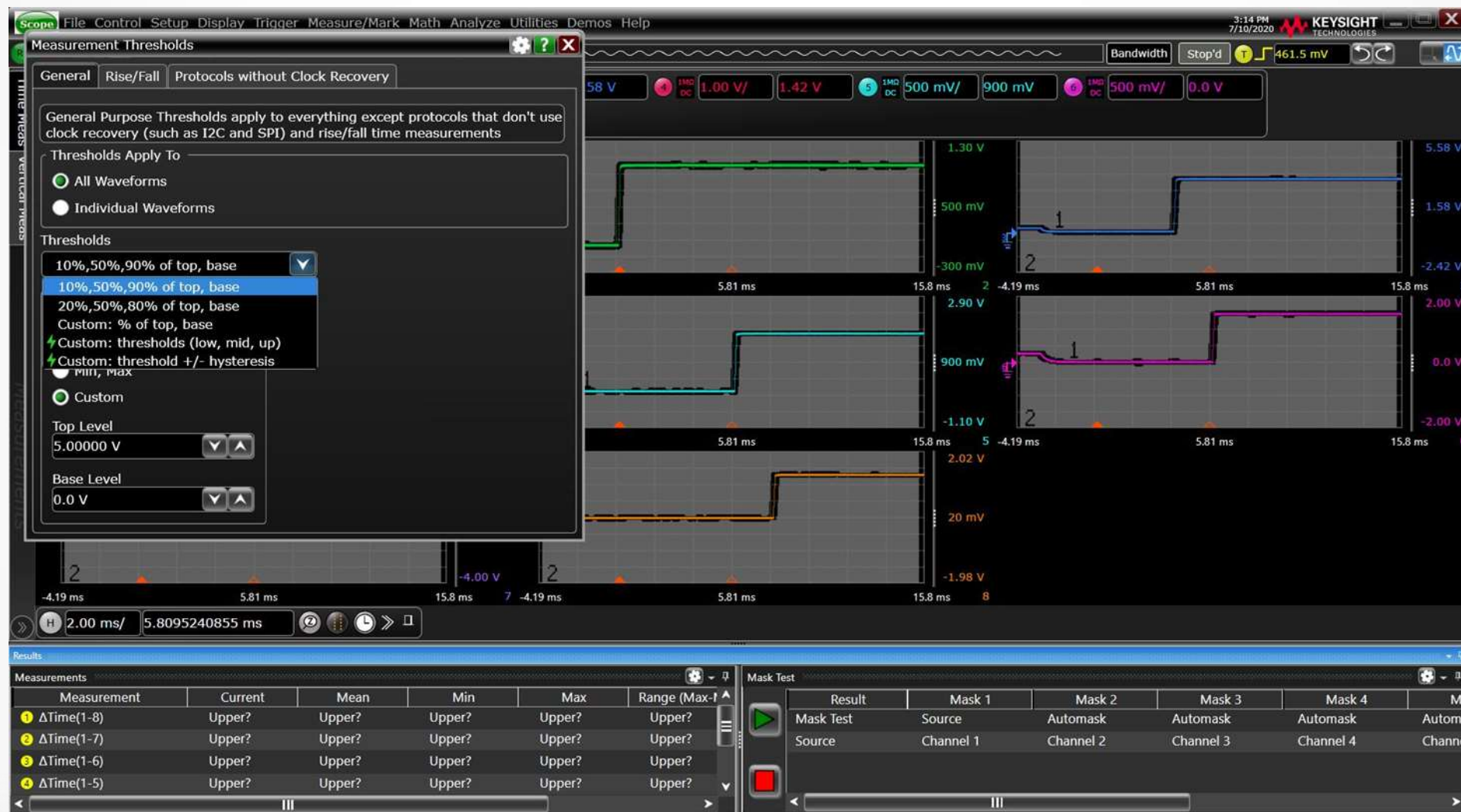
PMIC Testing

POWER SEQUENCE TESTING—MASK ON EVERY CH.



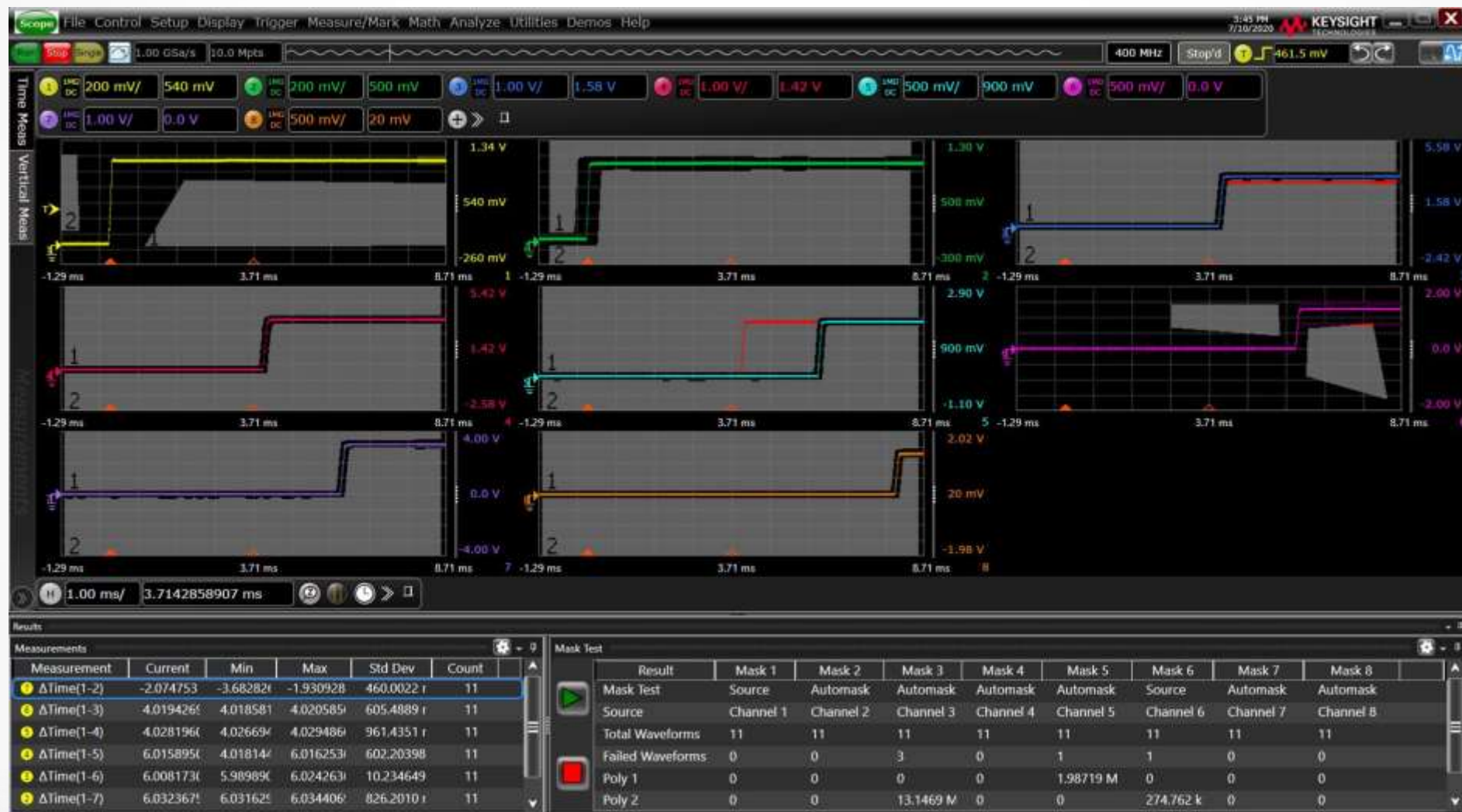
PMIC Testing

POWER SEQUENCE TESTING— Δ TIME MEASUREMENTS



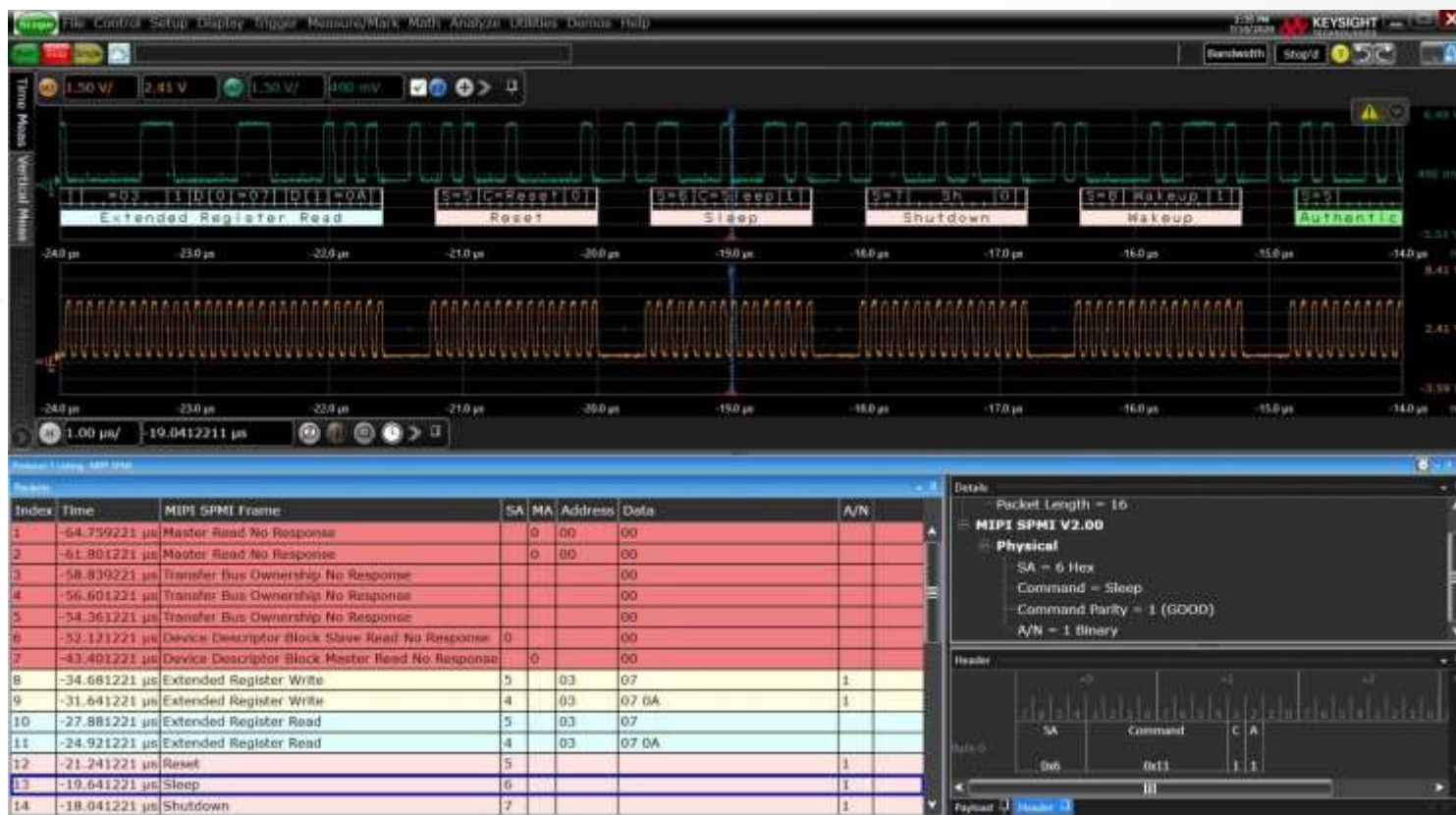
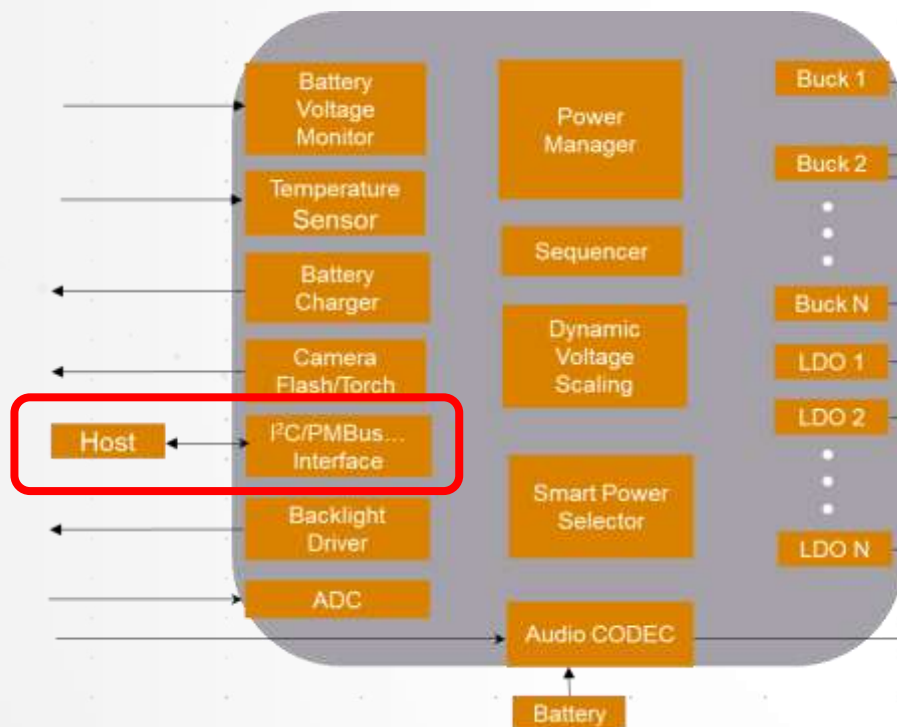
PMIC Testing

POWER SEQUENCE TESTING—ONE PAGE REPORT.



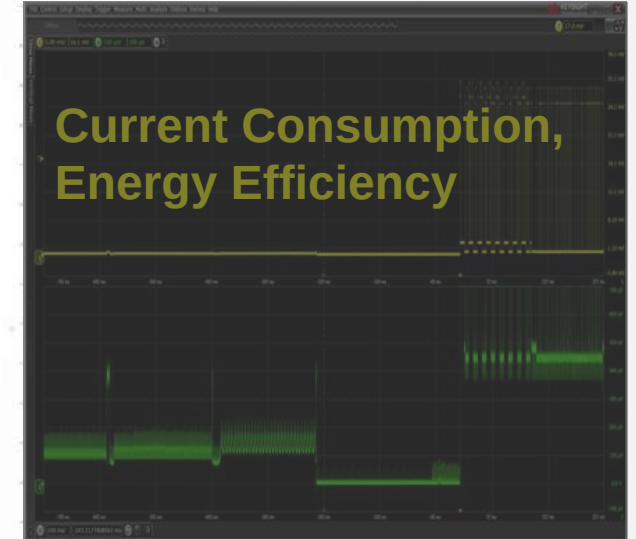
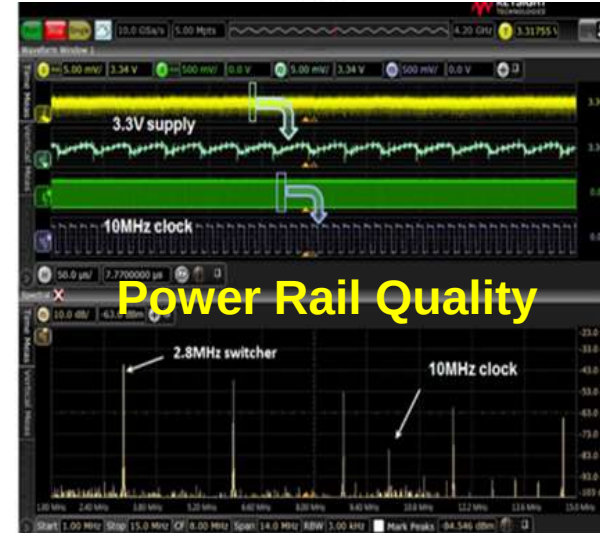
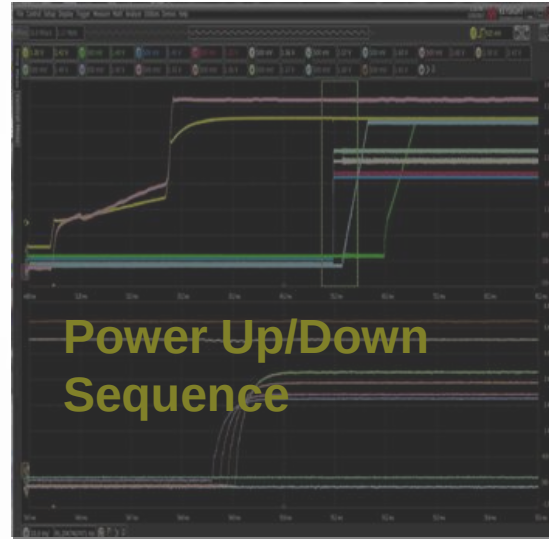
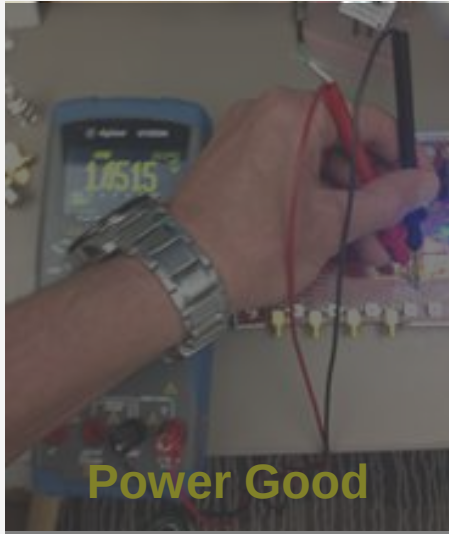
PMIC Testing

PROTOCOL DECODE AND ANALYSIS—SPMI EXAMPLE



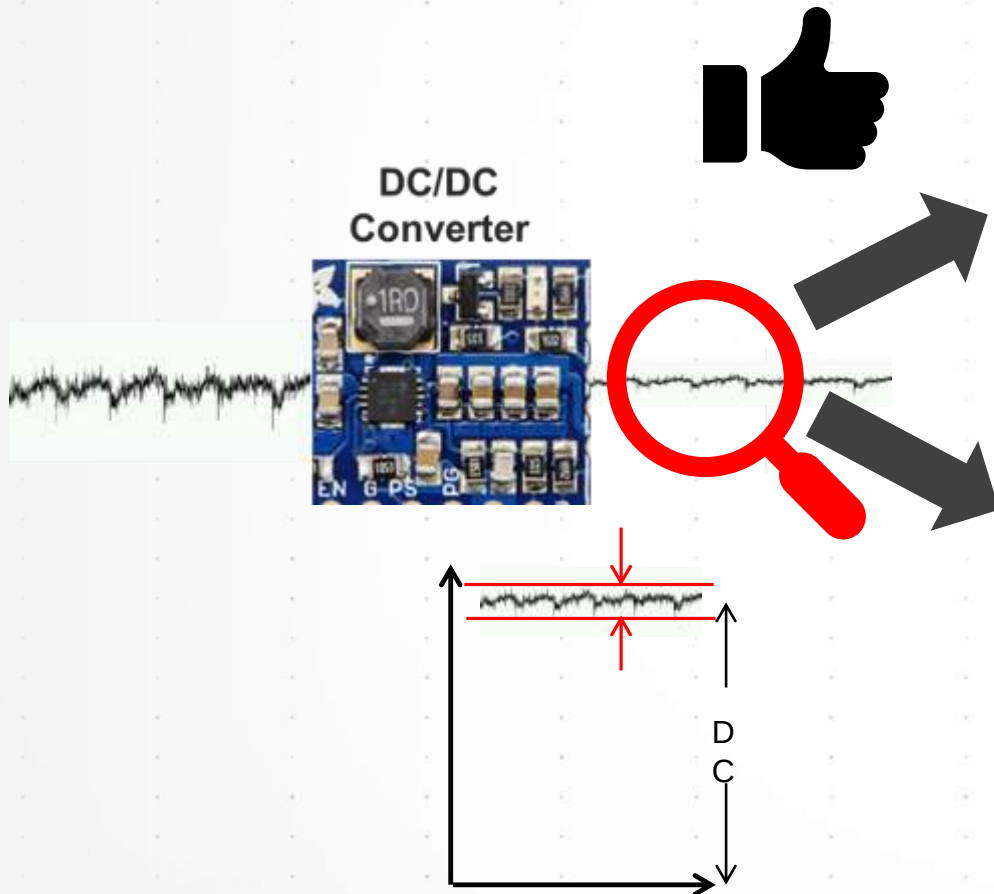
Power Integrity (PI)

TYPICAL TEST FLOW



Power Integrity

POWER RAIL QUALITY



Power Integrity

KEYSIGHT POWER RAIL PROBES FOR MXR-SERIES

- Keysight invented the Power Rail probe and their use with oscilloscopes
- Optimized for measuring the quality of power rails

N7020A
2GHz



N7024A
6GHz

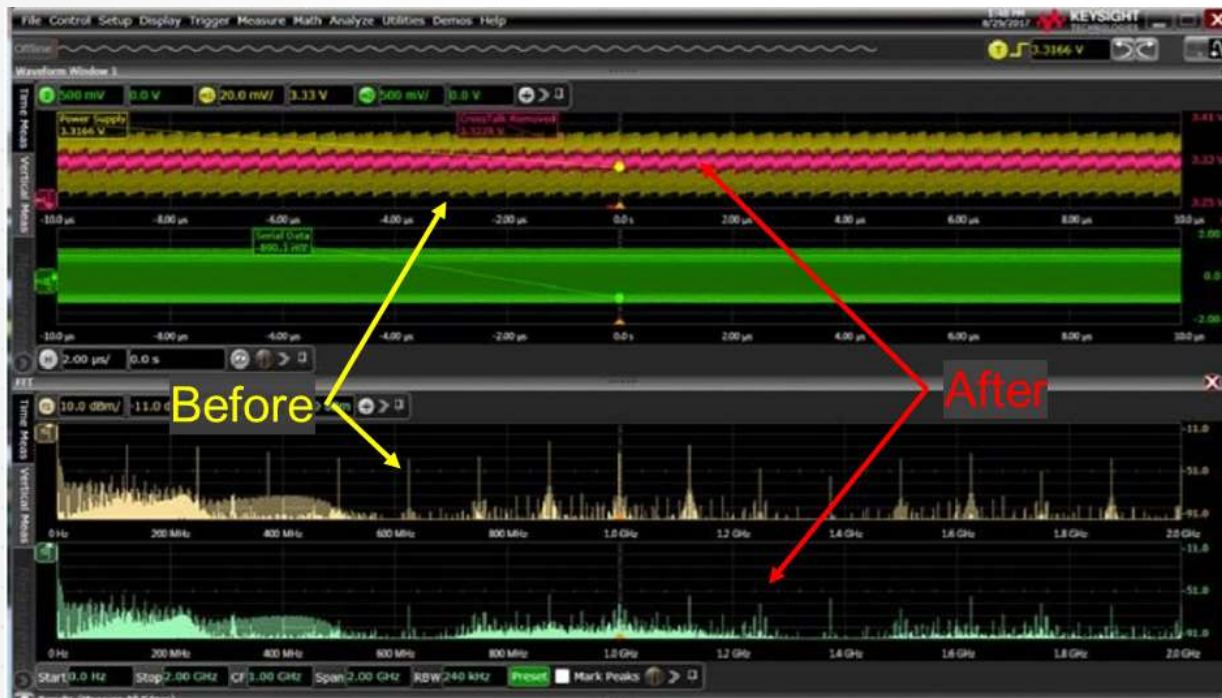


Power Integrity

D9010POWA POWER INTEGRITY ANALYSIS APP

- Helps you understand power rail noise sources and power rail noise effects

Power Rail, before (with switching loads)
& after (effects of switching loads removed)



Data Line before (with the effects of power rail noise)
& after (effects of power rail noise removed).



Power Integrity

D9010POWA POWER INTEGRITY ANALYSIS APP



Power Integrity

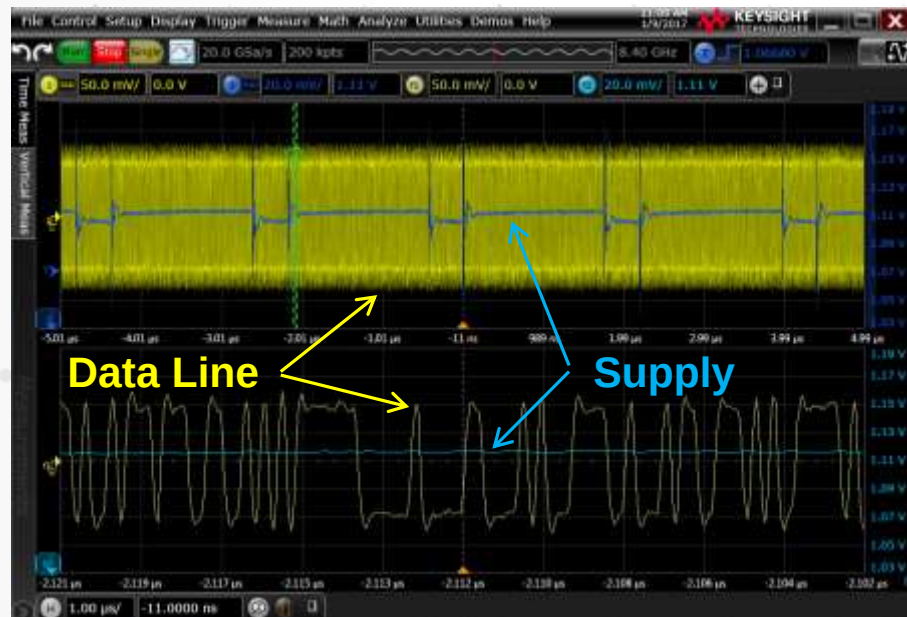
D9010POWA POWER INTEGRITY ANALYSIS APP



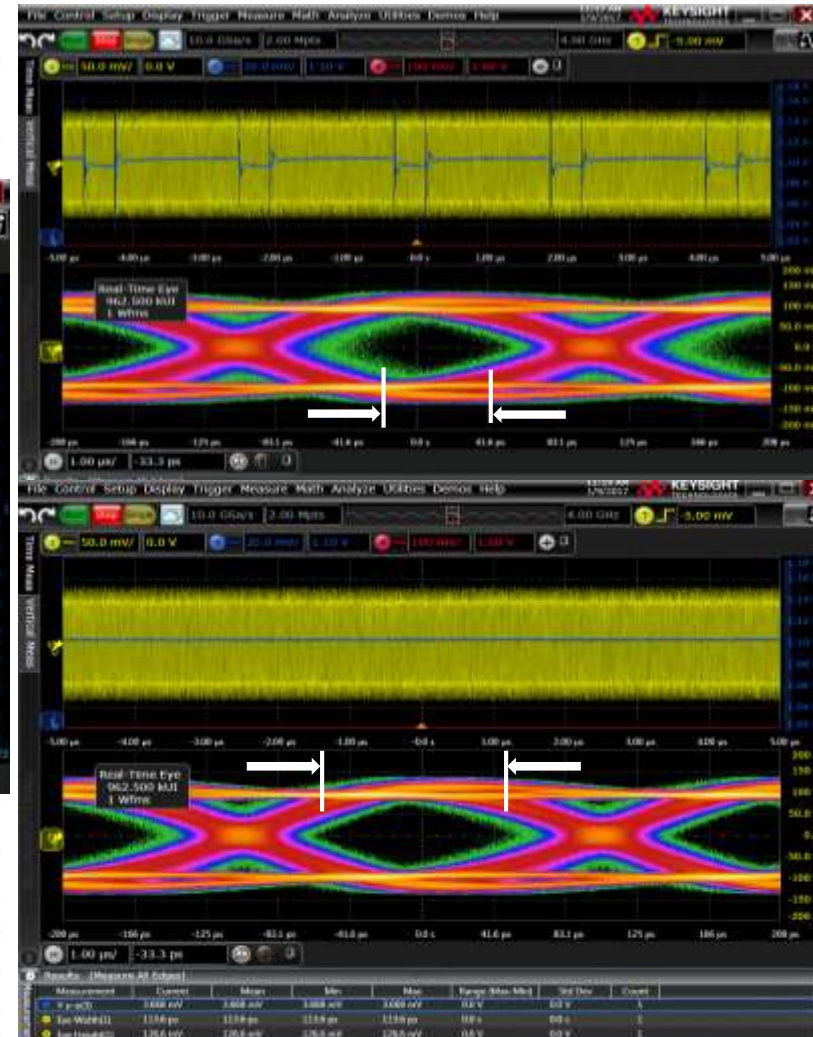
Power Integrity

D9010POWA POWER INTEGRITY ANALYSIS APP

1.10V Supply with 115mV_{pp} Noise (±5%)



1.10V Supply with 3mV_{pp} Noise



Power Integrity

D9010POWA POWER INTEGRITY ANALYSIS APP



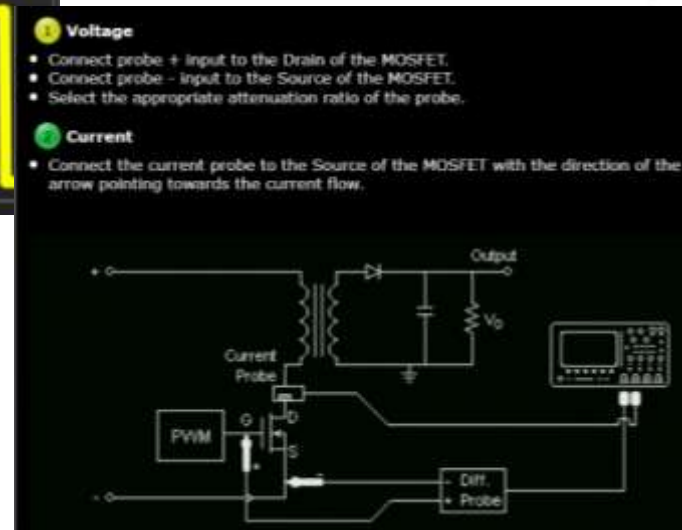
Power Integrity

D9010PWRA—POWER ANALYSIS APPLICATION

- Automated, time saving analysis of switch mode and linear power supplies
 - 20 measurements



- 'Setup Wizard' provides clear directions.



Type of analysis

Input measurements

Measurement

Power quality

- Real power
- Apparent power
- Reactive power
- Power factor
- Crest factor
- Phase angle

Current harmonics

Inrush current

Switching loss

Rds(on)

Vce(sat)

Slew rate

Safe operating area

Output ripple

Turn-on time

Turn-off time

Efficiency

Transient response settling time

Power supply rejection ratio (PSRR)

Control loop response (gain and phase)

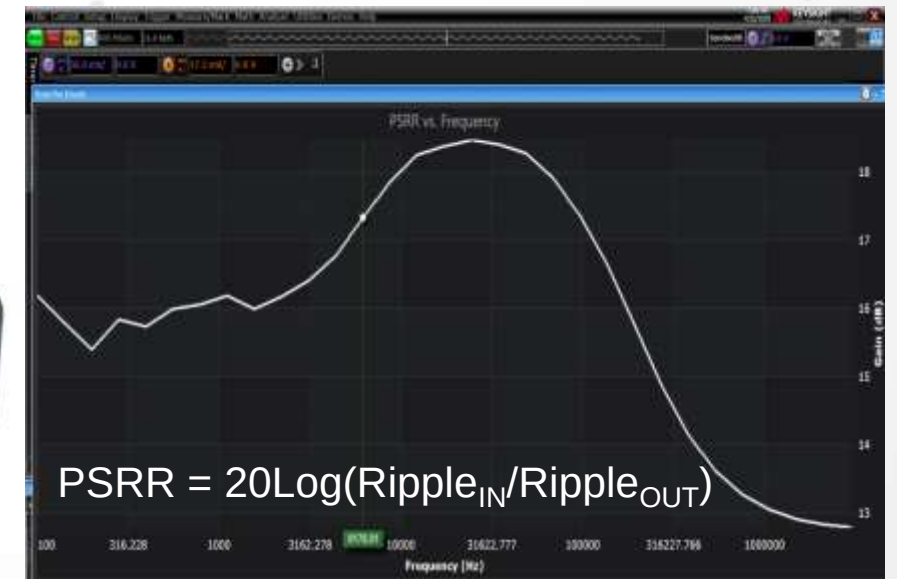
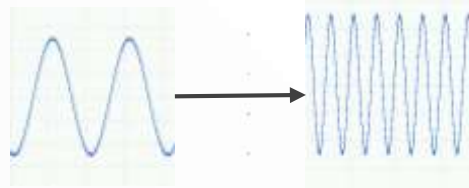
Power Integrity

POWER SUPPLY REJECTION RATIO--PSRR

- PSRR is a measure of how well a DC-DC converter can reject noise on the input from getting to the output.

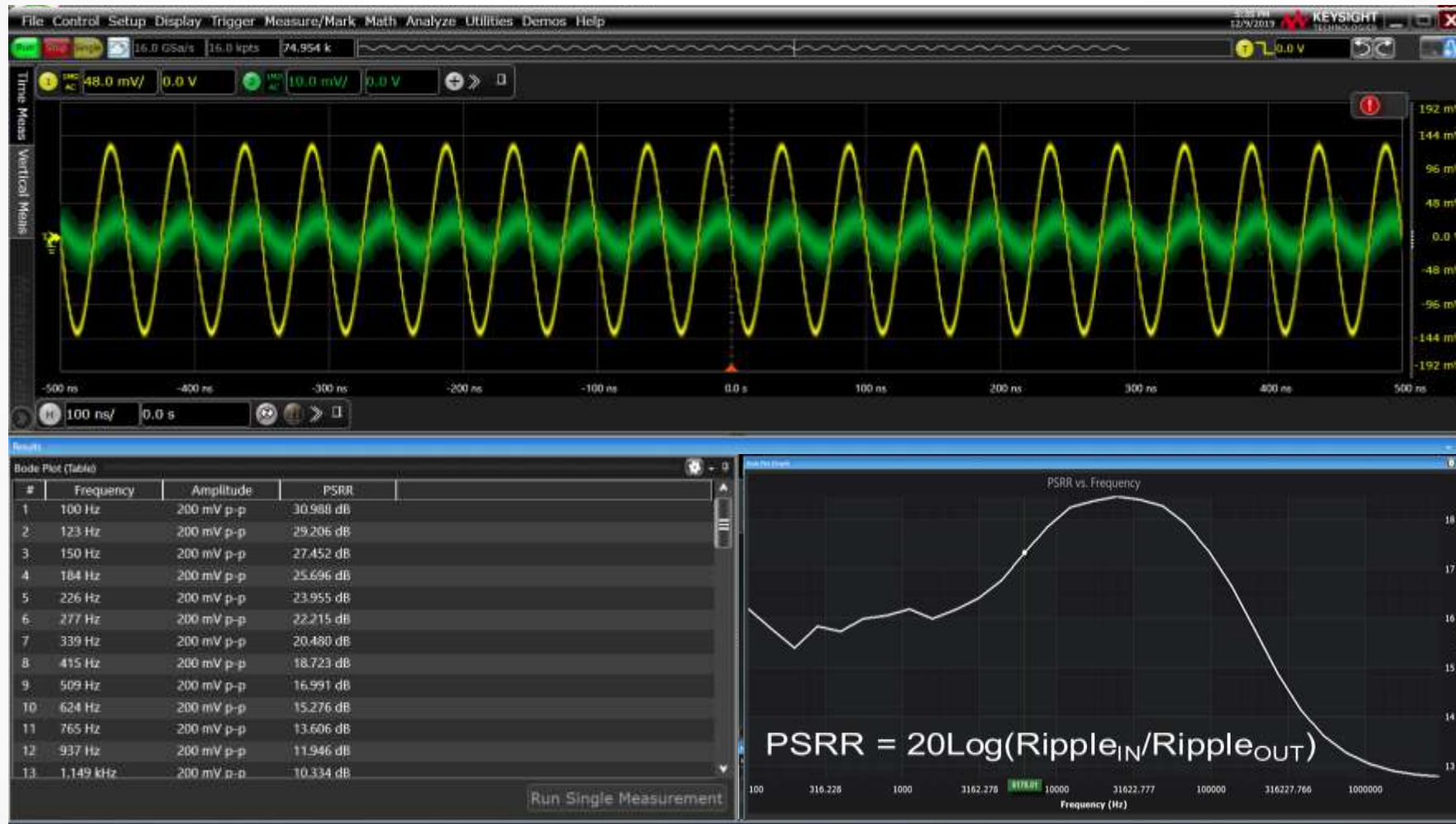


WaveGen



Power Integrity

POWER SUPPLY REJECTION RATIO--PSRR



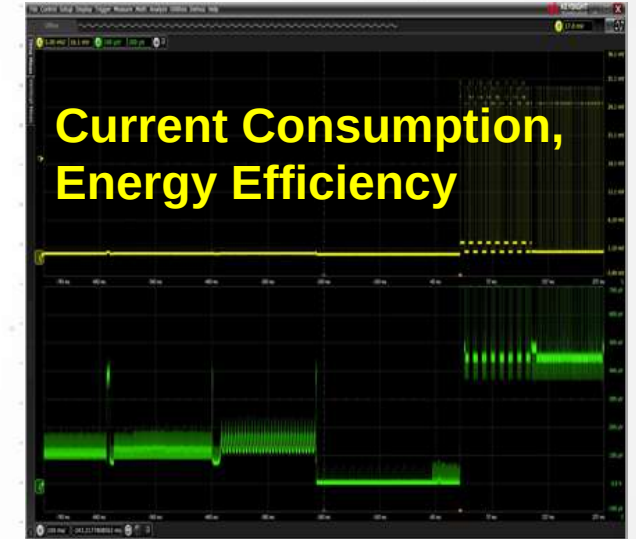
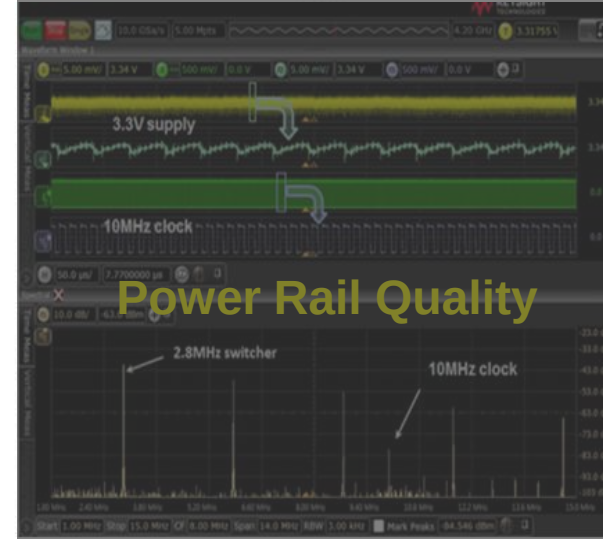
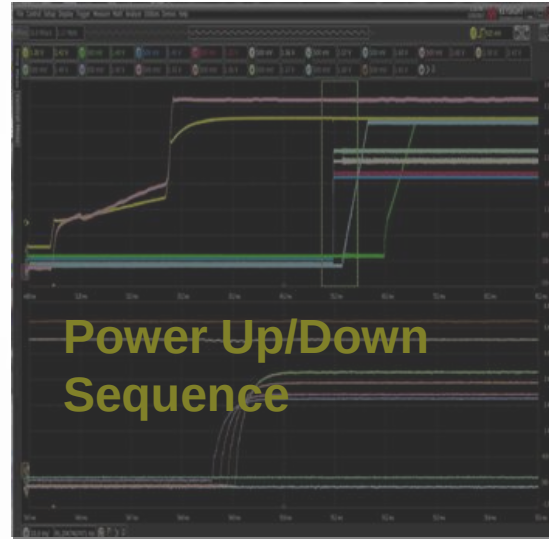
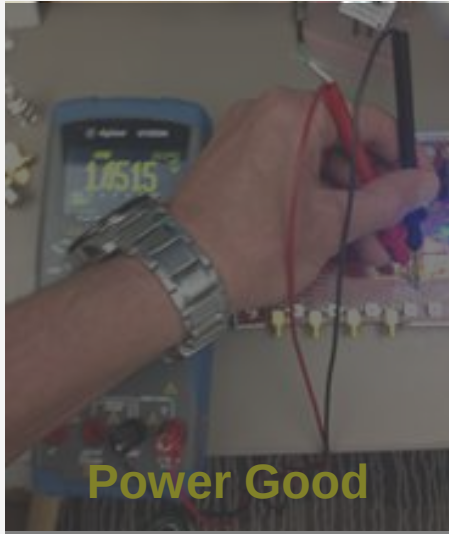
Power Integrity

CONTROL LOOP RESPONSE (BODE)



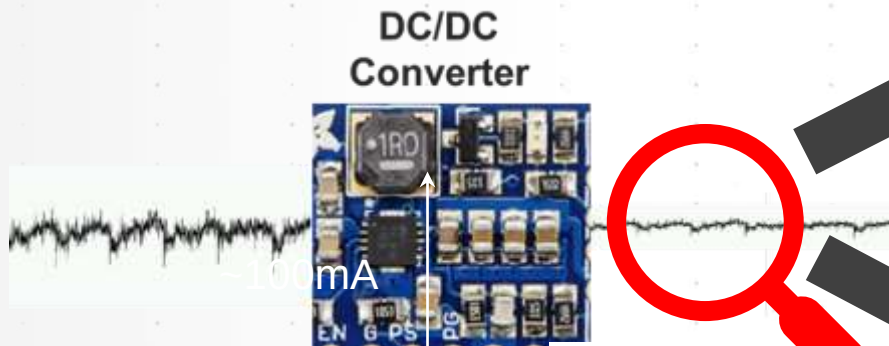
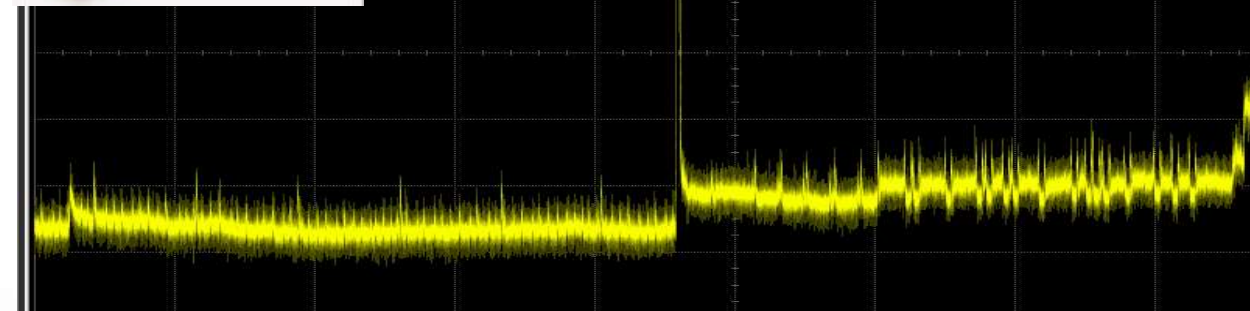
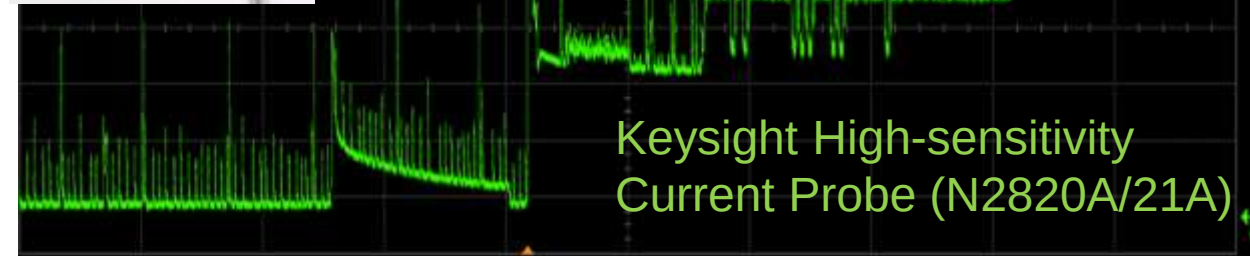
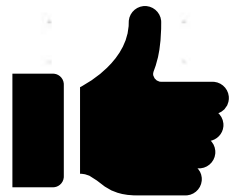
Power Integrity (PI)

TYPICAL TEST FLOW



Power Integrity (PI)

CURRENT CONSUMPTION, ENERGY EFFICIENCY



Power Integrity

HIGH-SENSITIVITY CURRENT PROBES

- N2820A-Series Current Probes
 - High Sensitivity
 - High Dynamic Range
 - R_{SENSE} : 1m Ω to 1M Ω



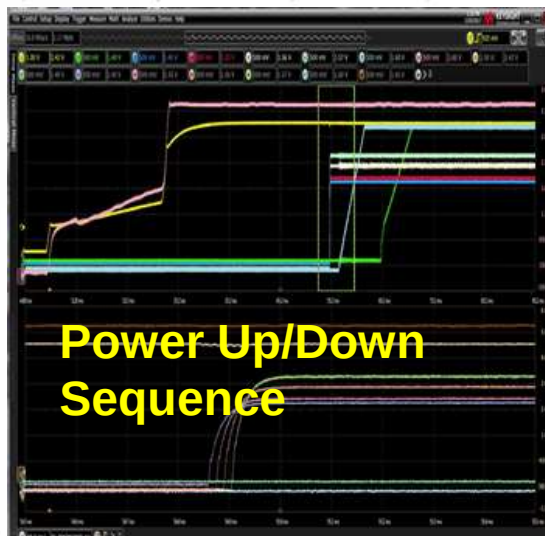
Power Integrity (PI)

SUMMARY



MXR With:

- Built-in Digital Volt Meter (standard feature).



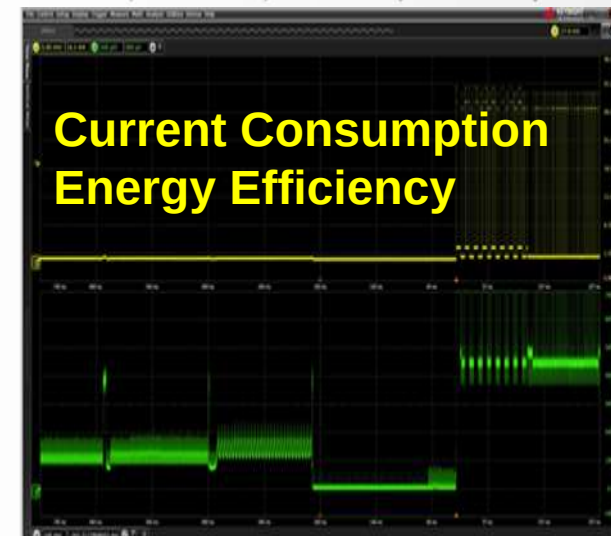
MXR With:

- Simultaneous mask testing on every channel and automatic mask generation (standard feature)



MXR With:

- 2Ghz & 6GHz Power Rail Probes (N7020A, N7024A)
- PI App--D9010POWA
- Power App-D9010PWRA
 - PSRR, etc.



MXR with:

- High-sensitivity current probes (N2820A, N2821A)



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