KEYSIGHT WORLD 2020

# Testing Next-Gen Type-C Technologies of USB4, Thunderbolt 4, and DP 2.0

*Jacky Yu*

*Project Manager / Keysight Technologies*

# Agenda

Preparing to test and avoid pitfalls in your USB4 implementations

- USB4/DPoC Overview
- USB4/DPoC Compliance Testing Overview
- USB4/DP Electrical Testing
- Q & A

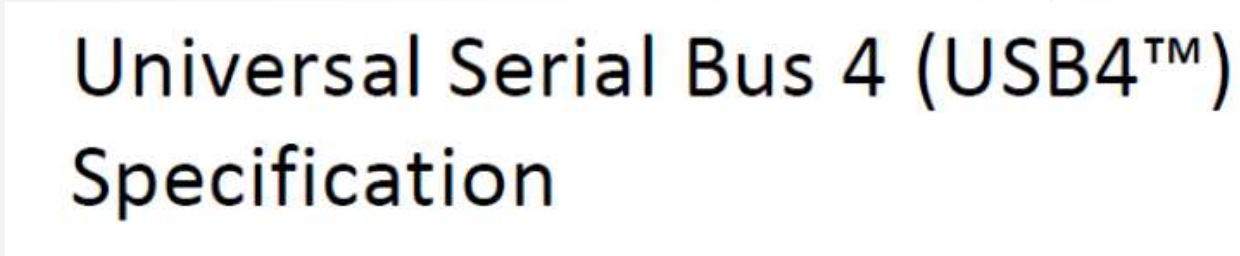
Note：

- USB4™, USB Type-C™ and USB-C™ are trademarks of USB Implementers Forum
- Thunderbolt™ is a trademark of Intel Corporation
- VESA® is a registered trademark and DisplayPort™ is a trademark of VESA
- USB4 diagrams courtesy of the USB-IF

# USB4/DPoC Overview

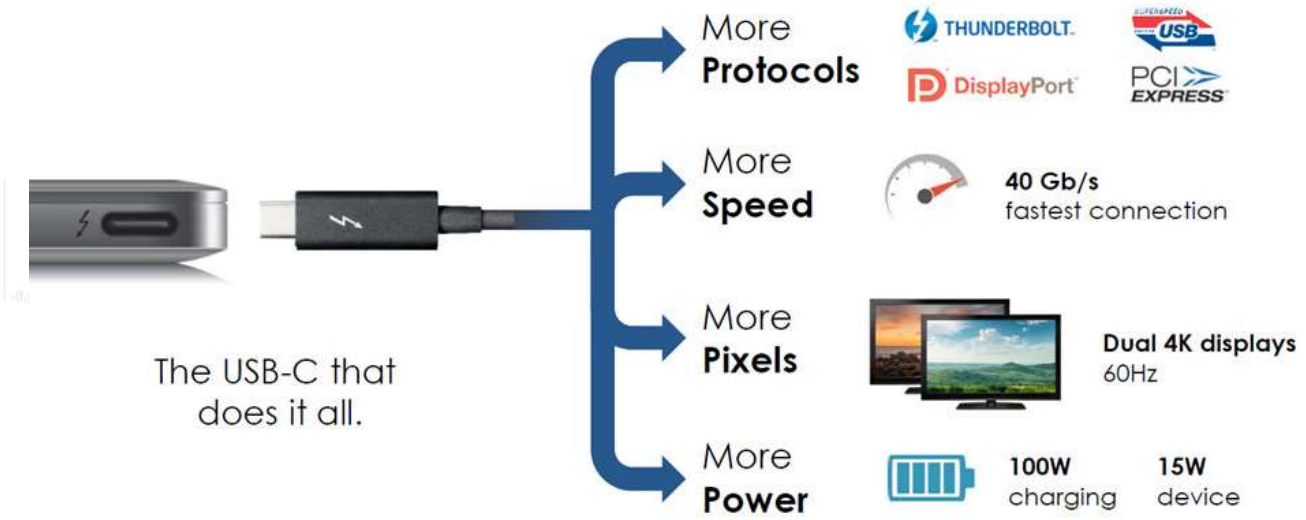
# USB4 Overview

- Announced by USB-IF in March 2019
- Spec released September 2019
- Based on the Thunderbolt 3 protocol
- Open standard and potentially integrated in CPU
- Uses the Type-C connector
- Tunnels USB, DP, and PCIe
- Channel aggregation: two independent 20Gbps bonded into one logical 40Gbps link
- Supports other standards through ALT mode
- Keysight solution help test with early adopter Protocol Decode, TX, RX, and Return Loss



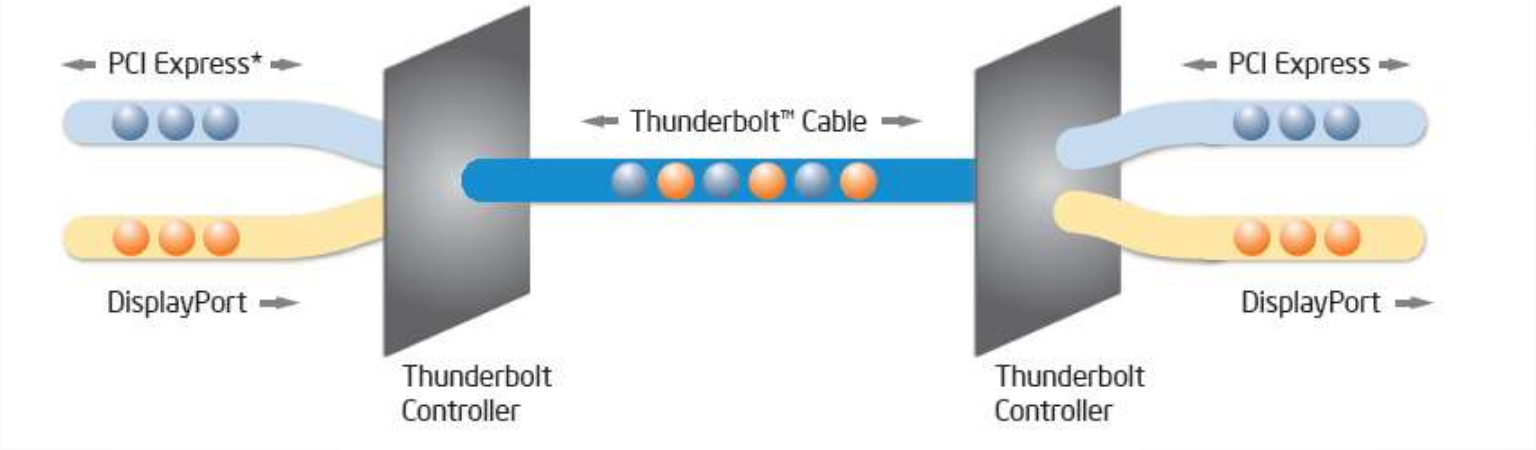
# Thunderbolt 3 Overview

- Announced in Q2 2015
- Uses the Type-C connector
- Channel aggregation: two independent 20Gbps links into one logical 40Gbps link
- Supports other standards through ALT mode
- Cost competitive vs multi-chip, discrete, mux solutions



# Thunderbolt and CIO (Converged IO)

- Thunderbolt features two bidirectional (full duplex) channels that run up to 20Gbps each and allows daisy-chaining of up to six devices.
- Passive or active Cable
- Thunderbolt tunnels two protocols (PCI Express and DisplayPort) when running in native Thunderbolt mode.



# TBT4 Overview

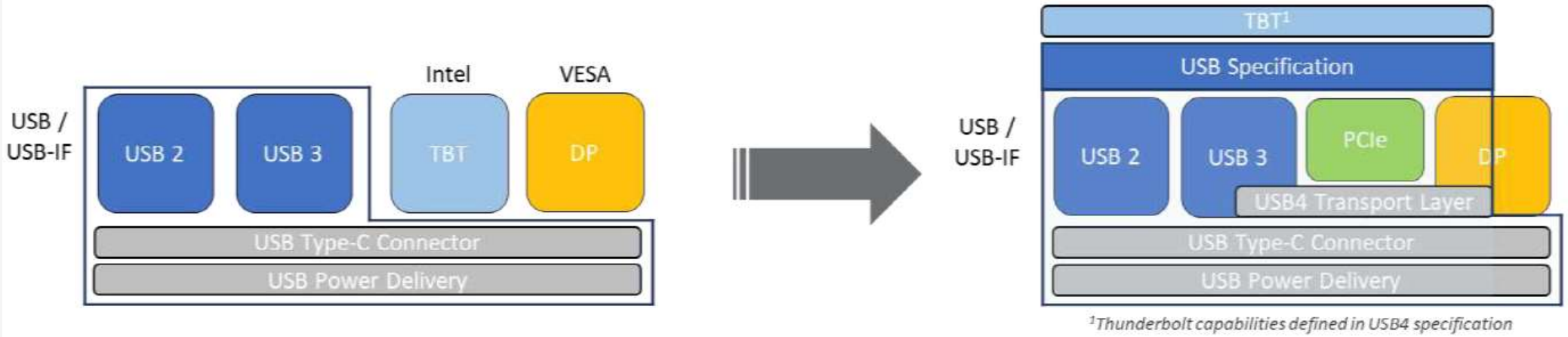
- To better align with USB4, Intel launch TBT4 in latest platform but provide same physical layer as TBT3.
- USB4 specification defines how to build TBT3 compatible products.
- Thunderbolt certification, brand names and logos are managed and owned by Intel without change.

# USB Revision Overview

| Revision | Brand Name | Throughput | Package Logo |
|---|---|---|---|
| USB1.1 | Low Speed<br>Full Speed | 1.5Mbps<br>12Mbps |  |
| USB2.0 | High Speed | 480Mbps |  |
| USB3.0<br>USB3.2 Gen 1x1 | SuperSpeed USB<br>5Gbps | 5Gbps |  |
| USB3.1<br>USB3.2 Gen 2x1 | SuperSpeed USB<br>10Gbps | 10Gbps |  |
| USB3.2<br>USB3.2 Gen 2x2 | SuperSpeed USB<br>20Gbps | 20Gbps |  |
| USB4<br>USB4 Gen 2x2 | USB4 20Gbps | 20Gbps |  |
| USB4<br>USB4 Gen 3x2 | USB4 40Gbps | 40Gbps |  |

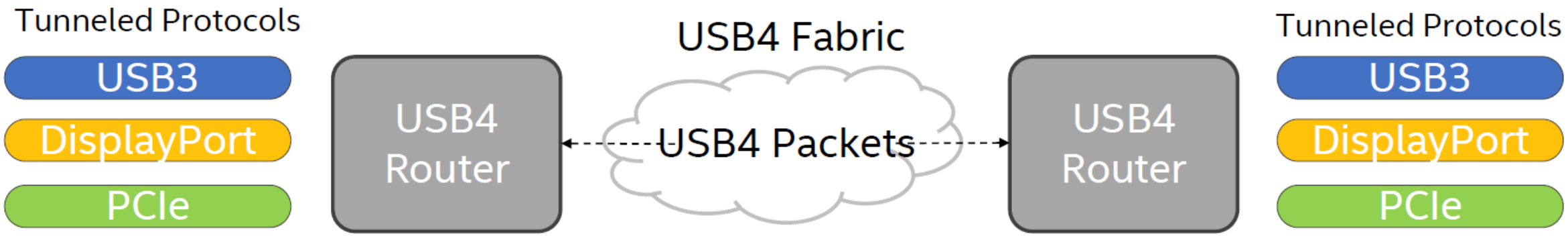
# Delivering the USB Type-C Vision

- USB4™ Specification Goals:
  - Help converge USB Type-C connector ecosystem to minimize end-user confusion
  - Drive broad adoption of USB4 architecture
- What the Specification Enables:
  - Standards-based ownership for specifications and certification
  - Third party vendors can build Thunderbolt™ 3 compatible SOC or peripheral silicon



# USB4™ Architecture Overview

- Runs over USB Type-C® interconnect
- Tunnels USB3, PCIe and DP protocols
- Signaling rates of 10 or 20 Gbps (10 to 40Gbps aggregated b/w)
- Utilizes passive and active cables (longer reach)
- Topologies with up to 6 routers
- Time sync accuracy support across USB4™ Fabric



# What is DisplayPort?

- Digital display interface from GPU to display
  - Addresses embedded models as well
- Administered by VESA[1]
- Up to 4 differential lanes
- Daisy chain up to 32 monitors
- Connectors
  - Standard DP
  - Mini DP
  - USB Type-C®

DPoC(Alt mode)

[1]Video Electronics Standards Association

# DisplayPort Interface

## Main Link

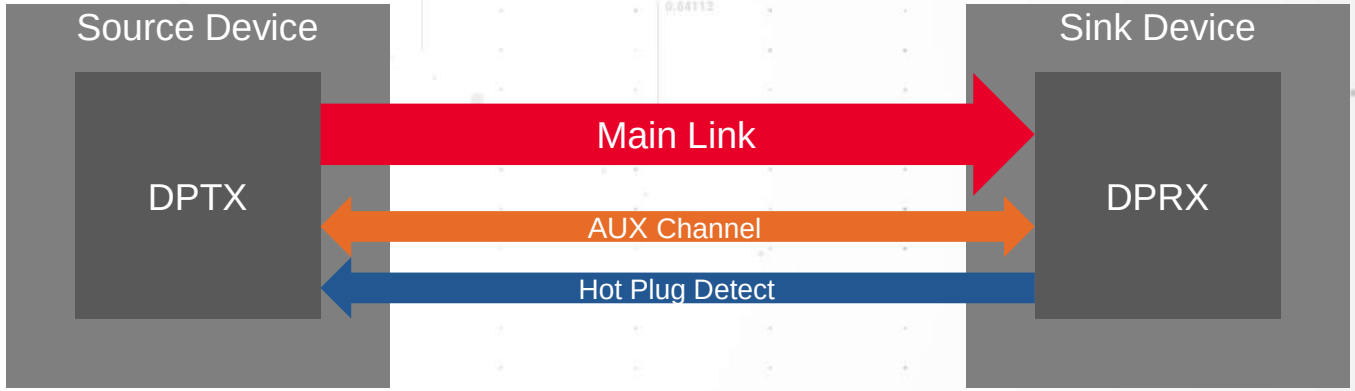
- Display data transfer
- 4 unidirectional high-speed lanes
- Multiple bitrates supported

## AUX Channel

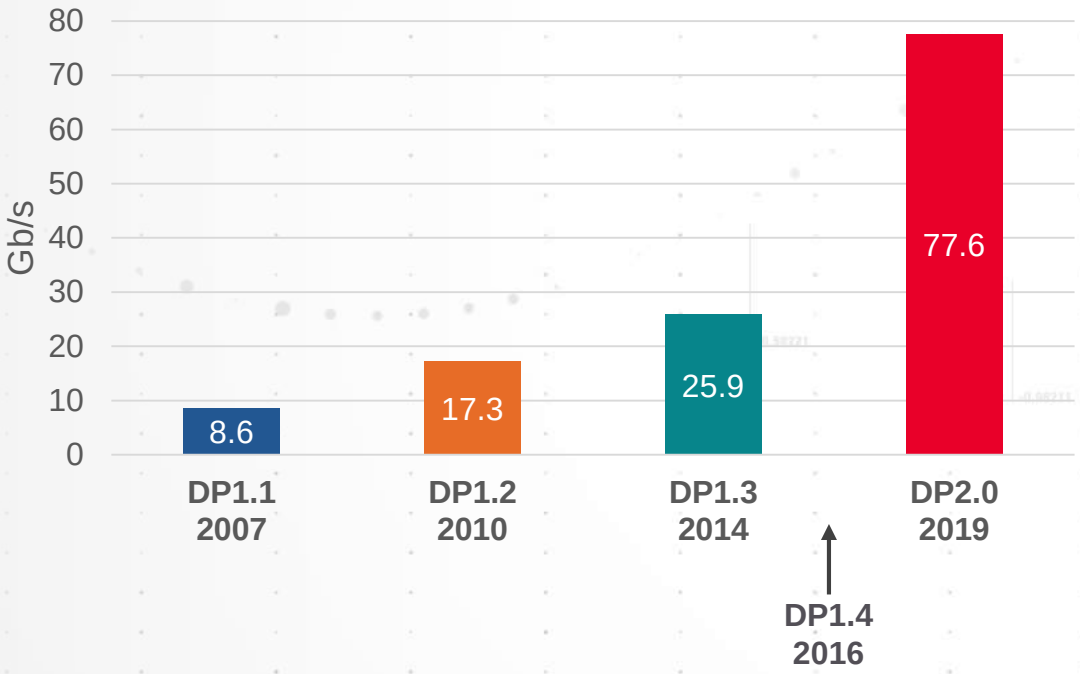
- Link management
- Test mode control
- 1 bidirectional low-speed lane

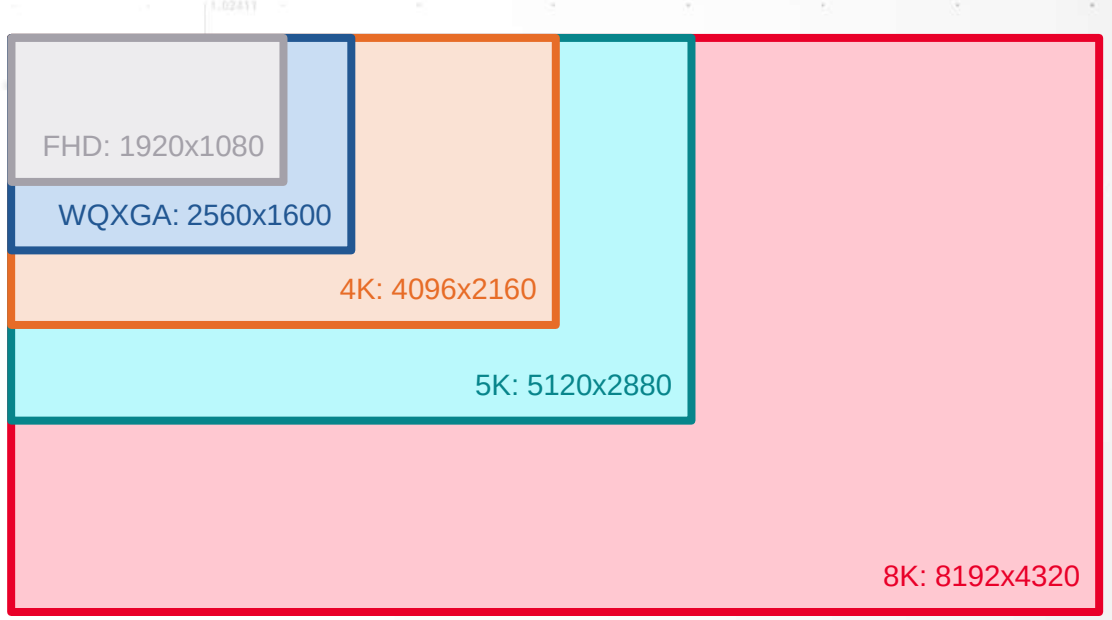
## Hot Plug Detect

- Source detects presence of sink
- Sink notifies of status changes via IRQ



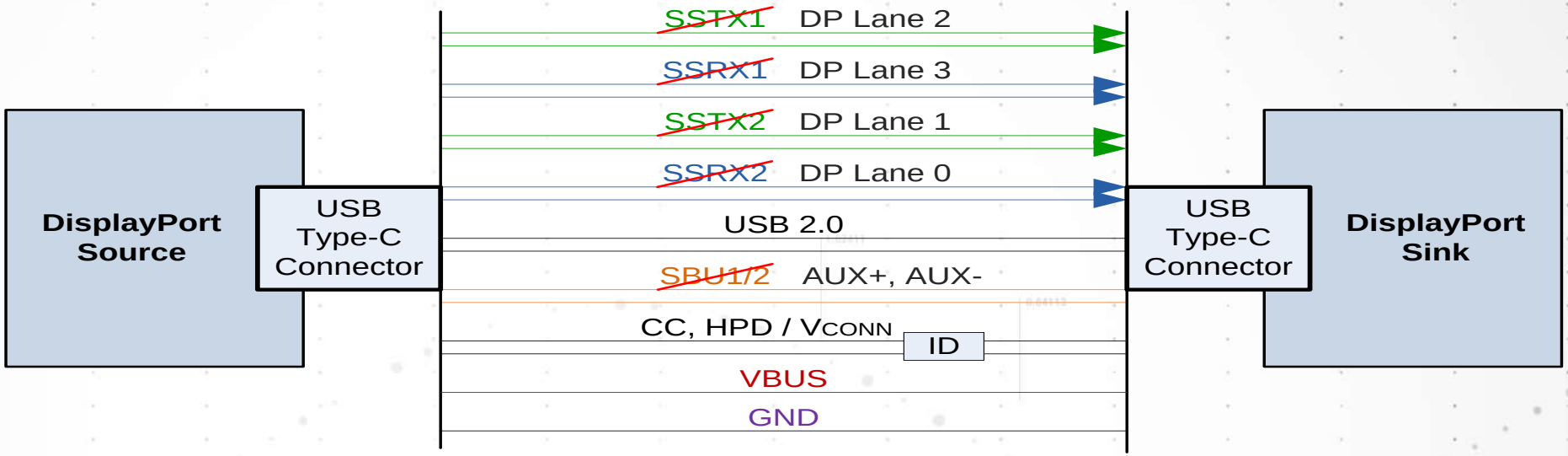
# DP Maximum Data Transfer Rate and Resolution[1]




[1]Color depth = 24 bpp, refresh rate = 60 Hz

# 4xDP Over a USB Type-C to USB Type-C Full Feature Passive Cable




- Utilizes optional DP Alt Mode capability of USB Type-C connector
- DisplayPort can use all four high speed lanes to deliver full DisplayPort performance
- The DisplayPort AUX Channel uses the SBU pins
- The DisplayPort HPD / IRQ is transmitted over the CC pin using the USB-PC protocol
- USB 2.0 and USB Power Delivery always available

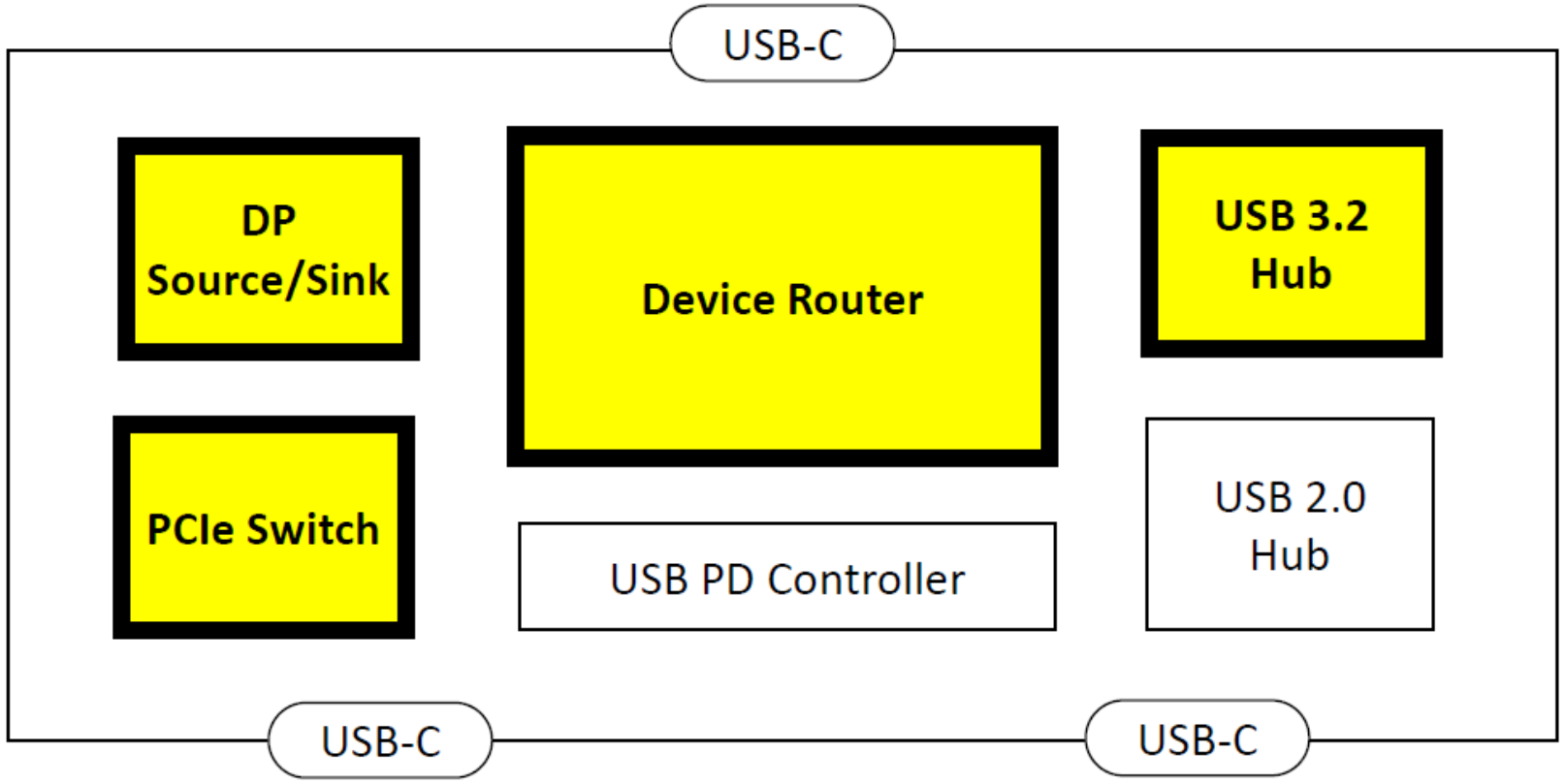
# USB4/DPoC Compliance Testing Overview

# USB4™ Certification Categories

| | CERTIFIED USB 20 Gbps | CERTIFIED USB 40 Gbps |
|---|---|---|
| USB4 Host | ✓ | ✓ |
| USB4 Hub | Not Allowed | ✓ |
| USB4-Based Dock | Not Allowed | ✓ |
| USB4 Peripheral Device | ✓ | ✓ |
| USB4 Active Cable | ✓ | ✓ |
| USB4 Passive Cable | ✓ | ✓ |

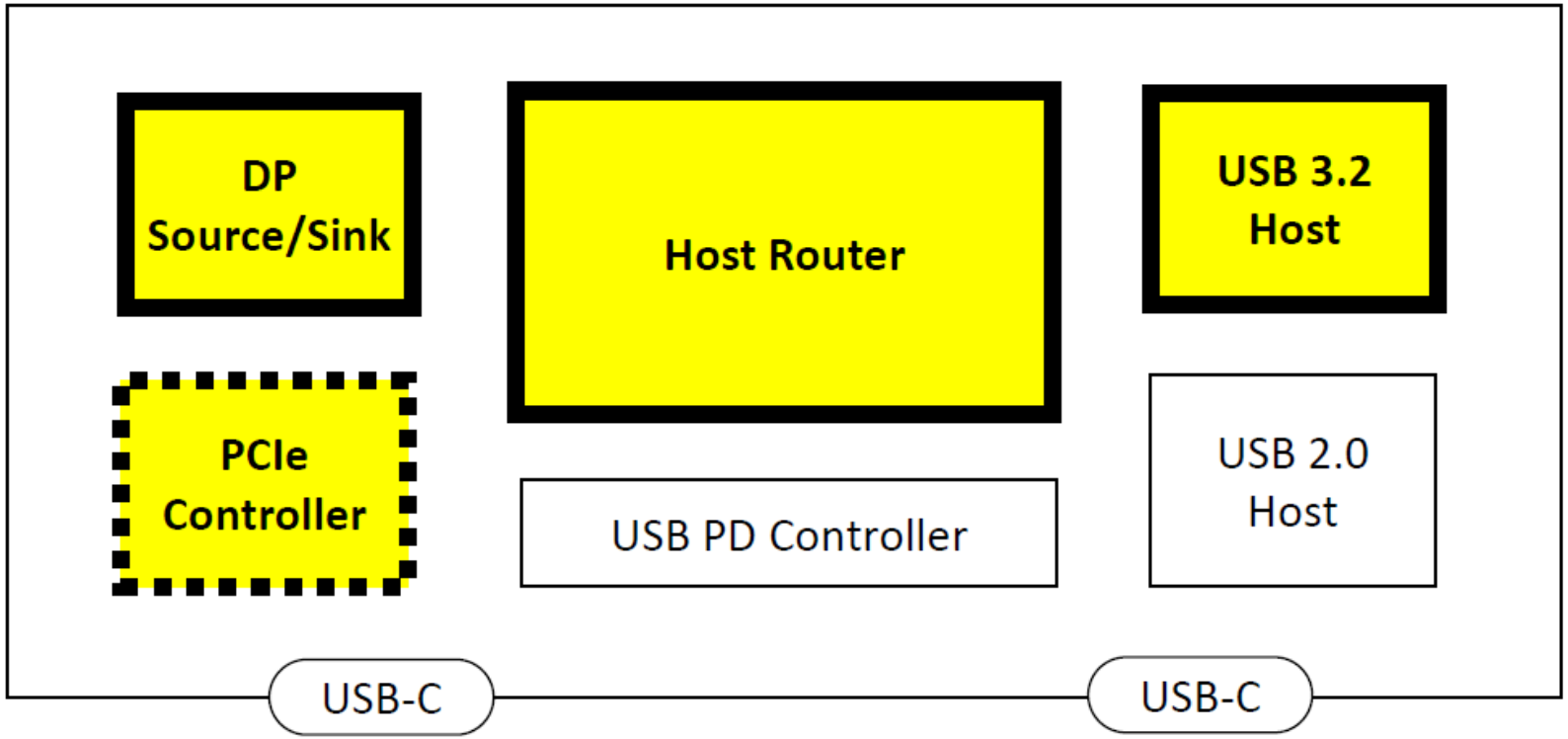
# USB4™ Required Testing – Hubs/Docks

- USB PD Compliance
- USB Type-C® Compliance
- USB 2.0 Compliance
- USB 3.2 Compliance
- **USB4™ Compliance**
  - **Tunneling**
  - **TBT3-Compatibility**



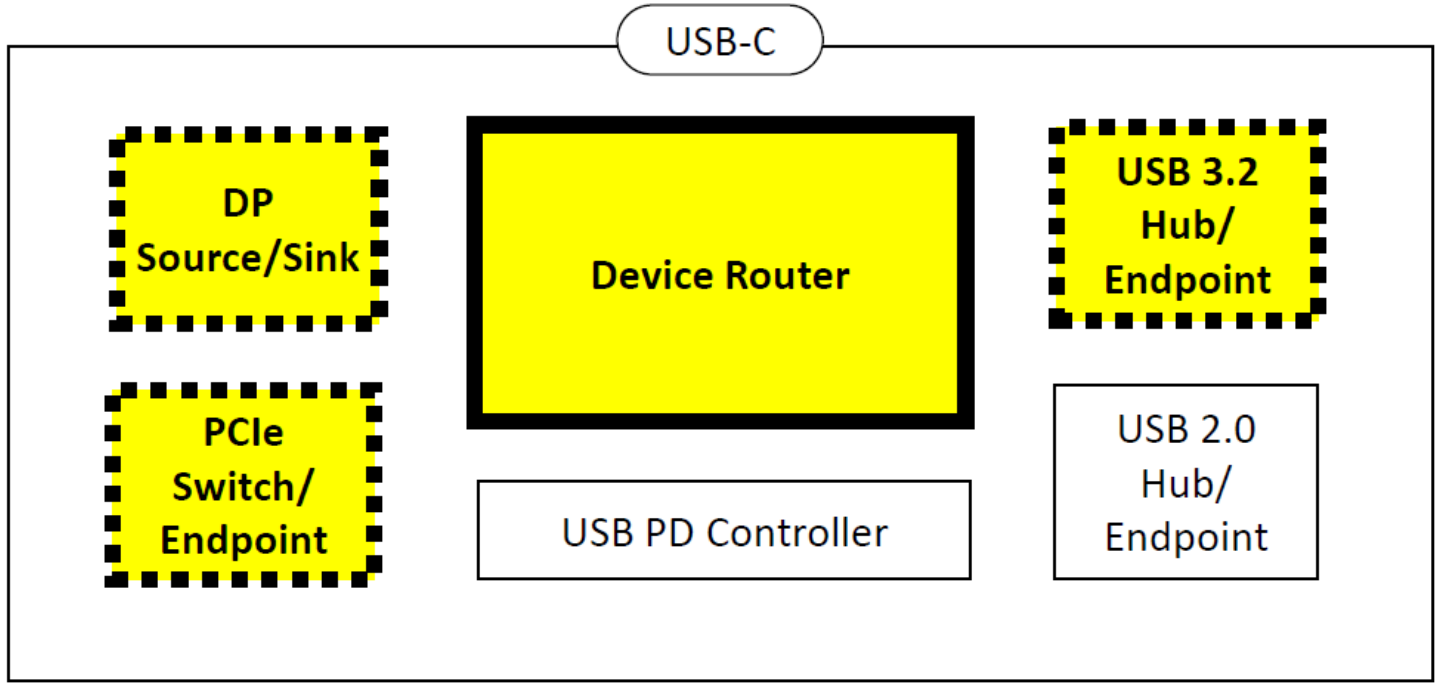
# USB4™ Required Testing – Hosts

- USB PD Compliance
- USB Type-C® Compliance
- USB 2.0 Compliance
- USB 3.2 Compliance
- **USB4™ Compliance**
  - **DP and USB3 Tunneling**
  - **If supported:**
    - **PCIe Tunneling**
    - **TBT3-Compatibility**



# USB4™ Required Testing – Peripheral Devices

- USB PD Compliance
- USB Type-C® Compliance
- USB 2.0 Compliance
- **USB 3.2 Compliance**
  - **If supported**
- **USB4™ Compliance**
  - **If supported:**
    - **DP Tunneling**
    - **USB3 Tunneling**
    - **PCIe Tunneling**
    - **TBT3-Compatibility**




**If support DP or PCIe tunneling, must support equivalent USB function (if available)**

# DP Compliance Program

- Managed by VESA
  - Jim Choate (former Agilent USB Pyramid Lead)
- Why do companies need the logo?
  - Ensure interoperability
  - Consumers can easily identify compliant products
- How to get it?
  - Pass the Compliance Program
  - Be a member of VESA
  - Sign the VESA DisplayPort Trademark License Agreement
- Authorized Test Centers (ATCs)
  - Allion, GRL, TTA, UL

# DP Compliance Test Specification

- **DP1.4a PHY CTS rev1.0** released in July 2018
  - Ongoing activities to release new revision (2.0 coming soon)
- Several DUT types
  - **Source (un)tethered**
  - **Sink (un)tethered**
  - Passive cables
  - Others…

| Item | Name | Normative/ Informative |
|---|---|---|
| 3.1 | Eye Diagram Test | Normative |
| 3.2 | HBR/RBR Non-PE Level Verification Test | Normative |
| 3.3 | HBR/RBR PE Level Verification and Maximum Differential Peak-to-Peak Voltage Test | Normative |
| 3.4 | HBR3/HBR2 PE Level and Equalization Verification Test | Normative |
| 3.5 | HBR3/HBR2 $V_{TX\_DIFFp\text{-}p\_MAX}$ Test | Normative |
| 3.6 | Inter-pair Skew Test | Informative |
| 3.7 | Intra-pair Skew Test | Informative |
| 3.8 | AC Common Mode Noise Test | Informative |
| 3.9 | Non-ISI Jitter Measurement Test | Normative |
| 3.10 | HBR3 TX Differential RL Test | Informative |
| 3.11 | TJ/RJ/DJ Measurement Tests | Normative |
| 3.12 | Main-Link Frequency Compliance Test | Normative |
| 3.13 | Spread-spectrum Modulation Frequency Test | Normative |
| 3.14 | Spread-spectrum Modulation Deviation Test | Normative |
| 3.15 | dF/dT Spread-spectrum Deviation High-frequency Variation Test | Informative |

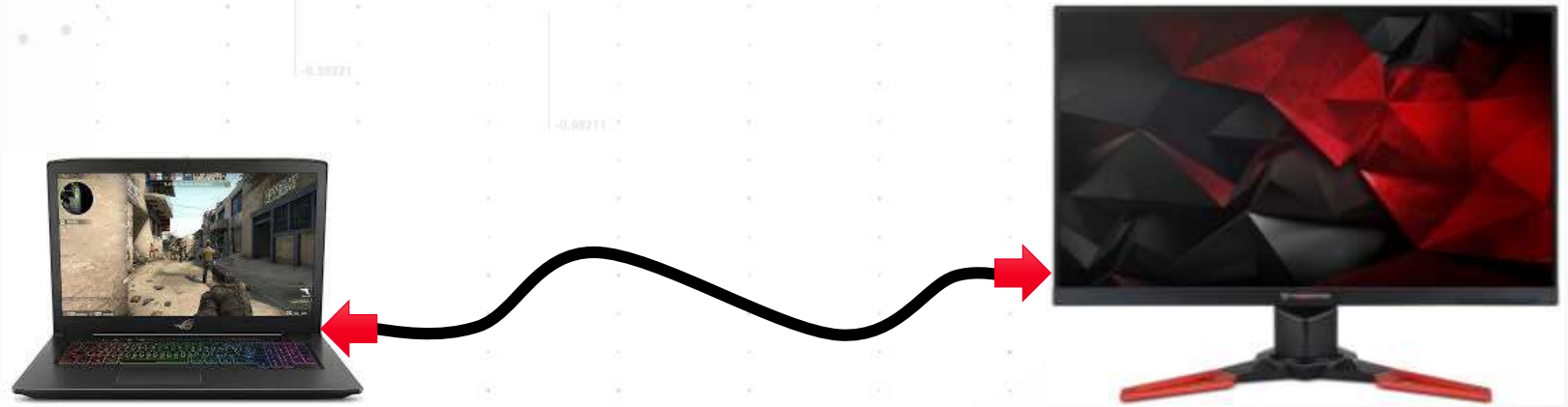
| Item | Name | Normative/ Informative |
|---|---|---|
| 4.1 | JTOL Test | Normative |

# DP Alt Mode Compliance Test Specification

The DP Alt Mode on USB Type C CTS Version 1.0, was released Jan 24, 2017.

Over 200 DP Alt Mode products have been certified over last two years

- Products include Sources, Sinks, Adapters and Docks



# DP Alt mode Certification Test Coverage

Test plan and CTS covers all features and supported pin assignments.

- USB PD Compliance Testing
  - Demonstration of proper functionality/behavior for DP Alt Modes
  - A device must pass DP Alt Mode USB-PD certification tests to receive DP certification
- TX and RX Electrical testing of all supported modes with PHY test fixtures
  - USB PHY electricals
    a. USB 3.2 5G
    b. USB 3.2 10G (if supported)
    c. USB 2.0 480Mb/s
- DP PHY electricals (DP 1.4a PHY CTS)
  - RBR, HBR, HBR2, HBR3
  - Aux Channel

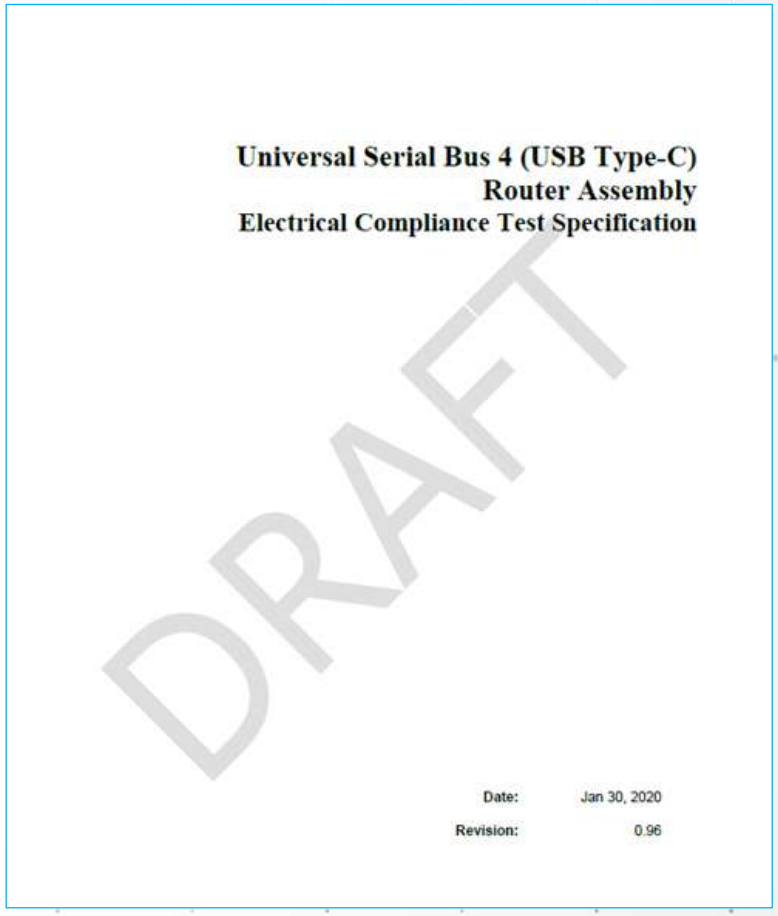
# USB4/DP Electrical Testing

# USB4 Electrical Testing Methodology

- PHY testing approach will be similar to Thunderbolt 3
  - Tx, Rx, and Return Loss
  - Active and Passive Cable Test

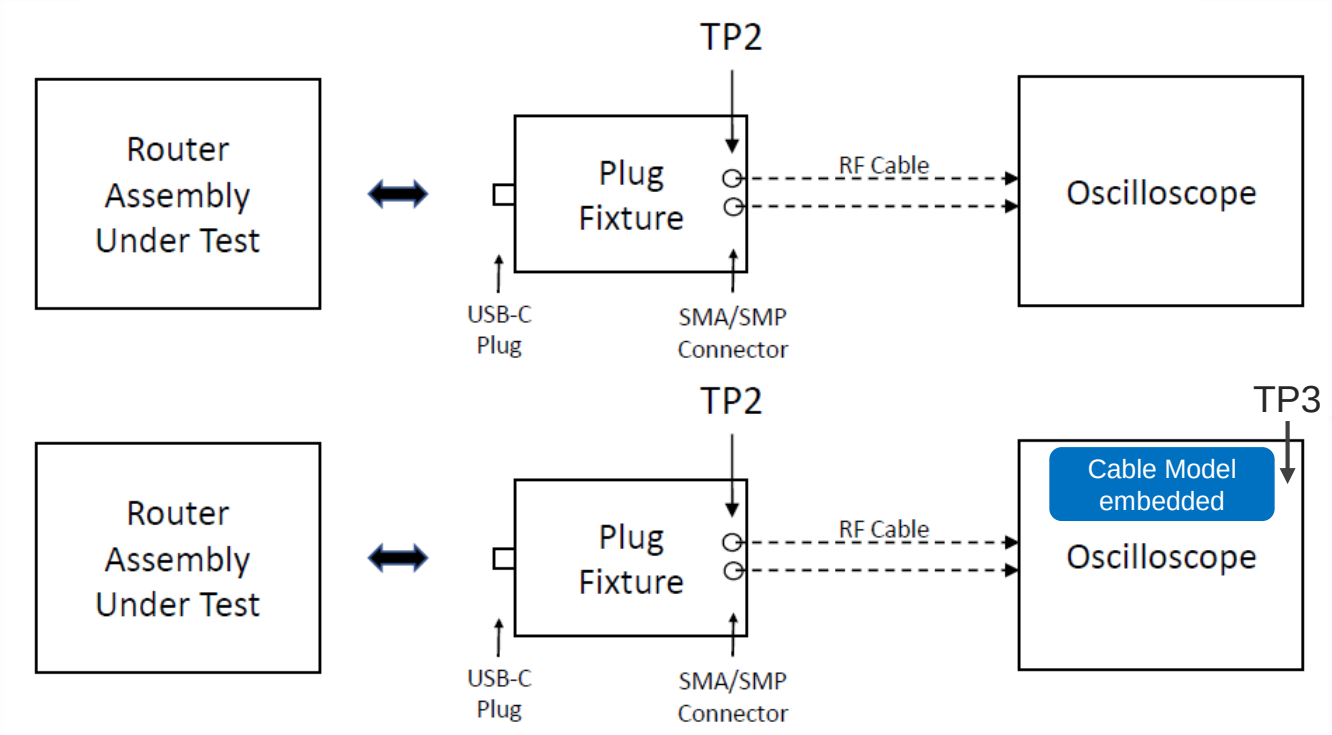
  Plus
  - Type-C Power Delivery
  - DP, USB over Type-C

**Universal Serial Bus 4 (USB Type-C)**
**Electrical Compliance Test Specification**



# Transmitter Measurement Point/Setup

- TP2 measurements are done using plug-fixture
- TP3 measurements are done using plug-fixture with cable model embedded in the oscilloscope



# Transmitter Specifications

- Traditional voltage, eye, SSC, 10ps min rise/fall time
- Traditional UI, TJ, DDJ jitter decomposition
- Challenge: New Uncorrelated jitter measurements

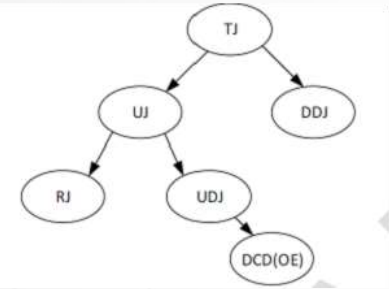
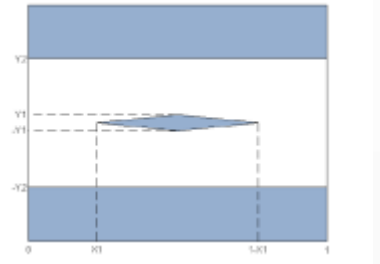



Table 3-3. Transmitter Specifications Applied for All Speeds (at TP2)

| Symbol | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| RL_DIFF | Differential Return Loss, 0.05-12GHz | -- | See Section 3.4.1.2 | dB | |
| RL_COMM | Common Mode Return Loss, 0.05 - 12GHz | -- | See Section 3.4.1.3 | dB | |
| TX_EQ | Transmitter Equalization Setting | -- | See Section 3.4.1.4 | | |
| SSC_DOWN_SPREAD_RANGE | Dynamic range of SSC down-spreading during steady-state | 0.4 | 0.5 | % | See Note 3, Note 4, and Figure 3-9. |
| SSC_DOWN_SPREAD_RATE | SSC down-spreading modulation rate during steady-state | 30 | 33 | KHz | See Note 4 and Figure 3-9. |
| SSC_PHASE_DEVIATION | Phase jitter associated with the SSC modulation during steady-state | 2.5 | 22 | ns pp | See Note 1, Note 4, and Figure 3-9. |
| SSC_SLEW_RATE | SSC frequency slew rate (df/dt) during steady-state | -- | 1250 | ppm/µs | See Note 2, Note 4, and Figure 3-9. |
| TX_FREQ_VARIATIONS_TRAINING | TX frequency variation during Link training, before obtaining steady-state | -- | See Section 3.4.1.1 | ppm | See Note 4. |
| LANE_TO_LANE_SKEW | Skew between dual transmit signals of the same USB4 Port | -- | 26 | ns | See Note 5. |
| RISE_FALL_TIME | TX rise/fall time measured between 20-80% levels | 10 | -- | ps | Test pattern shall be SQ128 (see Table 6-56). |
| V_ELEC_IDLE | Peak voltage during transmit electrical idle (one-sided voltage opening of the differential signal) | -- | 20 | mV | See Note 6. |
| V_TX_DC_AC_CONN | Instantaneous DC+AC voltages at the connector side of the AC coupling capacitors | -0.5 (min1) -0.3 (min2) | 1.8 | V | See Note 7. |

Table 3-6. Gen 2 Transmitter Specifications at TP2

| Symbol | Description | Min | Max | Units | Comments |
|---|---|---|---|---|---|
| UI | Minimum Unit Interval | 99.97 | 100.03 | ps | The minimum UI value corresponds to the Link baseline speed of 10.0 Gbps with an uncertainty range of -300 ppm to 300 ppm. See Note 4. |
| AC_CM | TX AC Common Mode voltage | -- | 100 | mV pp | |
| TJ | Total Jitter | -- | 0.38 | UI pp | See Note 2 and Note 3. |
| UJ | Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ) | -- | 0.31 | UI pp | See Note 2. |
| DDJ | Data-Dependent Jitter | -- | 0.15 | UI pp | See Note 5. |
| UDJ | Deterministic jitter that is uncorrelated to the transmitted data | -- | 0.17 | UI pp | |
| UDJ_LF | Low Frequency Uncorrelated Deterministic Jitter | -- | 0.04 | UI pp | See Note 6. |
| DCD | Even-odd jitter associated with Duty-Cycle-Distortion | -- | 0.03 | UI pp | |
| Y1 | TX eye inner height (one-sided voltage opening of the differential signal) | 140 | -- | mV | Measured for 1E6 UI. See Note 1, Note 2, and Figure 3-15. |
| Y2 | TX eye outer height (one-sided voltage opening of the differential signal) | -- | 650 | mV | Measured for 1E6 UI. See Note 1, Note 2, and Figure 3-15. |
| Notes: | | | | | |



# Return Loss

- TX and RX return loss
- Differential and Common Mode Return Loss
- Challenge: Jumping straight into TX and RX testing

E5080B New ENA Network Analyzer

Figure 3-10. TX Differential Return Loss Mask

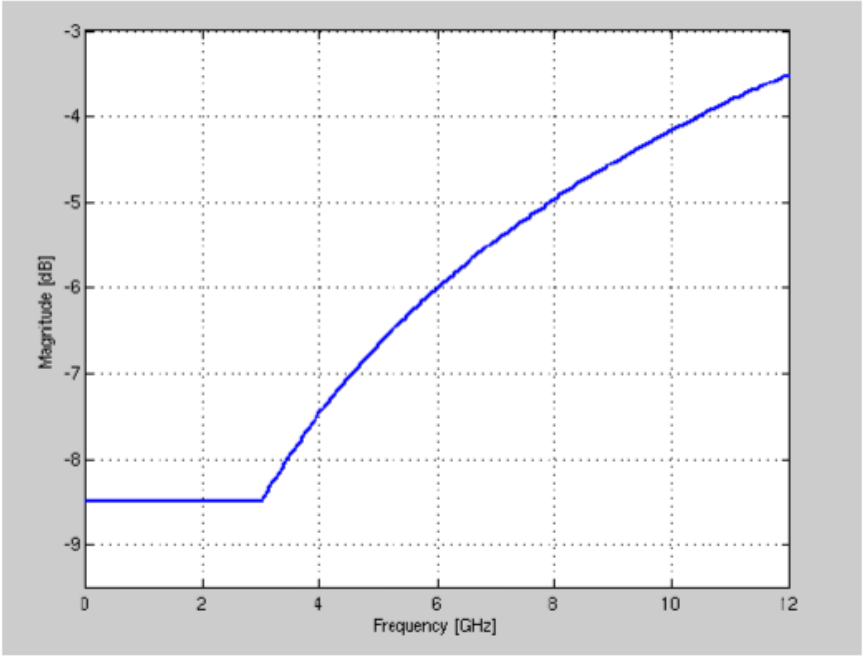
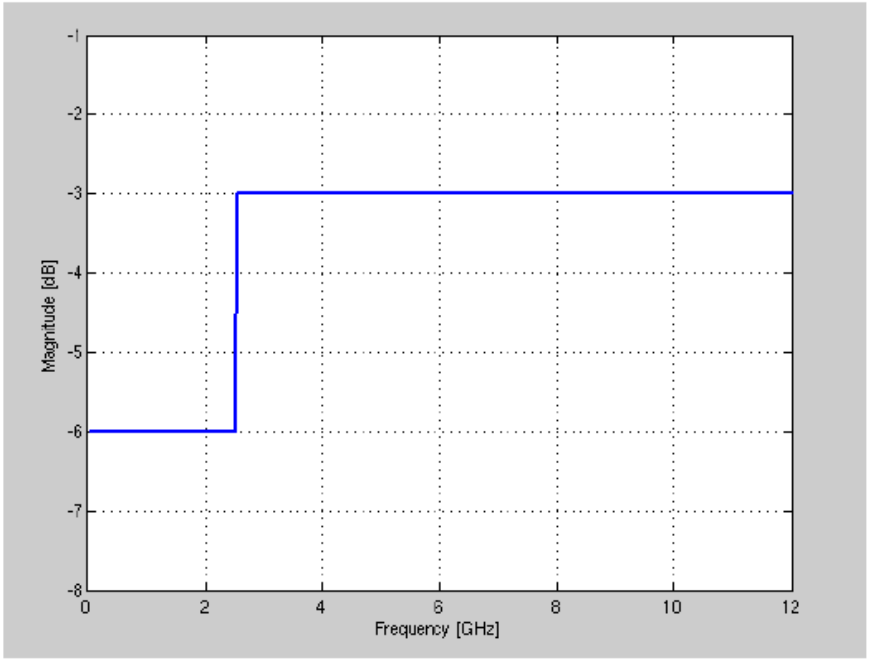



Figure 3-11. TX Common-Mode Return Loss Mask



# Transmitter Equalization

- Going from 1 pre-shoot and 1 de-emphasis to 16 presets, including a low-voltage variant
- Must test each preset, and also find optimal preset
- Challenge: Over-look optimization, or set incorrectly in TX silicon.

**Table 3-5. Transmit Equalization Presets**

| Preset Number | Pre-shoot [dB] | De-emphasis [dB] | Informative Filter Coefficients | | |
|---|---|---|---|---|---|
| | | | $C_{-1}$ | $C_0$ | $C_1$ |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | −1.9 | 0 | 0.90 | −0.10 |
| 2 | 0 | −3.6 | 0 | 0.83 | −0.17 |
| 3 | 0 | −5.0 | 0 | 0.78 | −0.22 |
| 4 | 0 | −8.4 | 0 | 0.69 | −0.31 |
| 5 | 0.9 | 0 | −0.05 | 0.95 | 0 |
| 6 | 1.1 | −1.9 | −0.05 | 0.86 | −0.09 |
| 7 | 1.4 | −3.8 | −0.05 | 0.79 | −0.16 |
| 8 | 1.7 | −5.8 | −0.05 | 0.73 | −0.22 |
| 9 | 2.1 | −8.0 | −0.05 | 0.68 | −0.27 |
| 10 | 1.7 | 0 | −0.09 | 0.91 | 0 |
| 11 | 2.2 | −2.2 | −0.09 | 0.82 | −0.09 |
| 12 | 2.5 | −3.6 | −0.09 | 0.77 | −0.14 |
| 13 | 3.4 | −6.7 | −0.09 | 0.69 | −0.22 |
| 14 | 3.8 | −3.8 | −0.13 | 0.74 | −0.13 |
| 15 | 1.7 | −1.7 | −0.05 | 0.55 | −0.05 |

# Transmitter Specifications at TP3

- Use case for 0.8m or 2m cable
- Challenge: Can be most difficult test case, coupled with no channel test case.

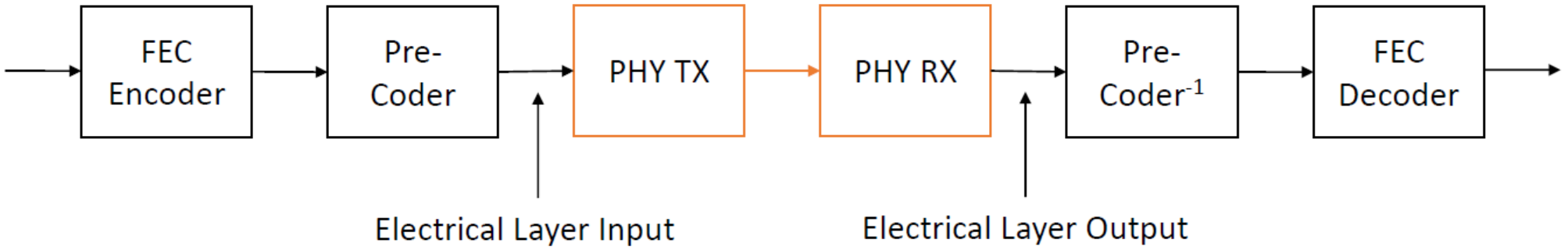
**Table 3-9. Gen 3 Transmitter Specifications at TP3**

| Symbol | Description | Min | Max | Units | Comments |
|---|---|---|---|---|---|
| TJ | Total Jitter | -- | 0.60 | UI pp | See Note 2, Note 3. |
| UJ | Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ) | -- | 0.31 | UI pp | Note 2. |
| UDJ | Deterministic jitter that is uncorrelated to the transmitted data | -- | 0.17 | UI pp | |
| X1 | TX eye horizontal deviation | -- | 0.23 | UI | Measured for 1E6 UI. See Note 2, Note 4, and Figure 3-15. |
| Y1 | TX eye inner height (one-sided voltage opening of the differential signal) | 49 | -- | mV | Measured for 1E6 UI. See Note 1, Note 2, and Figure 3-15. |
| Y2 | TX eye outer height (one-sided voltage opening of the differential signal) | -- | 650 | mV | Measured for 1E6 UI. See Note 1, Note 2, and Figure 3-15. |

Notes:

1. TX voltage is differential.
2. Measured while applying the reference CDR described in Section 3.3.3 and the reference equalizer defined in Section 3.3.4. Note that the measured jitter includes residual SSC jitter passing the reference CDR.
3. TJ is defined as the sum of all "deterministic" components plus 14.7 times the RJ RMS (the transmitter RJ RMS multiplier corresponds to the target BER with some margin on top).
4. X1 specification is informative but shall be assumed as a valid reference if direct TJ measurement cannot be reliably performed.

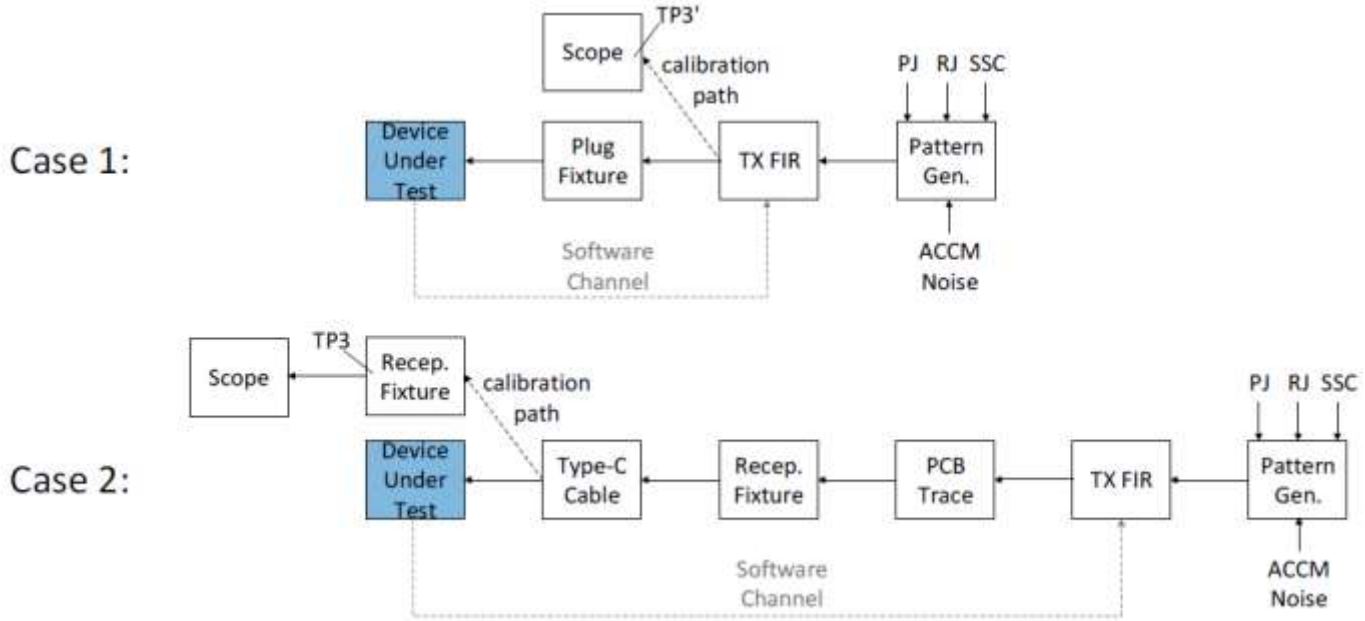
# USB4™ RX Testing Methodology




- The Electrical performance is tested in stand-alone mode without applying Pre-Coding nor Forward-Error-Correction
  - The testing is based on PRBS patterns driven by pattern-generator
- The coded BER performance cannot be measured directly due to the large measurement window needed (several years…) and therefore validated indirectly based on electrical layer indicators

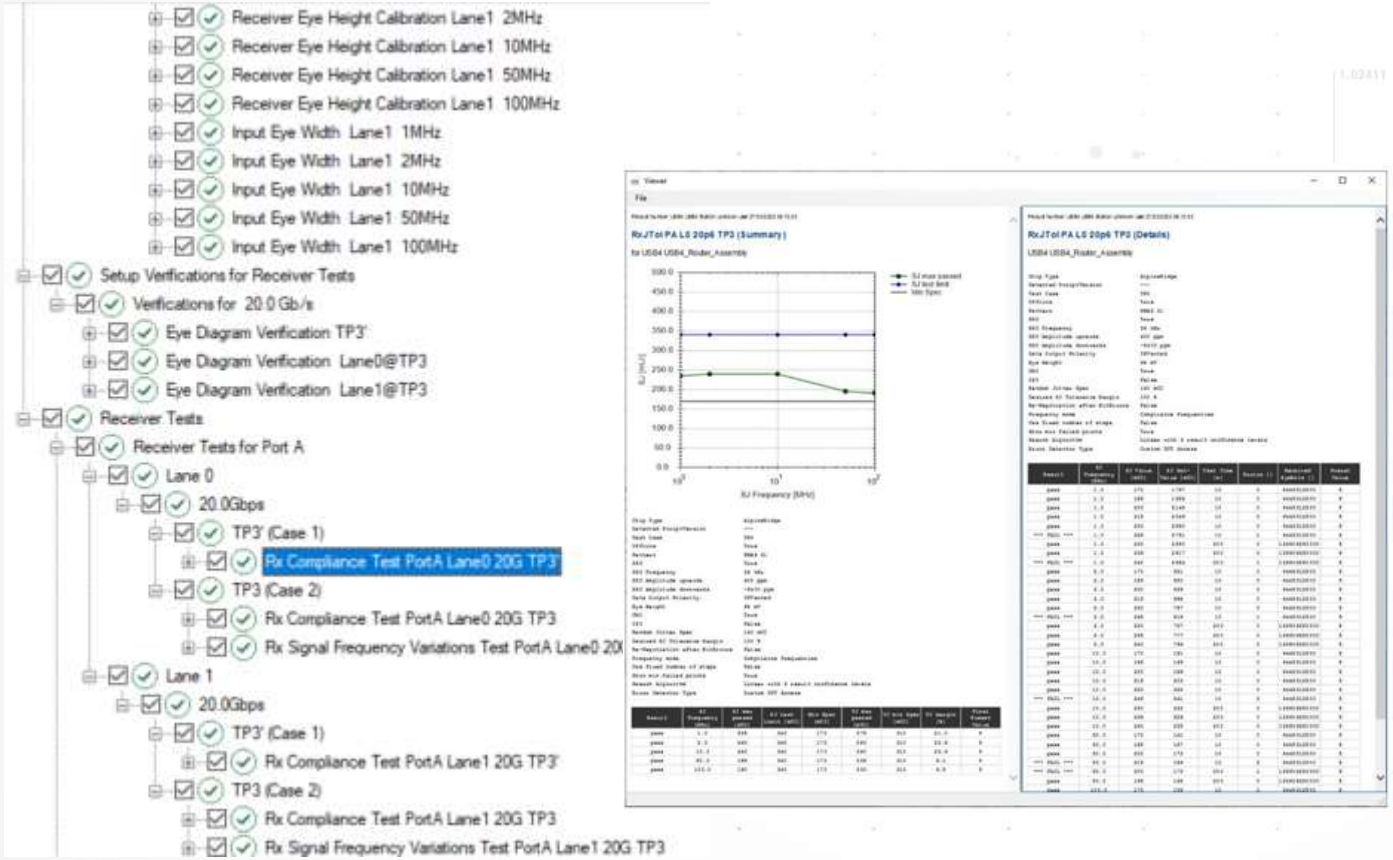
# Receiver Uncoded BER

- The receiver shall operate at uncoded BER of 1E-12 with stressed signal applied
- Two test setups are used for evaluating the receiver tolerance:
  - “Case1” addressing installations with low insertion-loss
  - “Case2” addressing installations with maximum insertion-loss



# USB4 Electrical Receiver Test Proposal

- Support Both M8020A and M8040A BERT
- N5991U40A USB4 Receiver Compliance Test Software



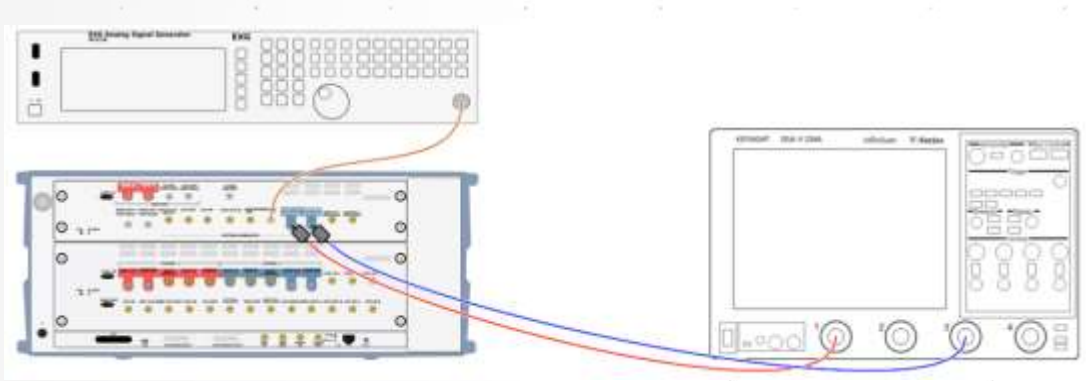


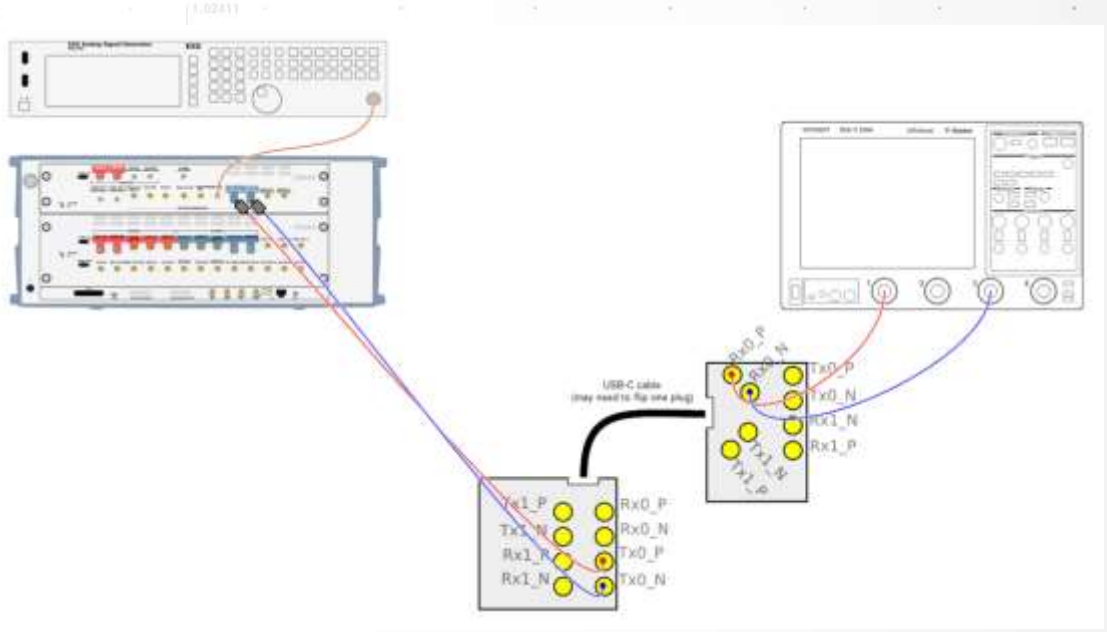

M8020A J-BERT + M8062A 32Gbps MUX

M8040A 32/64 Gbaud J-BERT

# USB4 Test Setup (M8020A): Calibration for Case 1 and Case 2

| Case 1 (Near End) | Case 2 (Far End) |
| --- | --- |

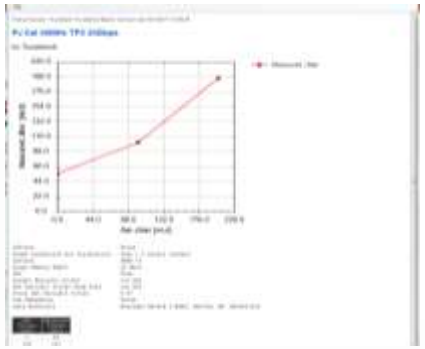


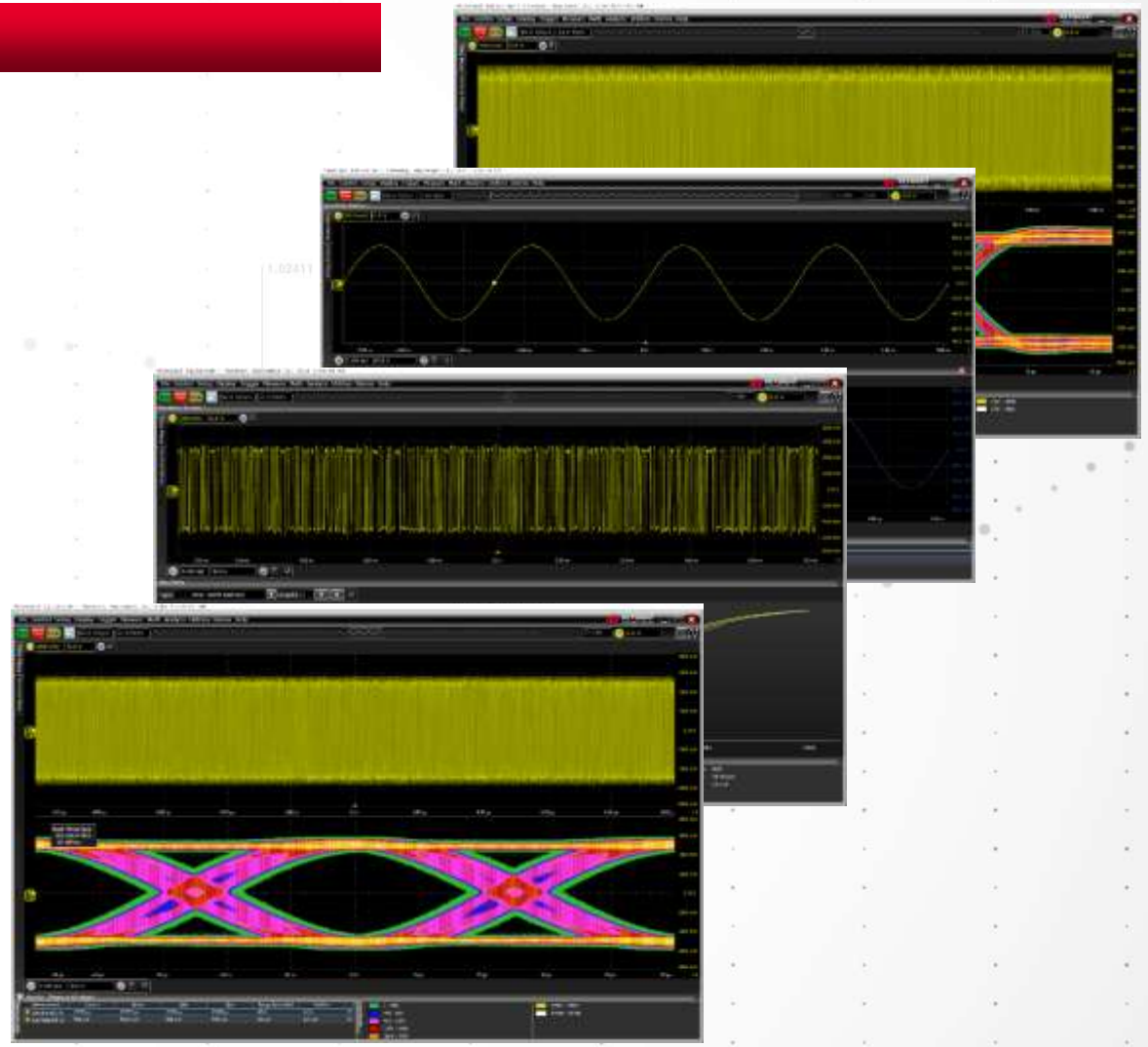


# USB4 Receiver Test Calibration for 10Gb/s, 10.3125Gb/s, 20Gb/s and 20.625 Gb/s

## THUNDERBOLT CTS V1.5 SECTION 4.2

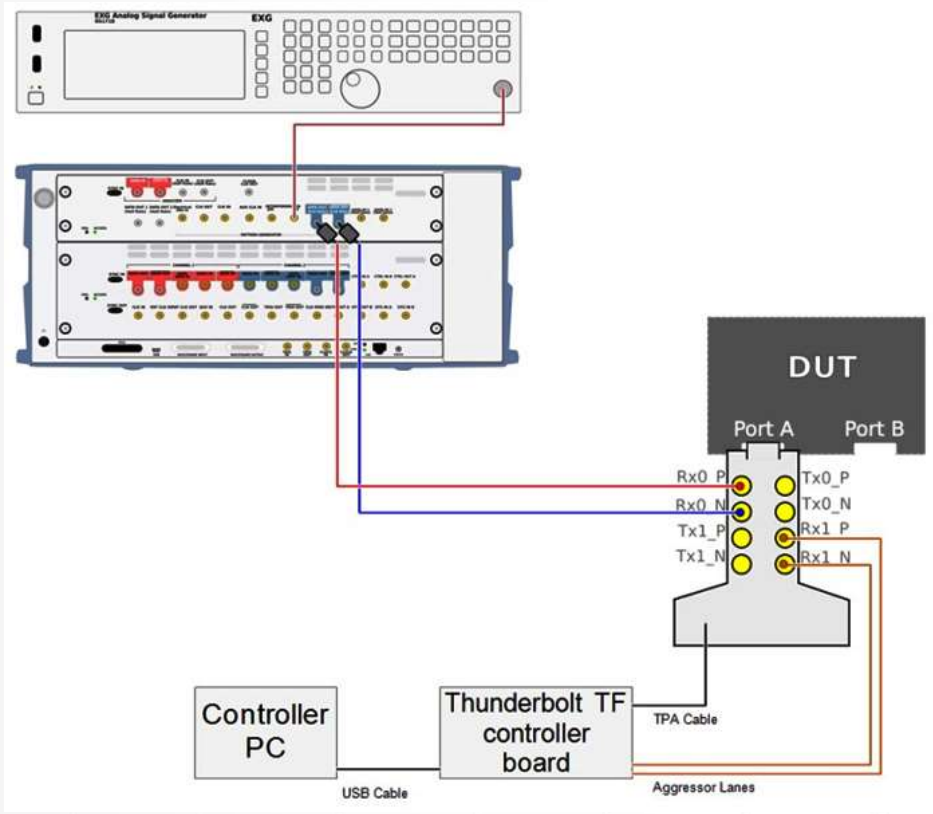
1. Select TX Equalization Preset for TP2 (Case 1)
2. Calibrate AC Common Mode for TP2 (Case 1)
3. Calibrate Random Jitter for TP2 (Case 1)
4. Calibrate Total Jitter at TP2 (Case 1) for all PJ frequencies: 1 MHz, 2 MHz, 10 MHz, 50 MHz and 100 MHz
5. Calibrate Eye Diagram at TP2 (Case 1) for all PJ frequencies: 1 MHz, 2 MHz, 10 MHz, 50 MHz and 100 MHz
6. Calibrate Total Jitter at TP3EQ (Case 2) for all PJ frequencies: 1 MHz, 2 MHz, 10 MHz, 50 MHz and 100 MHz
7. Calibrate Eye Diagram at TP3EQ (Case 2) for all PJ frequencies: 1 MHz, 2 MHz, 10 MHz, 50 MHz and 100 MHz

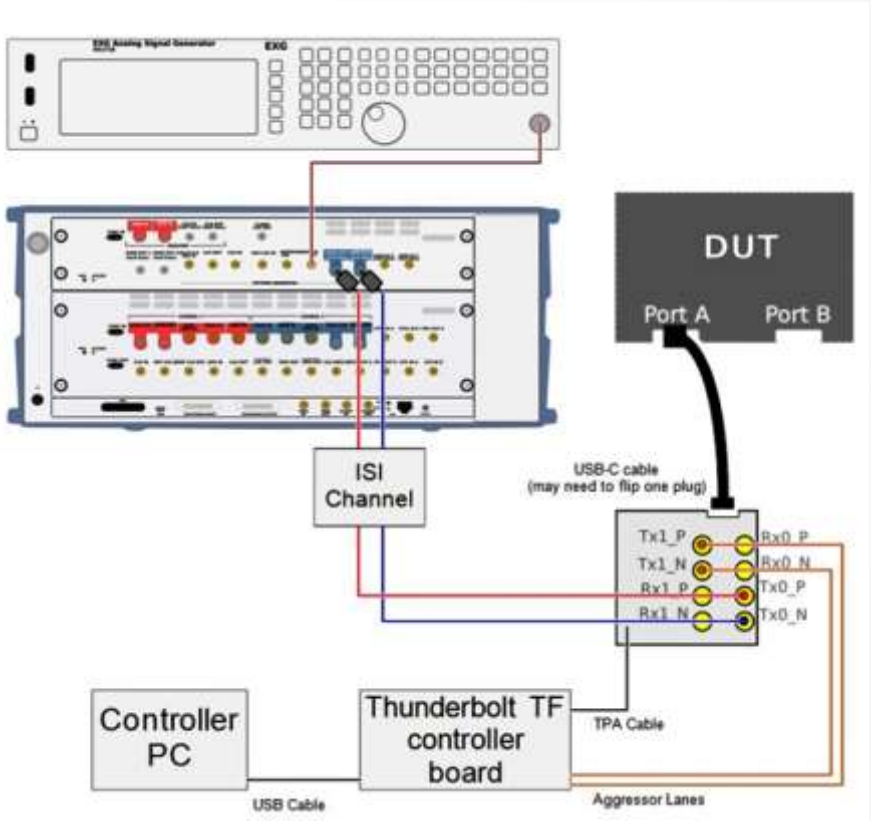




# USB4 Test Setup (M8020A): Case 1 and Case 2 Execution

| Case 1 (Near End) | Case 2 (Far End) |
| --- | --- |



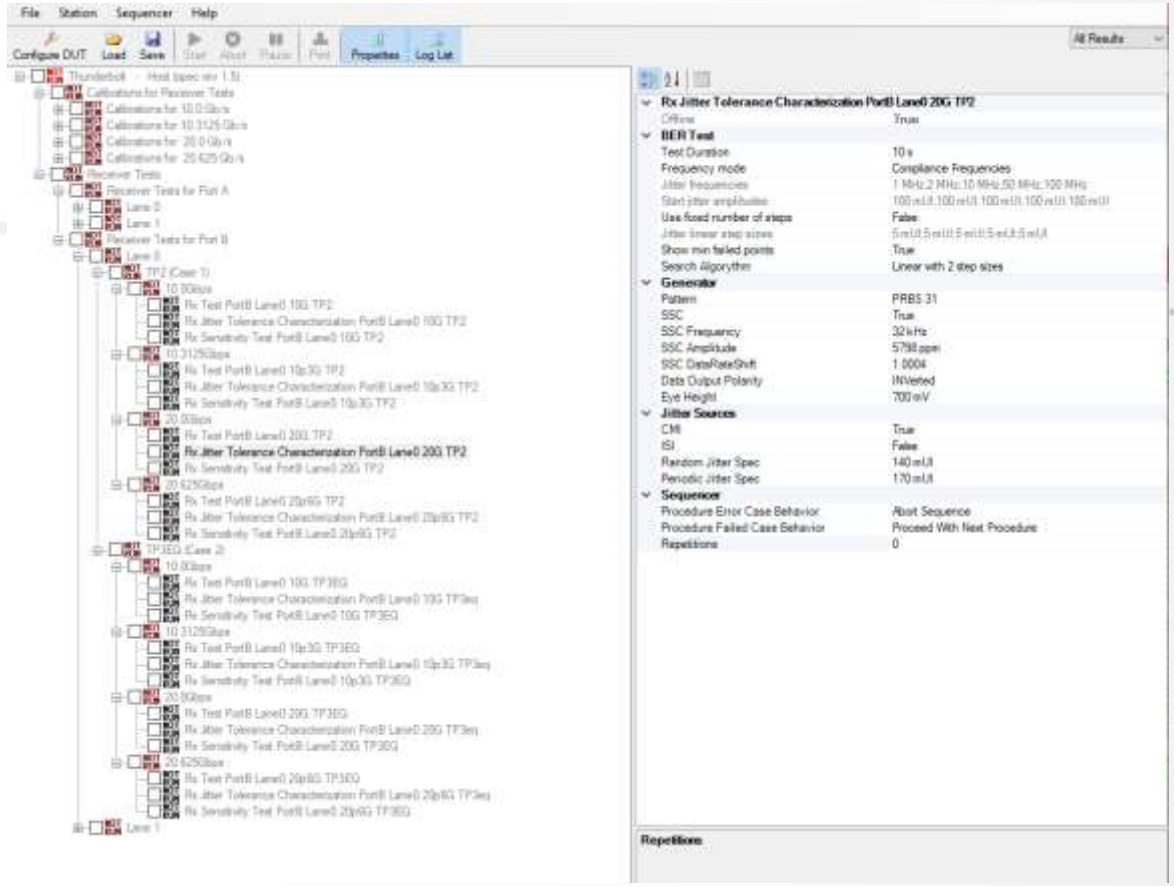



# USB4 Receiver Test Execution

## THUNDERBOLT CTS V1.5 SECTION 4.3

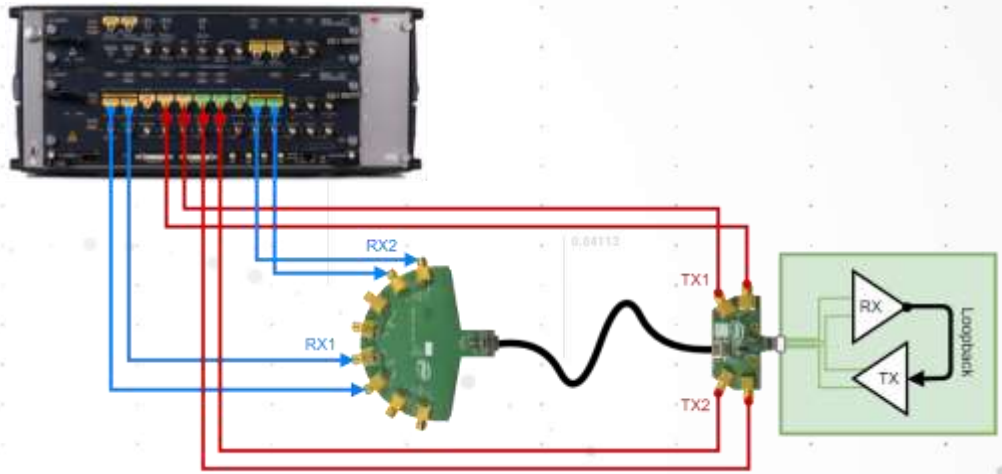
1. Connect the DUT for Receiver testing.
2. Recall Test Case 1 calibrated setup that was saved previously.
3. Negotiate Equalization Preset with the DUT
4. Run BER Test for 400s (Gen2) or 200s (Gen3)
5. If Error count >0, repeat step 4 but for 700s (Gen2) or 350s (Gen3)
6. If Error Count >2, FAIL the test, otherwise PASS
7. Repeat steps 2 to 6 for Test Case 2
8. Repeat steps 2 to 7 for all ports, speeds and PJ settings

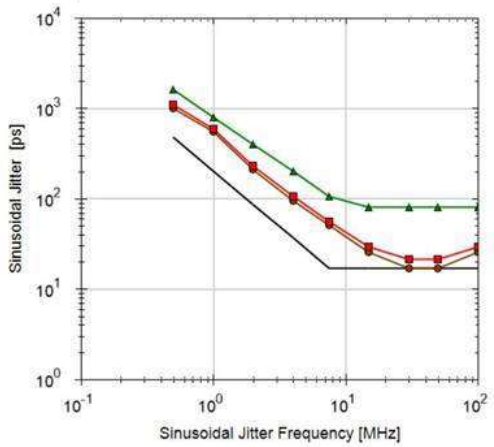
Keysight provides simple, repeatable automated and unattended calibration and test execution using automation SW for Tx and Rx Test



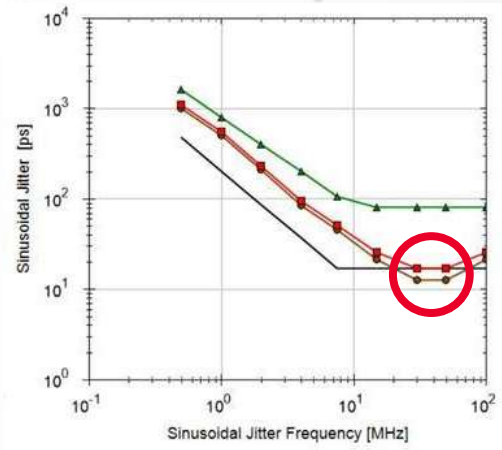
# USB3.2 x 2 Receiver Testing (BKM)

- Two Pattern Generators / Error Detectors
- Two independent RX paths fully calibrated
- Link Training in x2 mode
- **Concurrent** JTOL on both RX lanes
- USB-like traffic during test
- Test setup **like operating conditions**




**x1 vs x2**



# N7019A USB Type-C Active Link Test Fixture

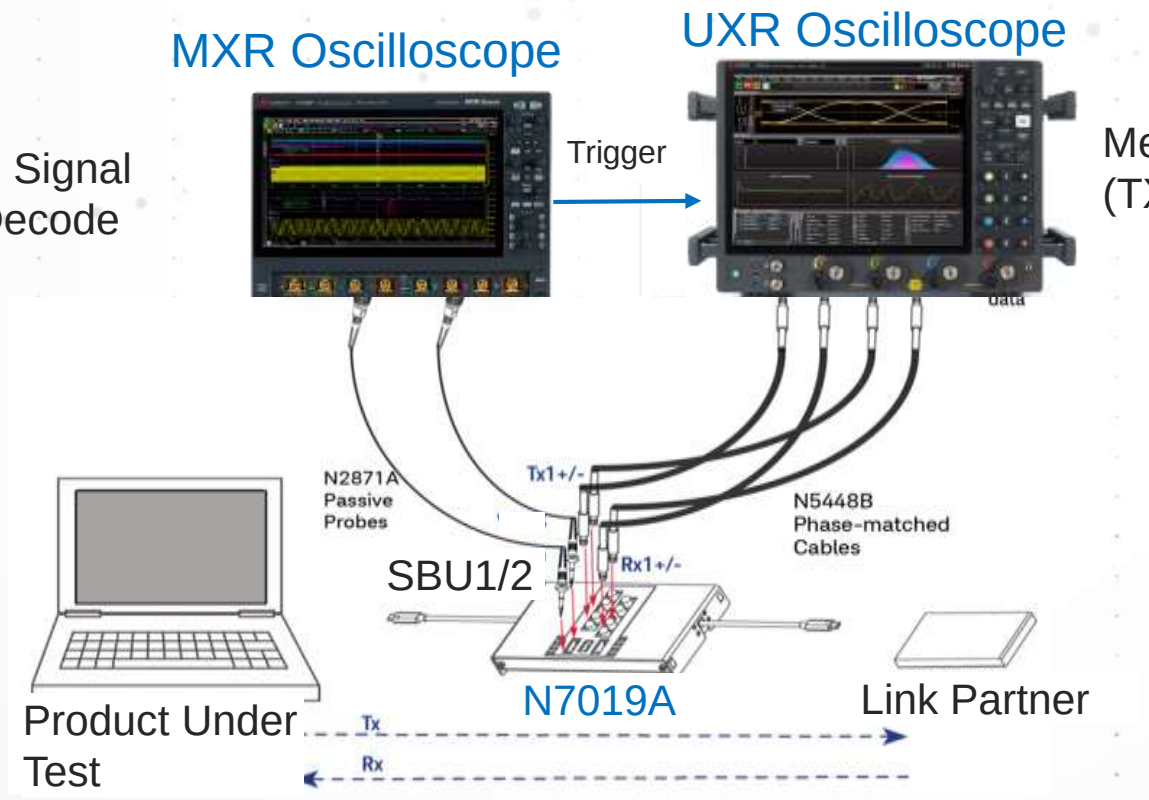

Provides access to all Type-C signals during an active link

Signals include Vbus, USB 2.0, USB-PD, SBU1/2, and TX/RX up to maximum USB4 rate of 20 Gbps

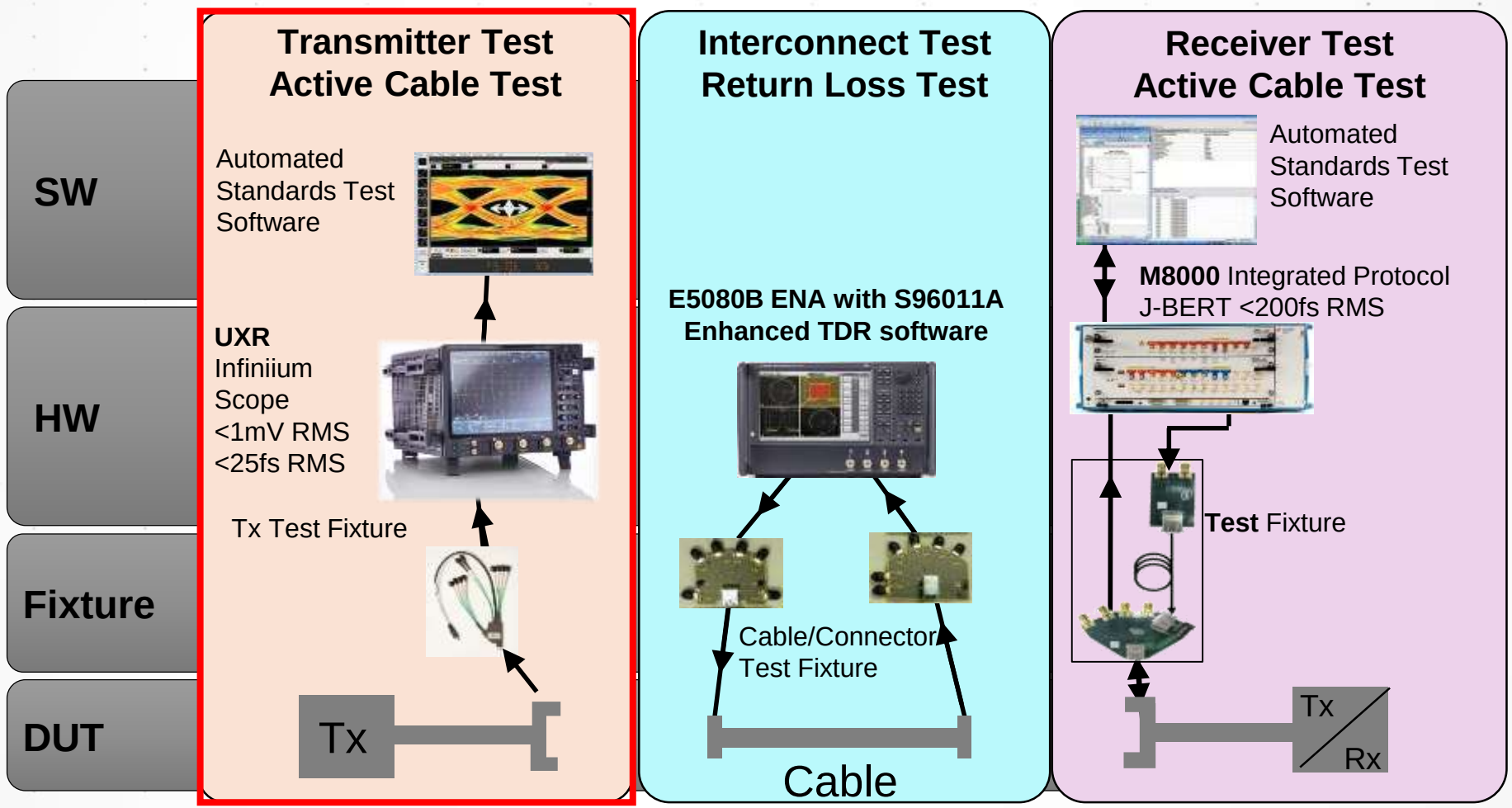
Works in conjunction with Keysight Protocol Trigger Decode solutions for USB-PD, USB 2.0, USB 3.2, and USB4

## N7019A Usage

Measure Low Speed Signal (SBTX/SBRX) and Decode



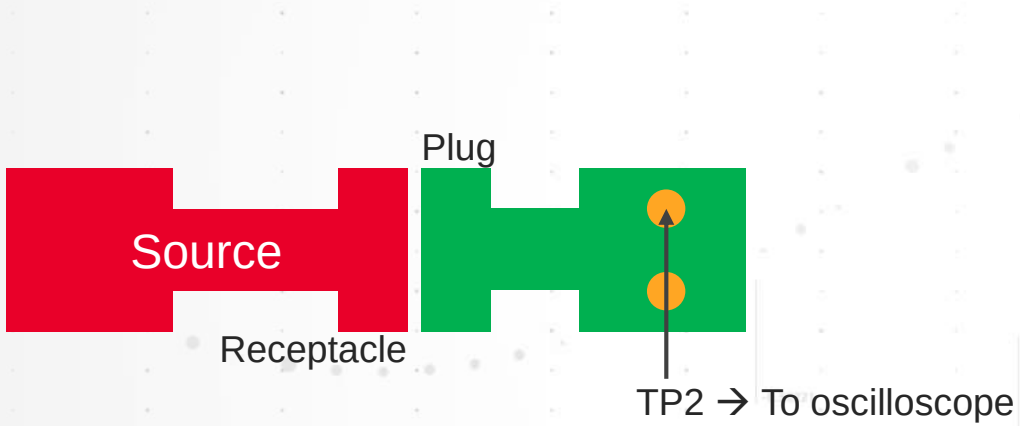
# Keysight USB4 Test Solution

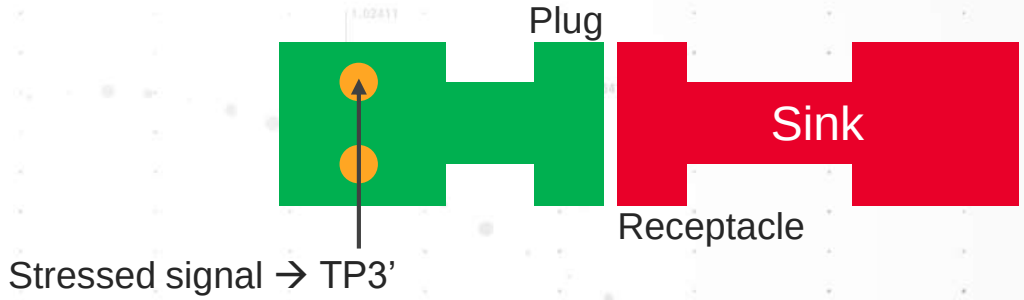


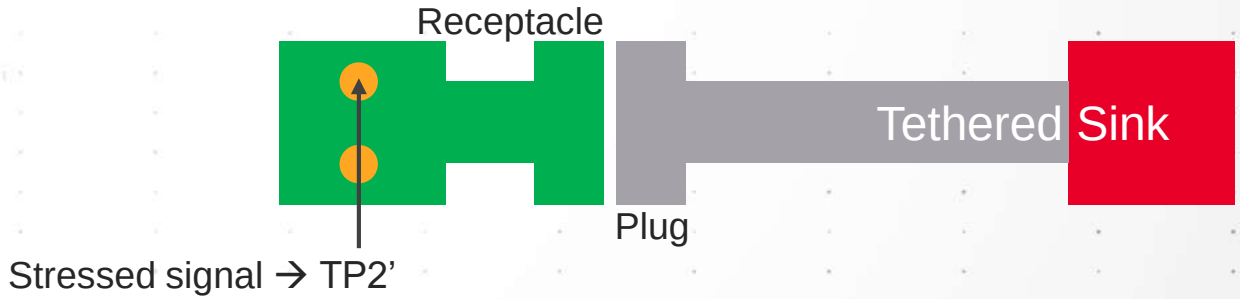
# DP Compliance Program

- Managed by VESA
  - Jim Choate (former Agilent USB Pyramid Lead)
- Why do companies need the logo?
  - Ensure interoperability
  - Consumers can easily identify compliant products
- How to get it?
  - Pass the Compliance Program
  - Be a member of VESA
  - Sign the VESA DisplayPort Trademark License Agreement
- Authorized Test Centers (ATCs)
  - Allion, GRL, TTA, UL

# DP Test Point Access

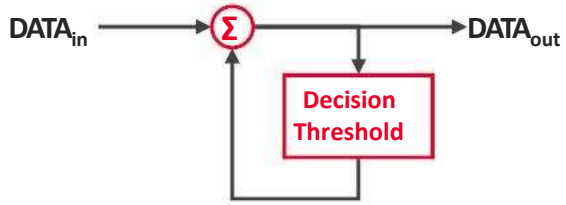


# DP2.0 Equalization

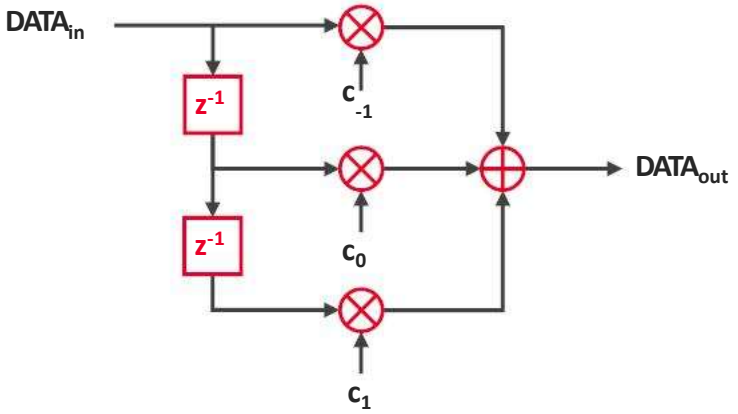
- DPTX: 3-tap FFE (16 presets)
- DPRX: CTLE (10 DC gain levels) + DFE
- Full characterization → 16 x 10 = **160 combinations**

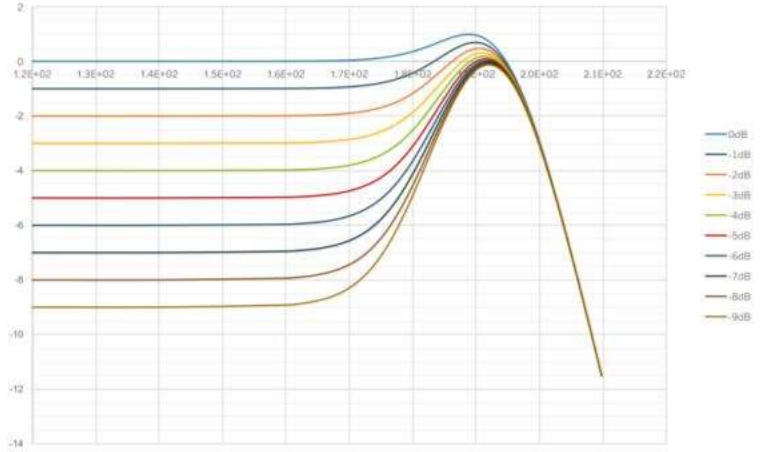



| Preset Number | Pre-shoot [dB] | De-emphasis [dB] | Informative Filter Coefficients | | |
|---|---|---|---|---|---|
| | | | $C_{-1}$ | $C_0$ | $C_1$ |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | −1.9 | 0 | 0.90 | −0.10 |
| 2 | 0 | −3.6 | 0 | 0.83 | −0.17 |
| 3 | 0 | −5.0 | 0 | 0.78 | −0.22 |
| 4 | 0 | −8.4 | 0 | 0.69 | −0.31 |
| 5 | 0.9 | 0 | −0.05 | 0.95 | 0 |
| 6 | 1.1 | −1.9 | −0.05 | 0.86 | −0.09 |
| 7 | 1.4 | −3.8 | −0.05 | 0.79 | −0.16 |
| 8 | 1.7 | −5.8 | −0.05 | 0.73 | −0.22 |
| 9 | 2.1 | −8.0 | −0.05 | 0.68 | −0.27 |
| 10 | 1.7 | 0 | −0.09 | 0.91 | 0 |
| 11 | 2.2 | −2.2 | −0.09 | 0.82 | −0.09 |
| 12 | 2.5 | −3.6 | −0.09 | 0.77 | −0.14 |
| 13 | 3.4 | −6.7 | −0.09 | 0.69 | −0.22 |
| 14 | 3.8 | −3.8 | −0.13 | 0.74 | −0.13 |
| 15 | 1.7 | −1.7 | −0.05 | 0.55 | −0.05 |

Notes:
1. The coefficients are normalized such that $|C_{-1}| + C_0 + |C_1|$ corresponds to full output swing. Preset configuration 15 represents operation mode with lower transmitter swing.
2. Preshoot and de-emphasis are calculated as following:

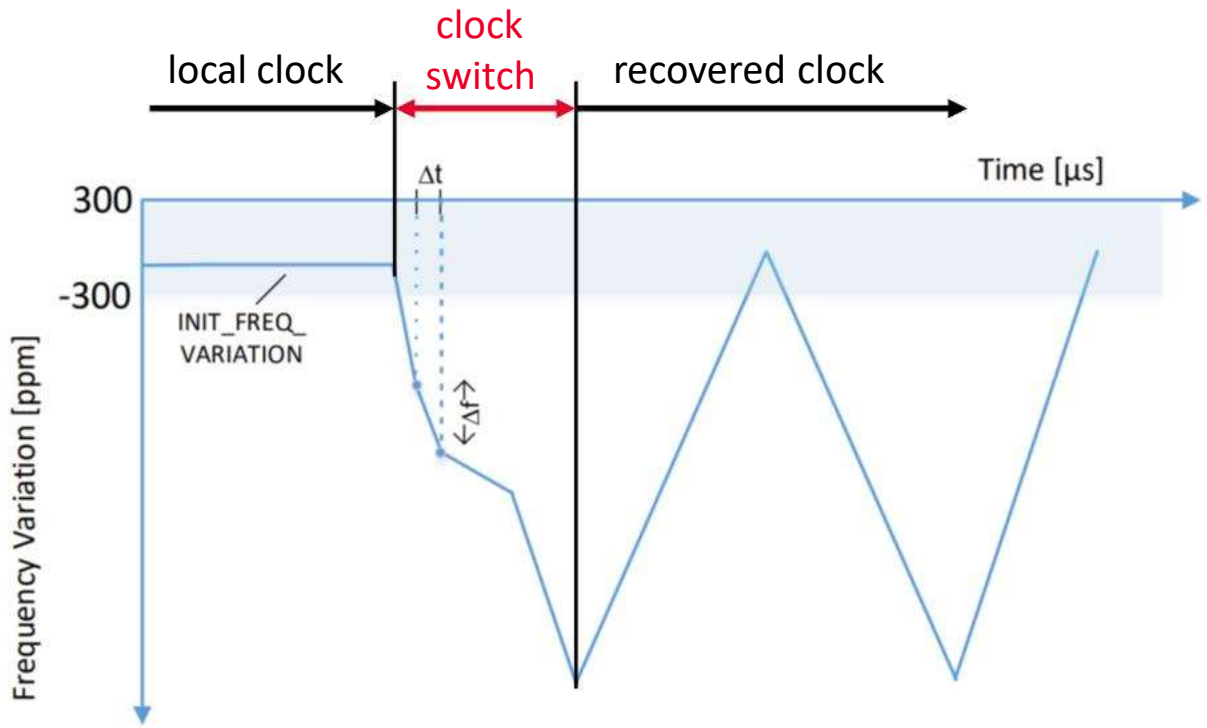
$$Preshoot = 20 \cdot \log 10\left(\frac{-C_{-1}+C_0+C_1}{C_{-1}+C_0+C_1}\right) \qquad De-emphasis = 20 \cdot \log 10\left(\frac{C_{-1}+C_0+C_1}{C_{-1}+C_0-C_1}\right)$$



# LTTPRs

- LTTPRs are needed as total channel loss increases with PHY rate
  - Longer channel
  - Extra latency
  - Longer and more complex link training
- Clock switch
  - During link training
  - 8b/10b in transparent mode
  - 128b/132b – SCR in progress
- Test methodology in development



# How to test DP PHY layer?

## Source

- Configure the source to output test patterns with certain drive settings → **AUX controller**
- Embed worst-case channels, apply equalization on the oscilloscope
- Run measurements

## Sink

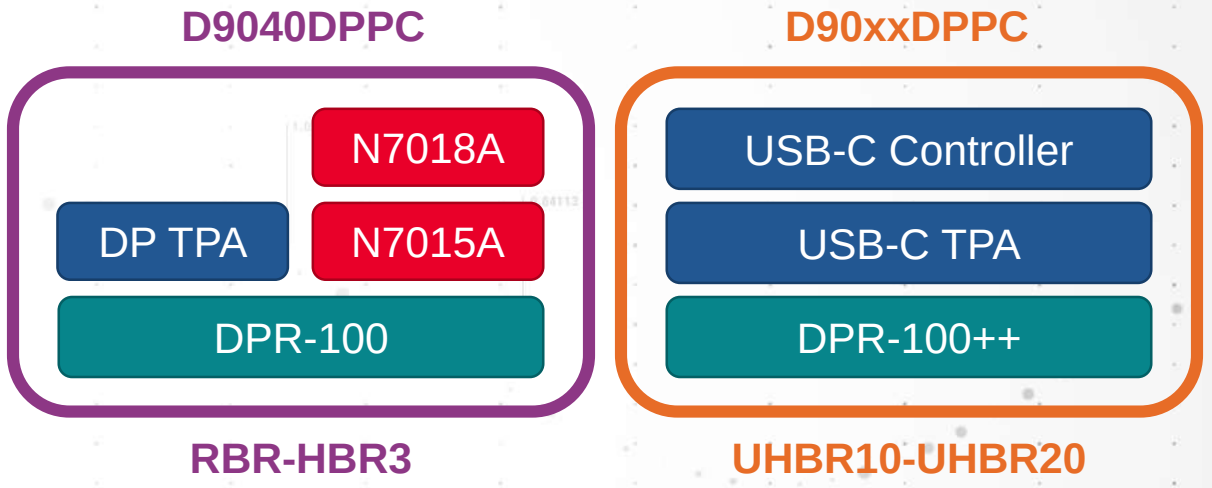
- Generate the stress signal with a pattern generator
- Guide the sink through Link Training → **AUX controller**
- Read built-in error counter

# DP Source Compliance Test

## SOFTWARE PACKAGES

Wilder | Keysight | Unigraf

- **Updated** software package D9040DPPC
- **New** software package D90xxDPPC
- Productivity improvements
  - ANPL
  - Disaggregation



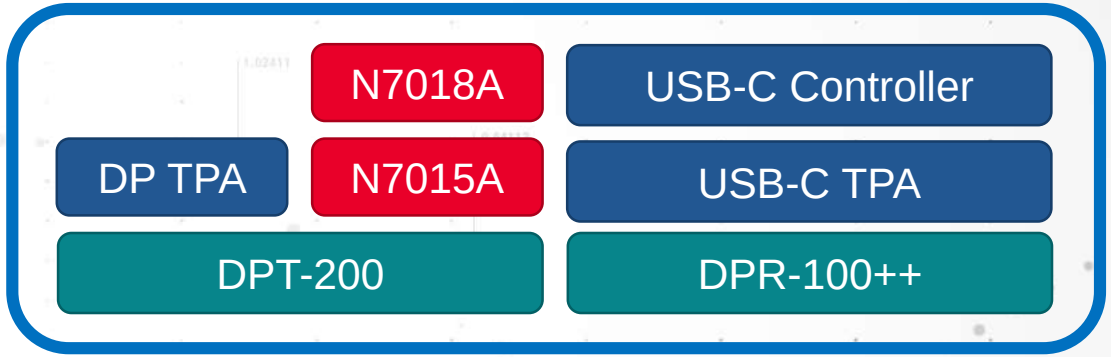

# DP Sink Compliance Test

**SOFTWARE**

Wilder | Keysight | Unigraf

- **New** software package N5991xxxA
- Automated sink calibration and tests
- All PHY rates **from RBR to UHBR20**
- Standard DP connector and USB Type-C

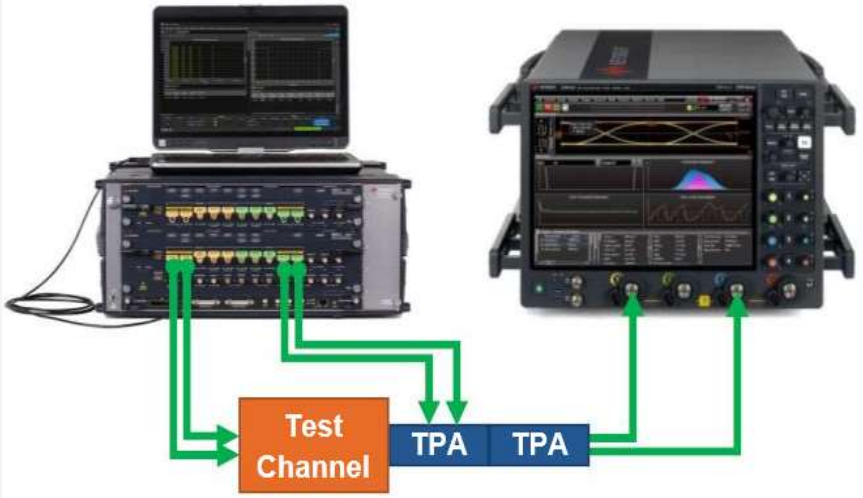
**N5991xxxA**

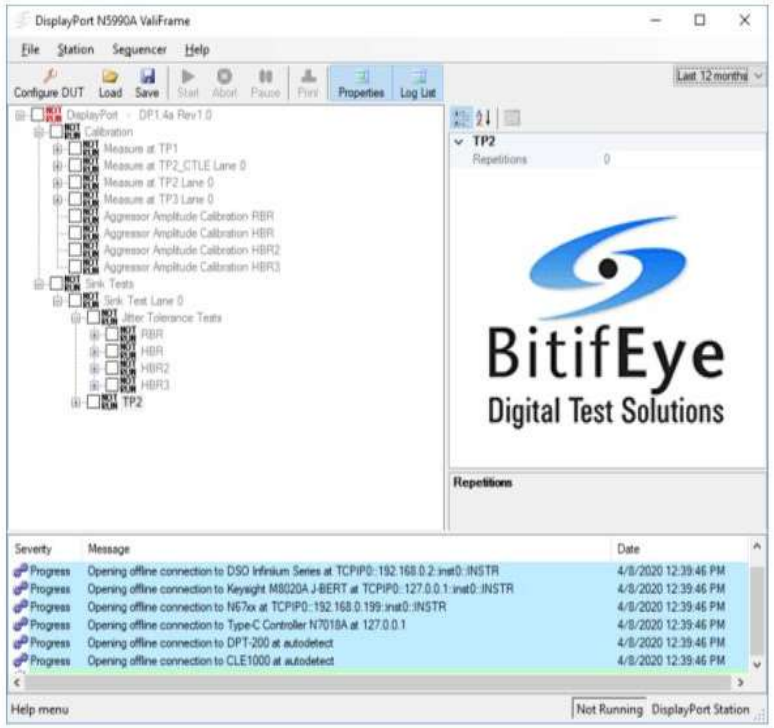



**RBR-UHBR20**

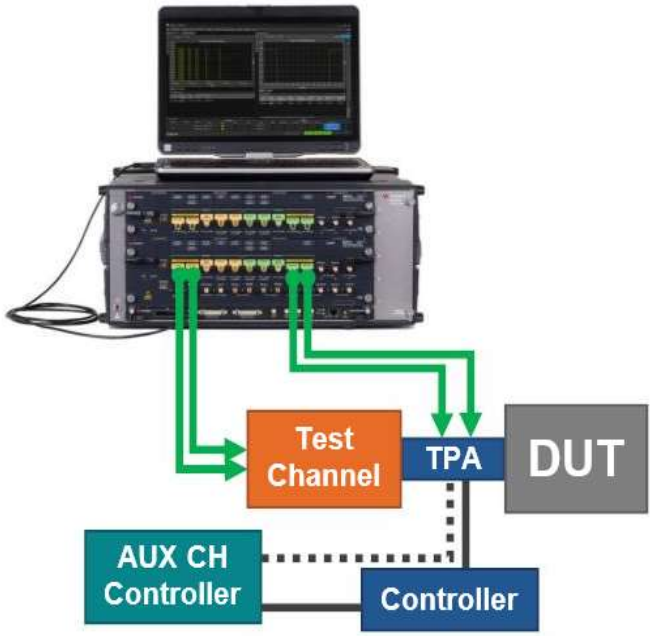
# DP Sink Compliance Test

## Calibrations




## Sink Tests



# Q & A


KEYSIGHT
WORLD 2020