KEYSIGHT WORLD 2020

Get Ready for the Gen5 Wave with PCIe Technologies

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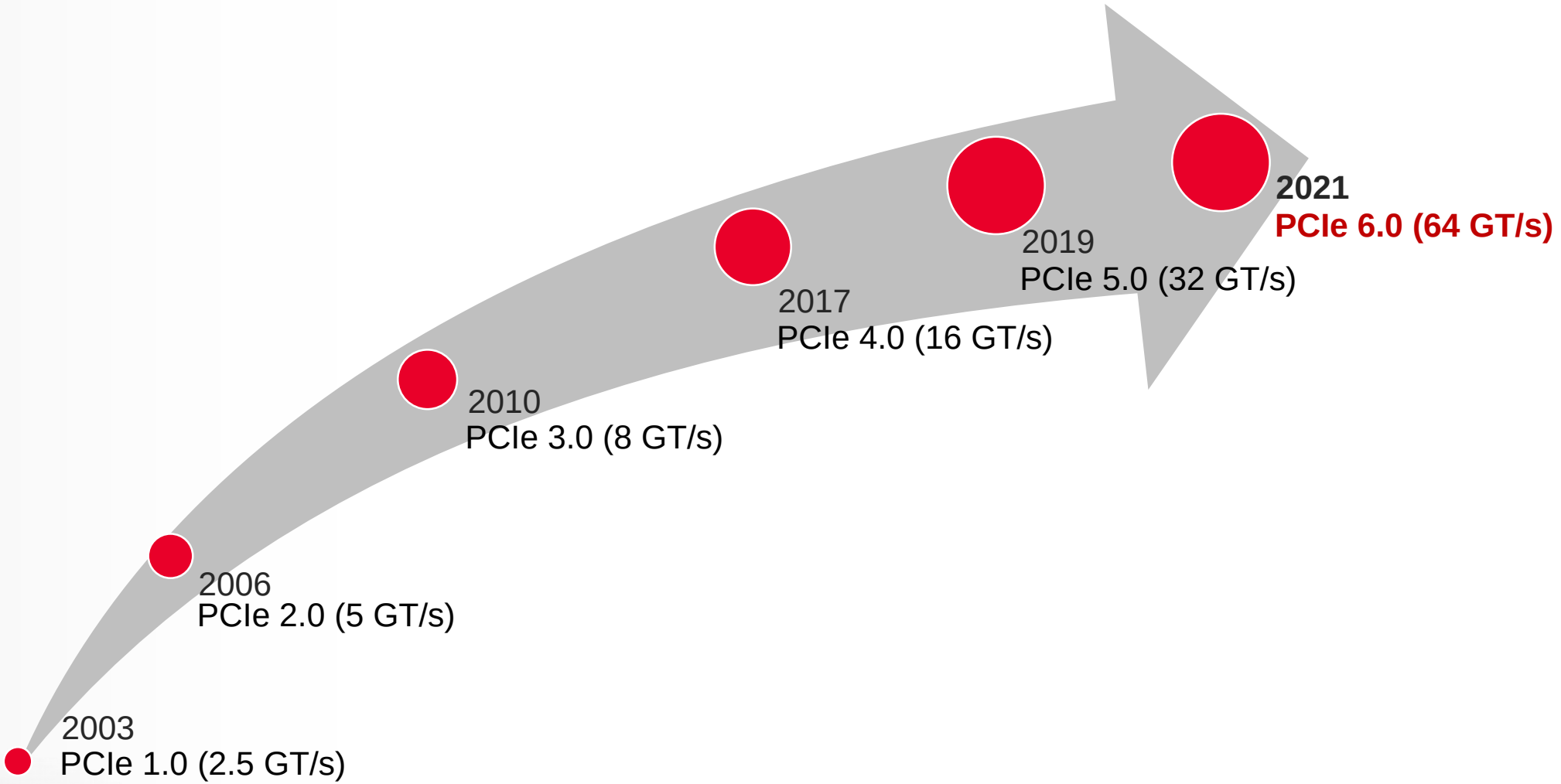
Agenda

- **PCIe 5.0 Development Timeline**
  - PCIe 5.0 and High Speed IO Standards
- **PCIe 5.0 Rx Test Calibration Considerations**
  - VNA vs Step Response - Determining ISI channel loss
- **PCIe 5.0 TX Test Consideration & Tools**
  - Base & CEM Scope Considerations
- **PCIe 4.0 CEM Dual Port Testing**
- **PCIe 6.0 64GT/s Pathfinding**
  - PCIe 5.0 to 6.0: From NRZ to PAM4

PCIe 5.0 Development Timeline

PCIe 5.0 and High Speed IO Standards

PCI Express Technology Roadmap

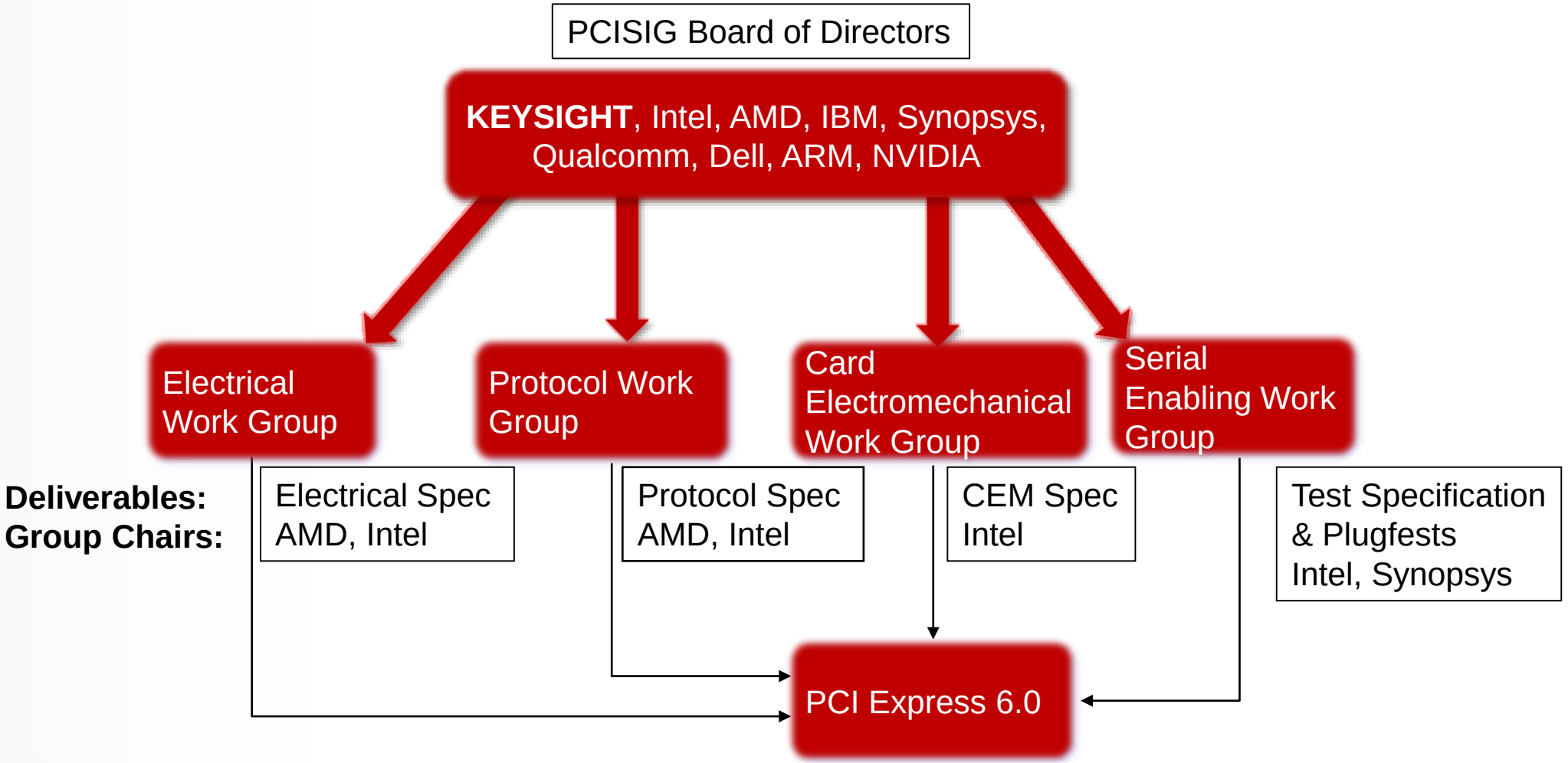


Computer I/O Innovations in Bus Technologies

PCIE, CCIX, GENZ, OPENCAPI

Standard	Physical Layer	Topology	Unidirectional BW	Mechanicals	Coherence
PCIe 6.0	PCIe Phy PAM4	p2p switched	64 Gb/s x16	PCIe	No
PCIe 5.0	PCIe Phy NRZ	p2p switched	32 Gb/s x16	PCIe	No
PCIe 4.0	PCIe Phy NRZ	p2p switched	16 Gb/s x16	PCIe	No
GenZ 1.0	IEEE 802.3 PCIe Phy	p2p switched & meshed	16/25/56 Gb/s per lane x256	SFF-TA	Full cache coherence
OpenCAPI 3.0	IEEE 802.3	p2p	25 Gb/s per lane x8	-	Coherent to system memory
CXL 1.1	PCIe 5.0	“all-to-all”	32 Gb/s x16	PCIe	Coherency between CPU and attachments

PCI Express Standards Development

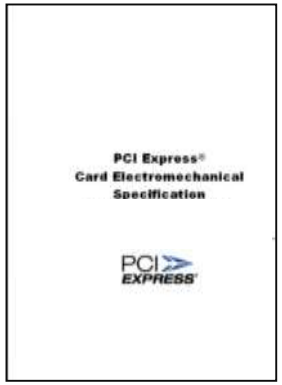


PCI Express Specifications and Scope

SELECT THE SPECIFICATIONS FOR YOUR SPECIFIC NEED

Base Specification
- Contains all the system knowledge
- Can directly be applied to Chip Test

PCIe 5.0 BASE
Released 1.0 May 2019



Card Electromechanical (CEM) Spec
- Applies to add-in cards and mother boards
- Mitigates card manufacturer's need to study the base specification
- Increases reproducibility through PCI-SIG supplied test tools CBB and CLB (compliance base and load board)

PCIe_CEM_SPEC_R5_V0.7.
Released Ver0.7 in June 2019

Phy Test Specification
- Defines compliance tests of CEM spec in detail

Latest
PCIe_5_0_PHY_Test_Spec_Ver0.5
Released Ver0.5 in June 2019

PCIe 5.0 – Goals

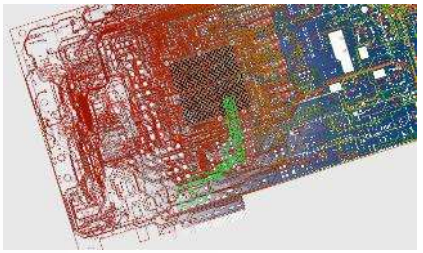
DELIVERING THE FASTEST PCIE SPEED YET

- PCIe 5.0 is backwards compatible with prior generations
  - Enhanced SMT connector
  - Same pinout
- Signaling is doubled (vGen4) to 32 GT/s
  - Minimal spec changes – only ones needed to enable speed bump
  - EIEOS changed to maintain frequency
  - Encoding remains 128/130
  - Loss budget: Goal 35-36 dB
  - Equalization: 8 GT->16 GT-> 32 GT/s
  - > 2x Tx jitter reduction
  - ~3x Reference Clock jitter reduction
  - Improved 32 GT/s Reference CTLE equalization, 3 tap DFE
  - BER target is 10e-12
- Same approach for TX and RX testing used for Gen4
  - Similar method for TX testing via de-embedding of breakout board traces
  - Similar method for calibrating the eye width and eye height as used with PCIe 4.0 (ISI based, fixed RJ)

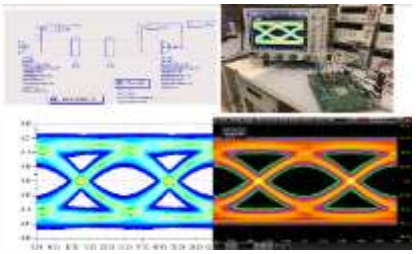
PCI Express® 5.0 – Keysight Total Solution

Physical Layer – System Simulation

ADS Design Software

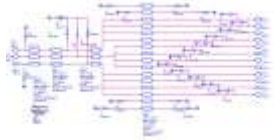


SIPro/PIPro



Simulation to Measurement Correlation

Physical layer – interconnect design



ADS design software

86100D DCA-X/TDR

N5227B PNA w/ PLTS

Physical layer- transmitter test

UXR-Series, Z-Series Real-Time Oscilloscopes

D9050PCIC PCI Express 5.0 TX Electrical compliance software

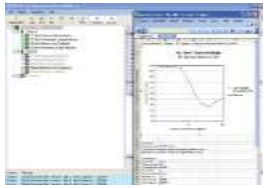
86100CU-400 PLL and Jitter Spectrum Measurement SW

Physical layer- receiver test

M8046A J-BERT High Performance BERT w/ integrated CDR + M8054A Interference Source

M8049A-1 Substitute PCIe 5 BASE Channel board

N5991PB5A
PCIe 5.0 32GT/s RX Test software



Complete System Simulation
From Pre-layout analysis to Post-layout extraction

Verify PCIe 5.0 Compliant Channels
Verify Return Loss Compliance
Capture break-out channel S-Params

DSA UXR-Series & Z-Series Real-Time Oscilloscopes

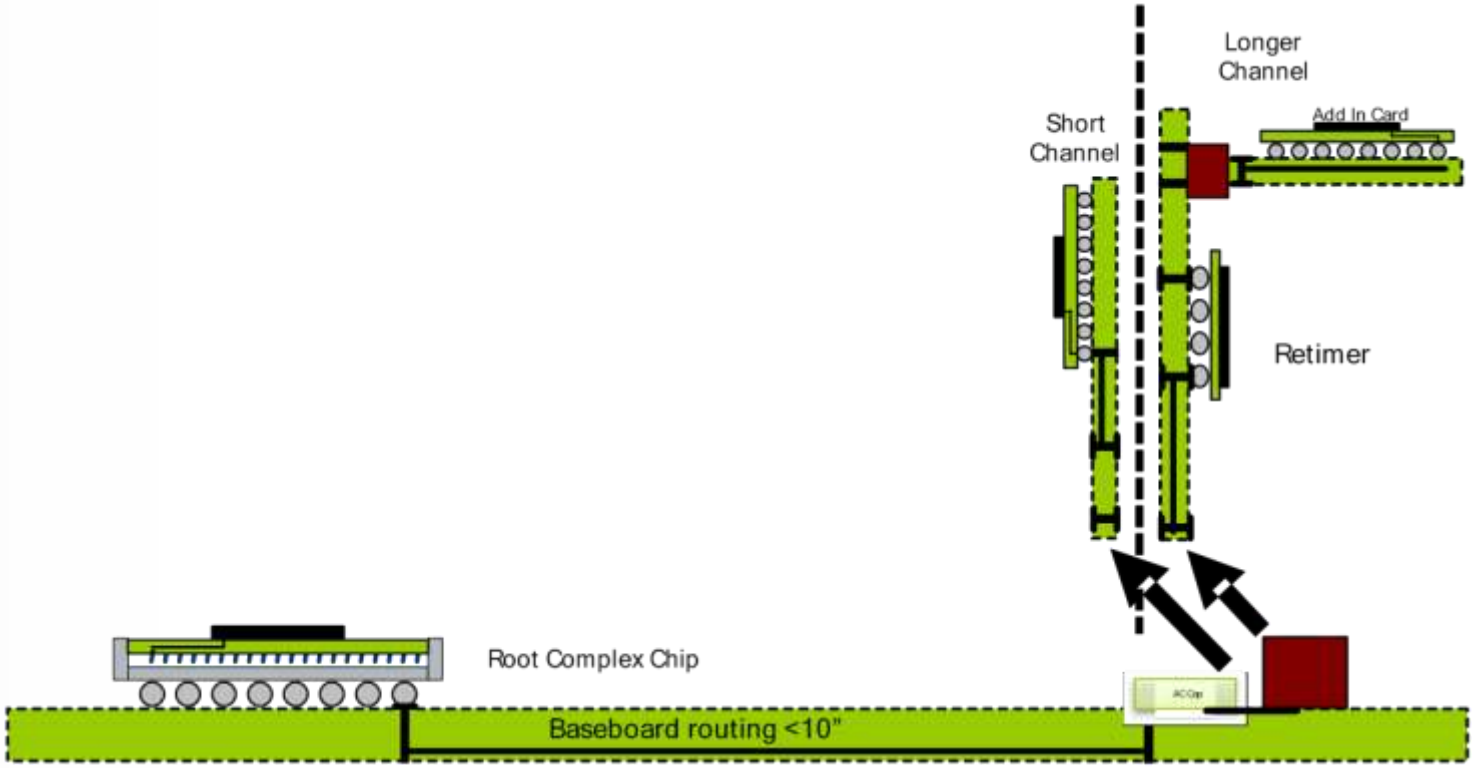
Automated RX Test software
- Accurate, Efficient
- Comprehensive RX Testing

PCIe 5.0 Rx Test Calibration Considerations

VNA vs Step Response - Determining ISI channel loss

PCI Express 5.0 Channel Topology

RETIMER REQUIRED WHEN LOSS EXCEEDS -36 DB OR >1 CONNECTOR



- Estimated allowable loss: ~= -36 dB @ 16 GHz
- Root complex pkg loss allowance ~= -9 dB @ 16 GHz
- Add-in Card pkg loss allowance ~= -4 dB @ 16 GHz
- Total AIC loss budget estimate = ~9 dB @ 16 GHz
- PCIe 5.0 CEM Connector loss budget ~= 1.5 dB @ 16 GHz

PCIe 5.0 32 GT/s RX Calibration (BASE)

15 MV EYE HEIGHT POST EQ (0.3UI EYE WIDTH) TARGET

Heavily dependent upon physical ISI channel

Optimal TX EQ
Diff Swing 800 mV

Calibration Channel
34-37 dB TP1 – TP2P

EH or EW Adjust

32.0 GT/s PRBS Generator

Combiner

CEM Connector

Replica Channel

Test Equipment

TP3

TP2

Constrained Impairments

Rj
.5 ps RMS

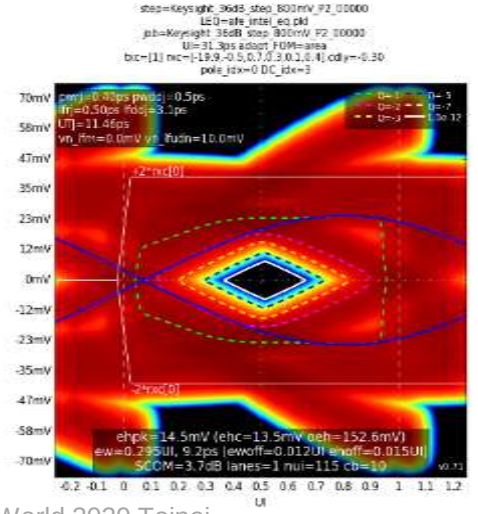
Sj
1-5 ps

Small EW Adjust

Diff
Interference
5 -30 mv

Small EH Adjust

CM
Interfer
ence



Post Processing Scripts:
Rx pkg model
Behavioral CTLE /DFE
Behavioral CDR

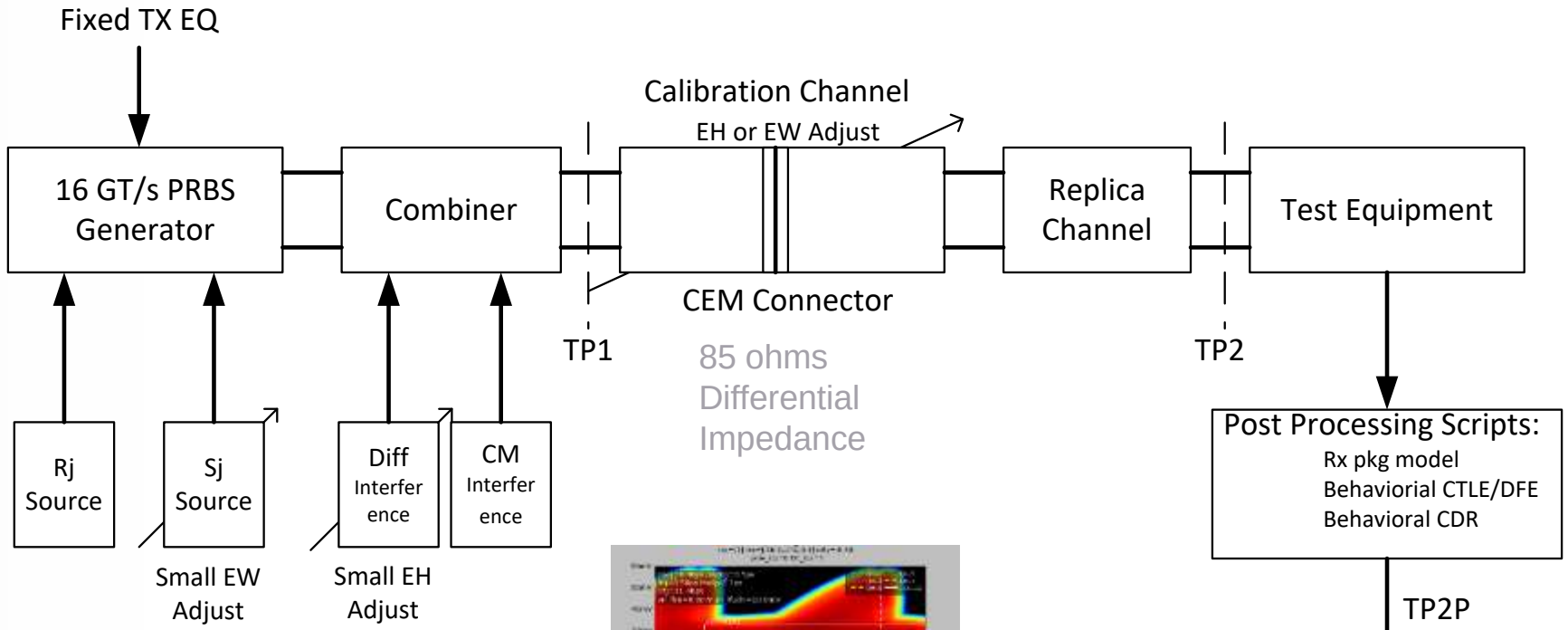
TP2P

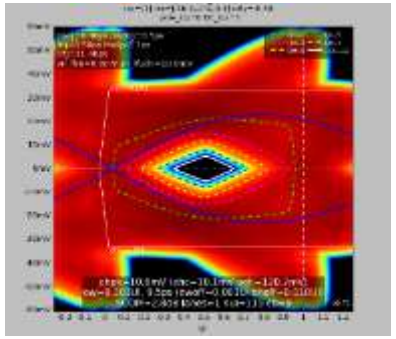
Very tight eye height margin.

15 mV / .3 UI at E-12 BER

PCIe 4.0 16 GT/s RX Calibration (BASE)

15MV EYE HEIGHT POST EQ (0.3UI EYE WIDTH) TARGET





15 mV / .3 UI at E-12 BER

Gen4 and Gen5 BERT Calibration

DIFFERENCES

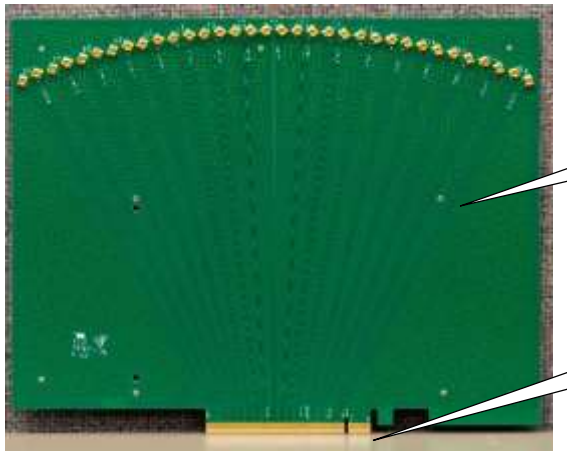
- PCI Express Channel Definition (for Calibration)
  - PCIe 4.0 includes BERT cable as part of the Rx calibration channel
  - PCIe 5.0 does not include extra cable connecting BERT to channel
    - M8040A has reference plane at the remote head+dedicated cable
- Steps for Closing Calibration
  - PCIe 4
    - PCIe 4 uses nominal stress values for SJ and DMSI (RJ is fixed)
    - PCIe 4 Objective: Find highest channel loss where EH & EW meet min Rx requirements
  - PCIe 5
    - Sweep SJ and DMSI through allowed ranges for a given amount of channel loss
    - Find the highest loss ISI channel pair where you can close the calibration while sweeping SJ and DMSI through the allowed ranges
- Calibration Assumptions
  - SJ allowances can help to adjust EW
  - DSMI allowances can help to adjust EH
  - In practice SJ changes EW and EH, and DMSI can change both EW & EH as well.

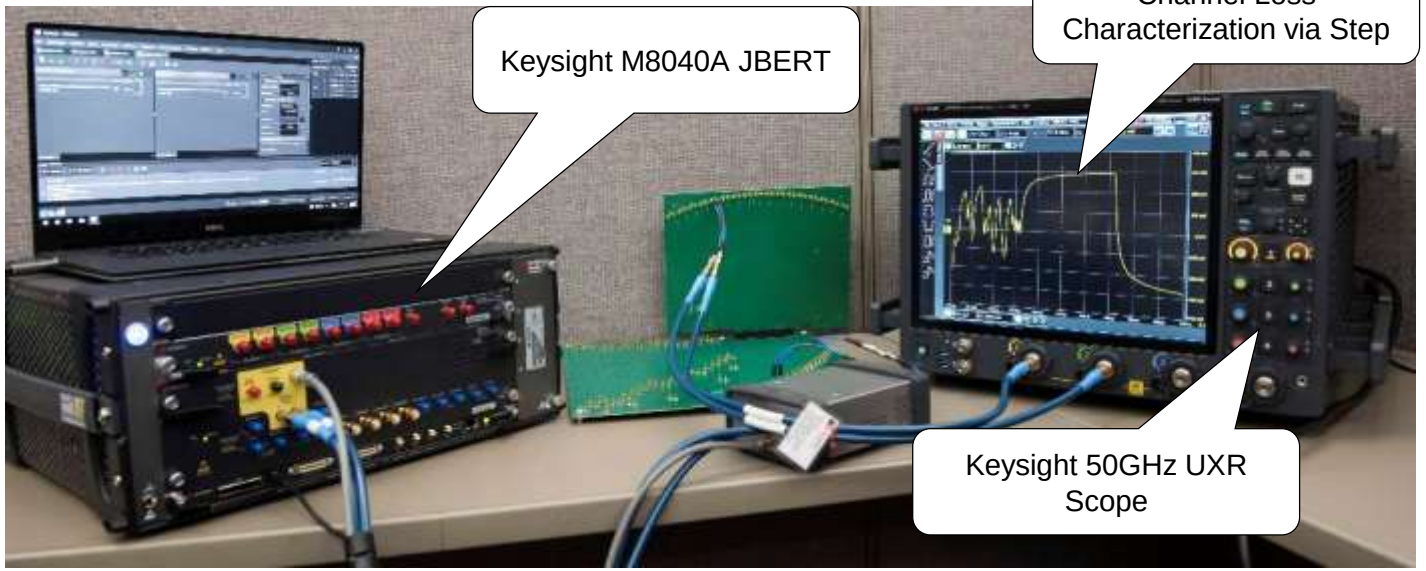
VNA vs Step Response

Determining ISI channel loss

PCIe 5.0 32 GT/s RX Calibration (BASE) Example

TARGET TEST CHANNEL BOARD W/ NEW CEM SMT CONNECTOR





VNA based Calibration

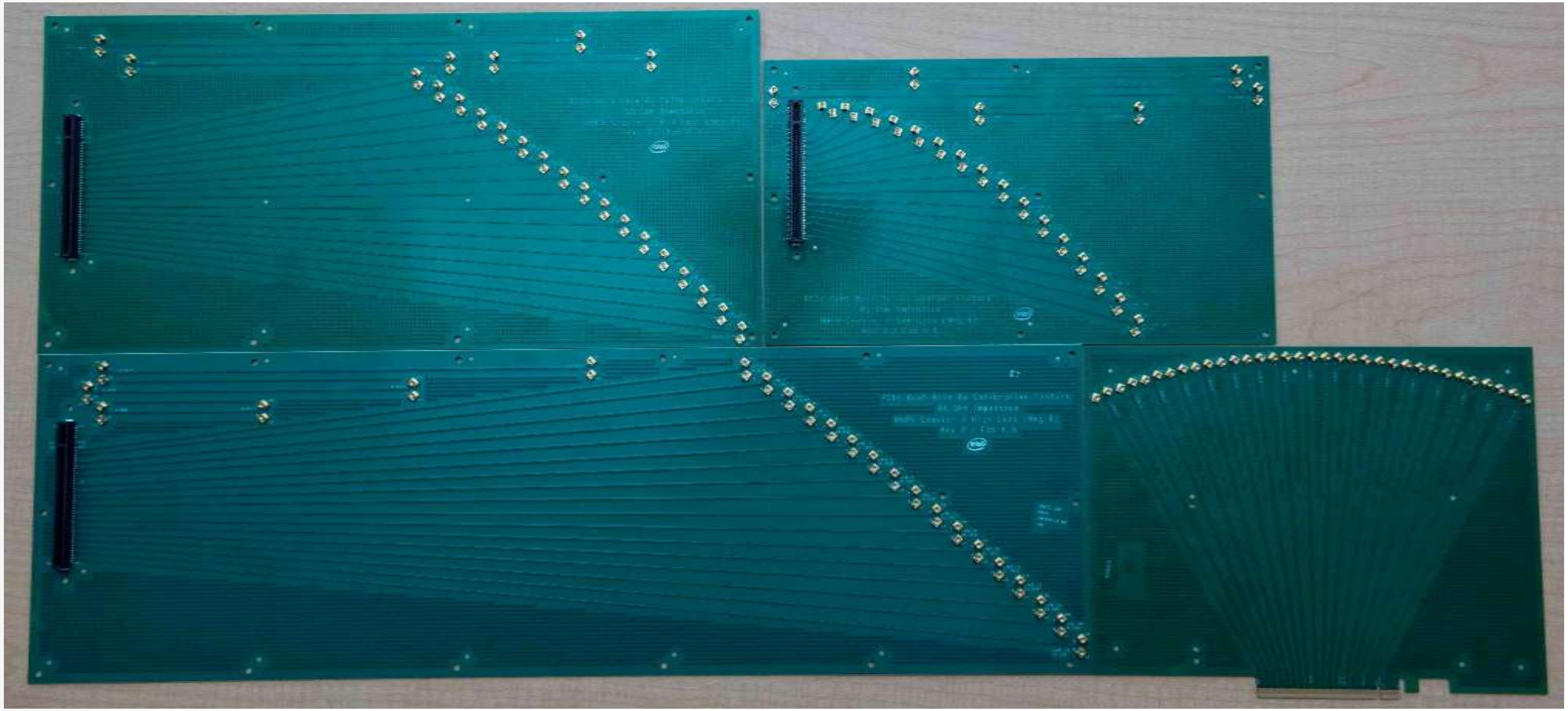
PCIE 4.0 CEM CLB/CBB SPREADSHEET

PCIe Gen4 Test Fixture Characterization			
		All cells with a bold outline must be filled in	
Insertion Loss Per Inch		**Notes**	**ypical Values**
Short Trace		Measured differential insertion loss (IL) on the CBB (J97/J99 <-> J96/J98) with SMA/SMP adaptors	1.110
Long Trace		Measured IL on the CBB (J74/J1 <-> J73/J2) with SMA/SMP adaptors	12.060
Loss/inch	0	(Long Trace IL – Short Trace IL) / 10	1.095
Coaxial Launch Loss			
SMA Female to SMP Female Cable		Adaptor cable loss can be measured, or obtained from data sheet	0.223
Coaxial Launch 2x	0	Long Trace Loss – 10" of loss/inch – loss of two adaptors = Loss of 2 coaxial launches	0.041
Mated CEM Connector Loss			
CBB Tx <-> CLB Rx		Measurement of CBB Tx Lane 0 with CLB Rx Lane 0 (CLB mated in CEM connector of CBB)	9.760
Mated CEM Connector Loss	0	Mated CEM Connector Loss = CBB & CLB Loss – SMA to SMP adaptor loss – trace loss – coaxial laun	1.609
CBB Tx Loss	0	CBB Tx Loss = Mated CEM Connector Loss + trace loss + coaxial launch	4.915
CLB Tx Loss	0	CLB Tx Loss = trace loss + coaxial launch	2.210
System Rx CAL		See "System Rx Calibration Diagrams" tab for measurement setups	
CBB ISI (Target)	15	Target loss for variable ISI board plus cables (SMP & SMA) on the CBB side	10.085
CBB ISI (Measured)		Variable ISI with cable measurement. Find variable ISI pair which gets the closest to "CBB ISI (Target)"	10.390
CBB ISI Pair		Identify the final variable ISI pair	Pair 16
27dB Channel (22 dB Measured)		Full channel channel measurement. Find variable ISI pair which gives a full channel measurement of 2	22.070
27dB CLB ISI Pair		Identify the final variable ISI pair	Pair 0
28dB Channel (23 dB Measured)		Full channel channel measurement. Find variable ISI pair which gives a full channel measurement of 2	23.020
28dB CLB ISI Pair		Identify the final variable ISI pair	Pair 2
30dB Channel (25 dB Measured)		Full channel channel measurement. Find variable ISI pair which gives a full channel measurement of 2	24.930
30dB CLB ISI Pair		Identify the final variable ISI pair	Pair 6
AIC Rx CAL		See "AIC Rx Calibration Diagrams" tab for measurement setups	
CLB ISI (Target)	5	Target loss for variable ISI board plus cables (SMP & SMA) on the CLB side	2.790
CLB ISI (Measured)		Variable ISI with cable measurement. Find variable ISI pair which gets the closest to "CLB ISI (Target)"	2.560
CLB ISI Pair		Identify the final variable ISI pair	Pair 0
27dB Channel (24 dB Measured)		Full channel channel measurement. Find variable ISI pair which gives a full channel measurement of 2	23.750
27dB CLB ISI Pair		Identify the final variable ISI pair	Pair 23
28dB Channel (25 dB Measured)		Full channel channel measurement. Find variable ISI pair which gives a full channel measurement of 2	24.850
28dB CLB ISI Pair		Identify the final variable ISI pair	Pair 25
30dB Channel (27 dB Measured)		Full channel channel measurement. Find variable ISI pair which gives a full channel measurement of 2	27.140
30dB CLB ISI Pair		Identify the final variable ISI pair	Pair 30
AIC Tx		See "AIC Tx Diagrams" tab for measurement setups	
CBB ISI (Target)	15	Target loss for variable ISI board plus cables (SMP & SMA) on the CBB side	10.085
CBB ISI (Measured)		Variable ISI with cable measurement. Find variable ISI pair which gets the closest to "CBB ISI (Target)"	10.390
CBB ISI Pair		Identify the final variable ISI pair	Pair 16
System Tx		See "System Tx Diagrams" tab for measurement setups	
CLB ISI (Target)	5	Target loss for variable ISI board plus cables (SMP & SMA) on the CLB side	2.790
CLB ISI (Measured)		Variable ISI with cable measurement. Find variable ISI pair which gets the closest to "CLB ISI (Target)"	2.560
CLB ISI Pair		Identify the final variable ISI pair	Pair 0

Four-port VNA for Channel Analysis

PCIe 5.0 ISI Channel

VERSION 3.0



Cables Provided in PCIe 5.0 BASE Fixture Kit

HUBER+SUHNER CABLES

PCISIG Supplied

0.9m H+S #85105115 2.92mm(M)-2.92mm(M)

24” H+S #85120962 MMPX(M)-MMPX(M)

4” H+S #85119609 MMPX(M)-MMPX(M)

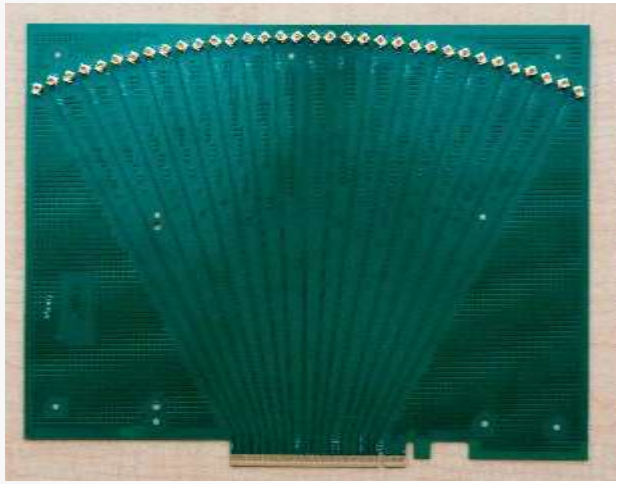
Suggested MMPX Accessories (not PCISIG Supplied)

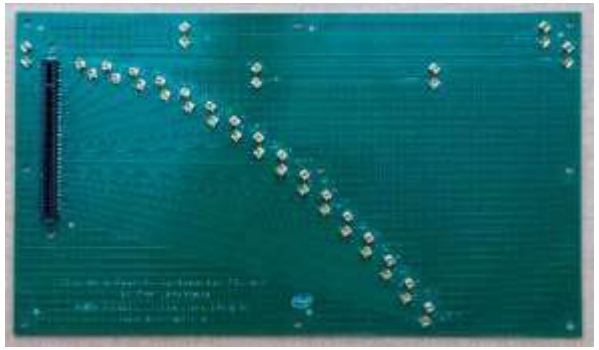
H+S #84071648 2.92mm(F) to MMPX (M)

H+S #84071696 2.92mm(M) to MMPX (F)

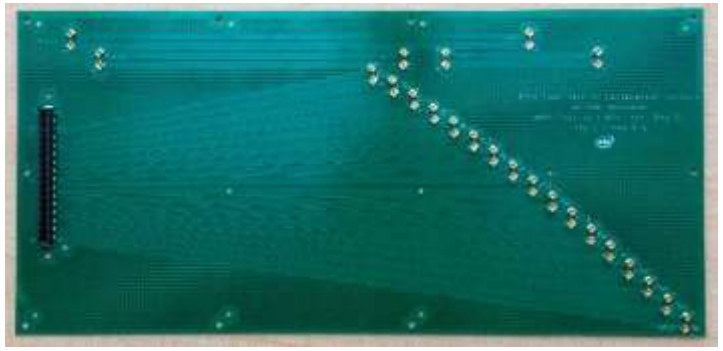
PCIe 5.0 BASE ISI Channel

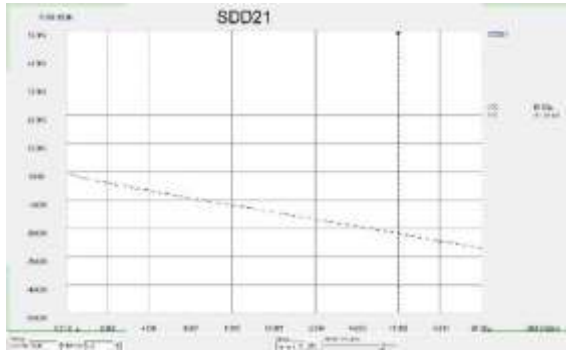
MAXIMUM CHANNEL LOSS PAIRS



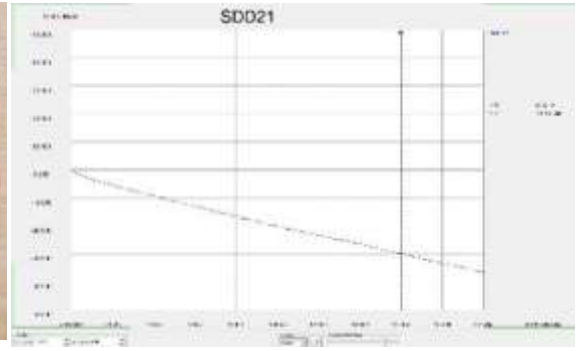


Loss of Pair 15 at 16GHz = -15.3dB





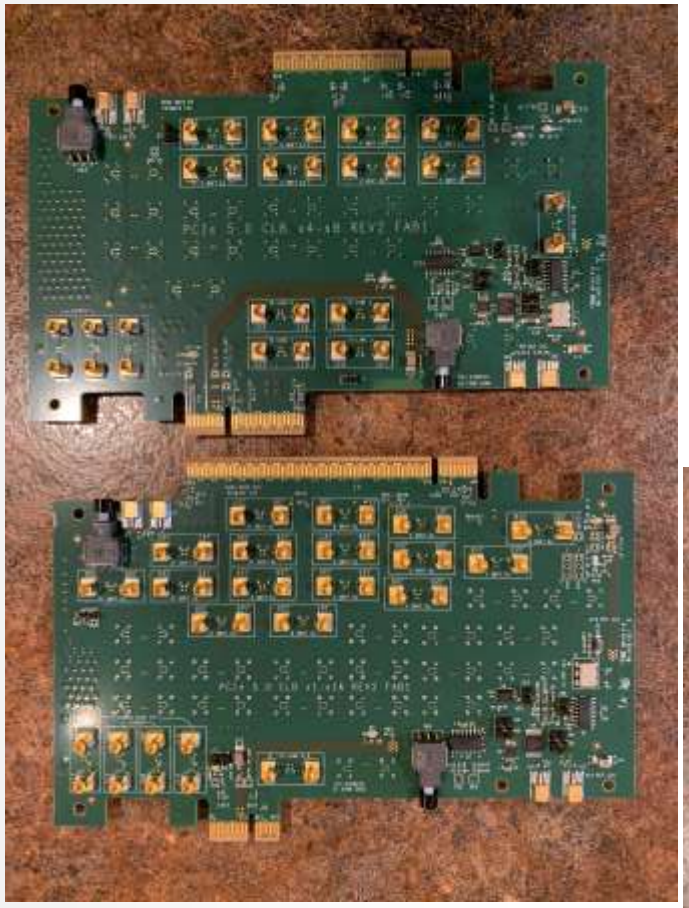
Loss of Pair 15 at 16GHz =-21.7dB

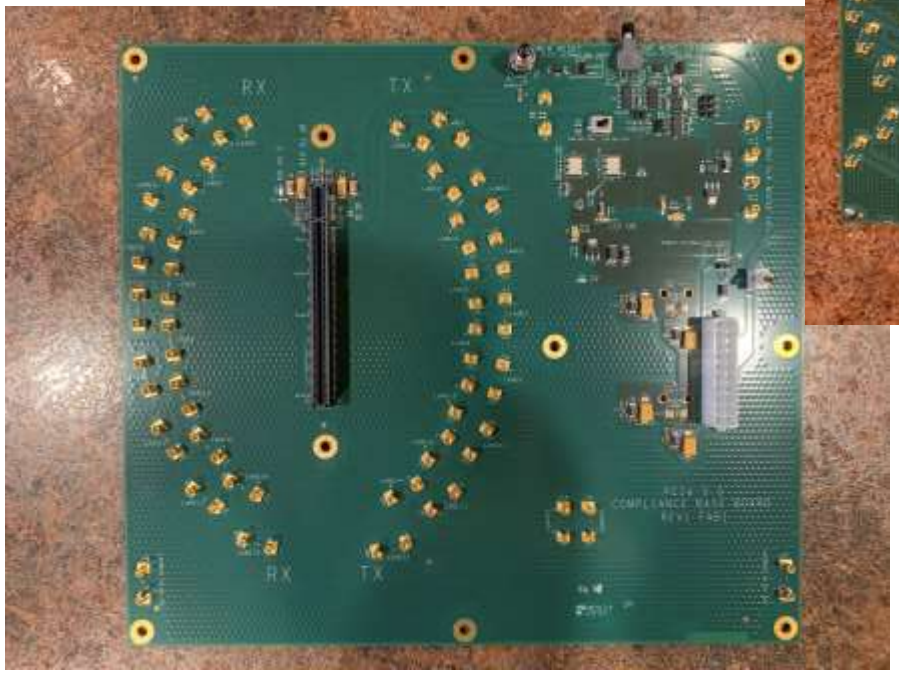


Loss of Pair 15 at 16GHz =-29.9dB

PCIe 5.0 CEM Fixture, Prototype

CLB, CBB AND ISI BOARD

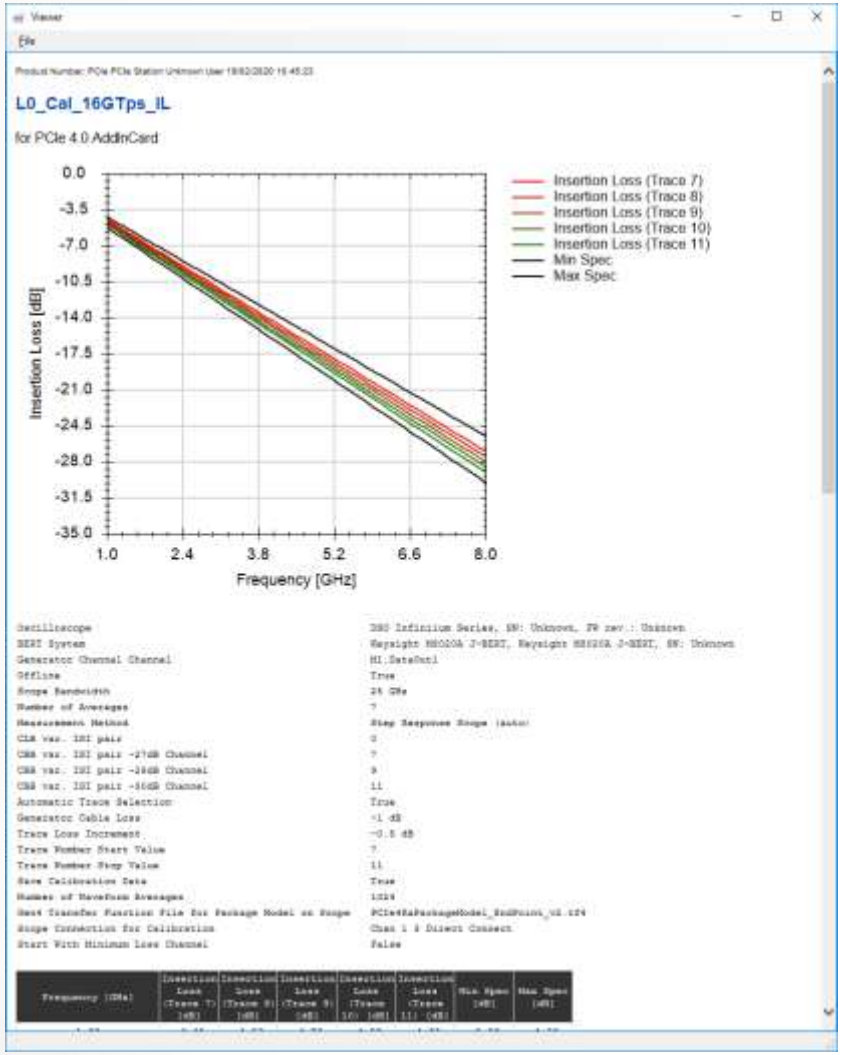


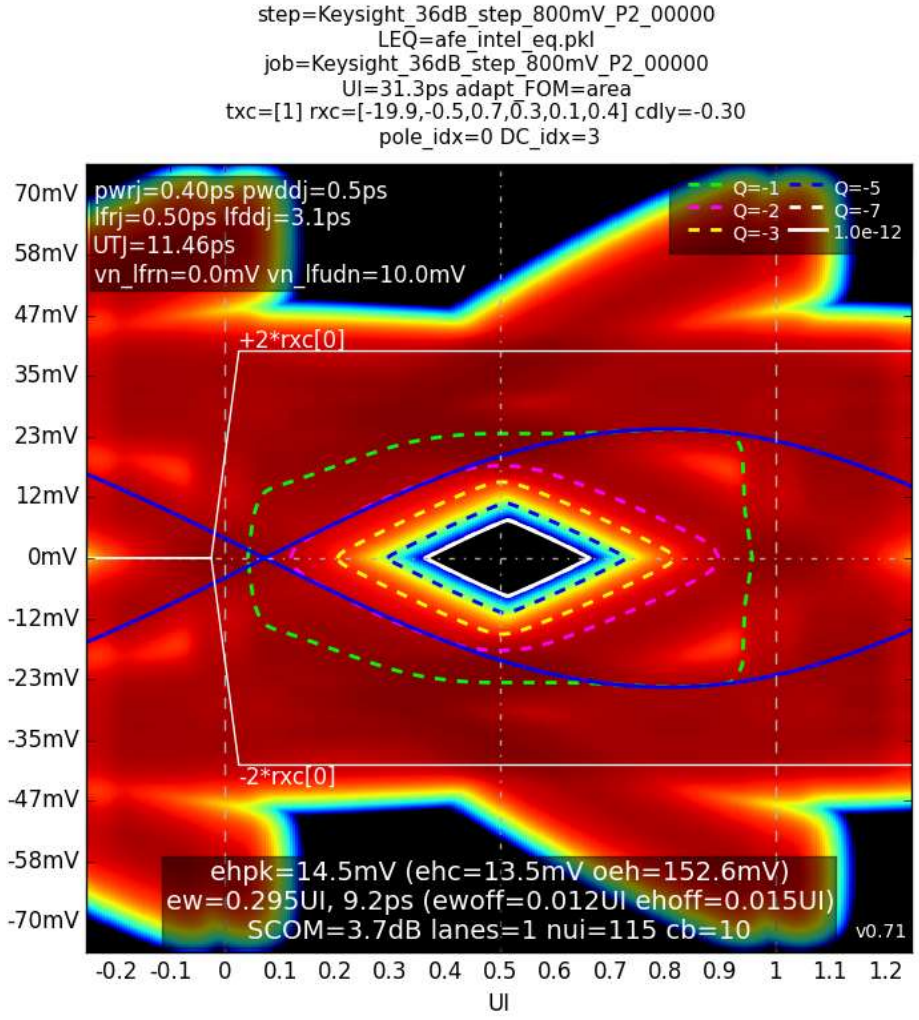


~$20K
Prototype, not final

Choosing the Right ISI Pair

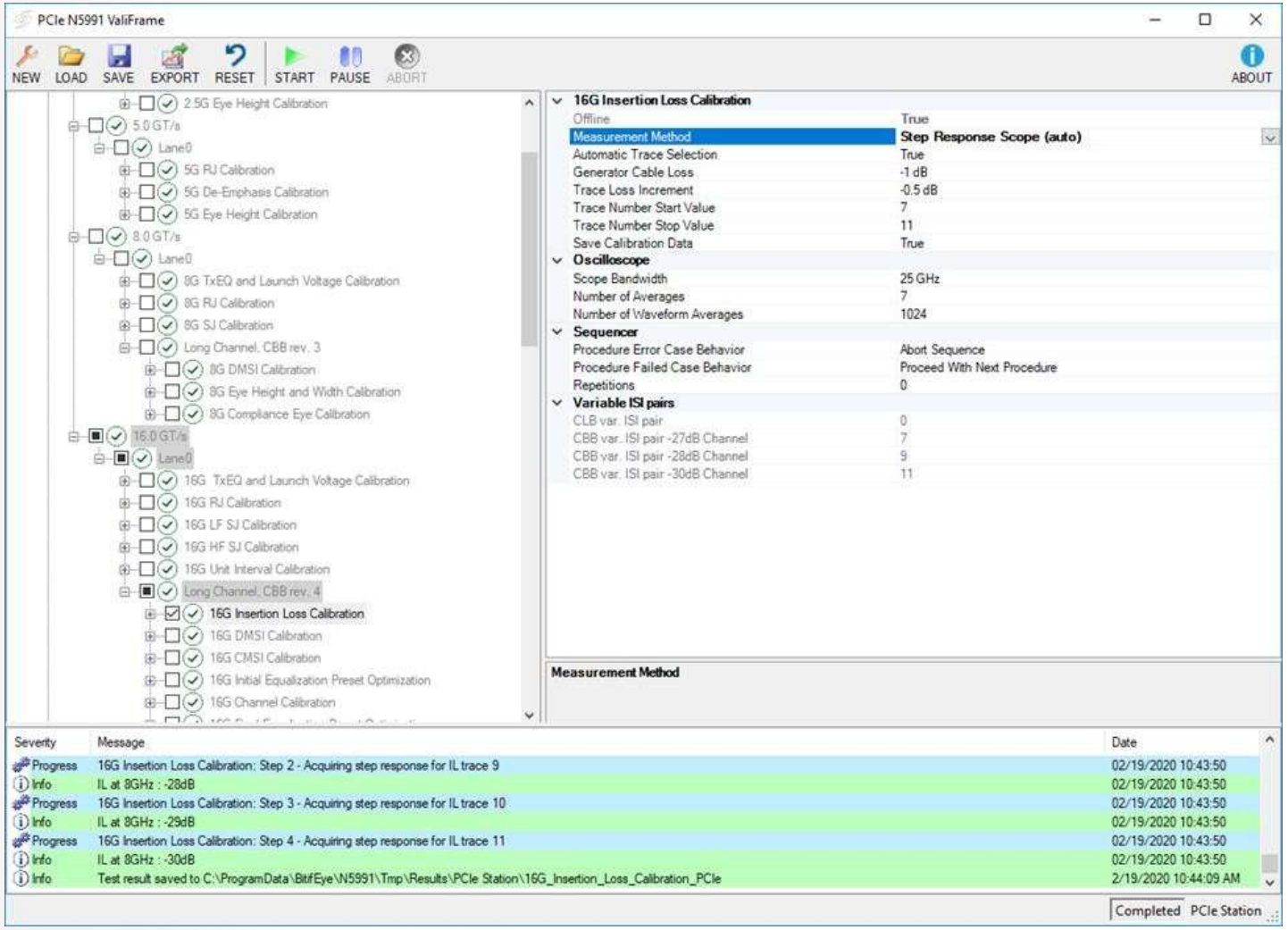
PCIE 5: PICK THE MAXIMUM LOSS CHANNEL

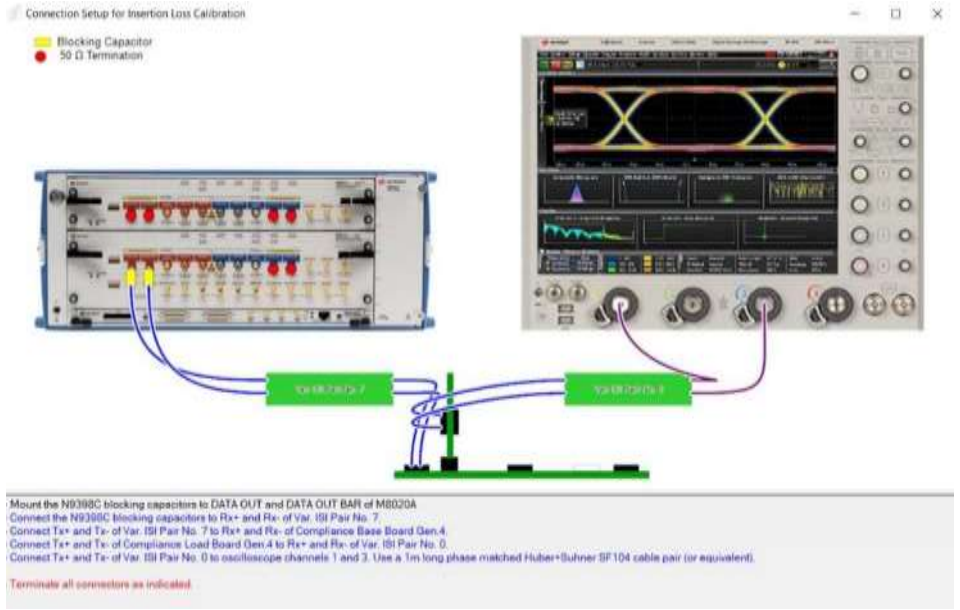




Choosing the right ISI Pair

STEP RESPONSE SUPPORTED PCIE 4 AND PCIE 5





Keysight Recommends the VNA Approach
For calculating ISI channel loss.

PCIe 5.0 TX Test Consideration & Tools

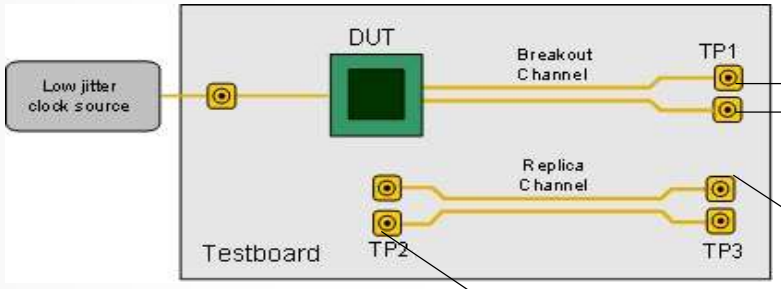
Base & CEM Scope Considerations

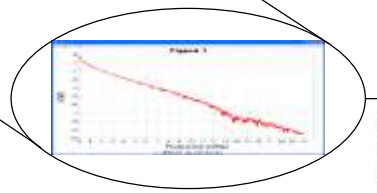
PCIe 5.0 32 GT/s Tx Testing

BREAK OUT CHANNEL FOR ASIC REQUIRED

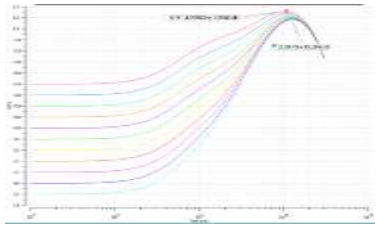
Keysight UXR-Series Real-Time Oscilloscope

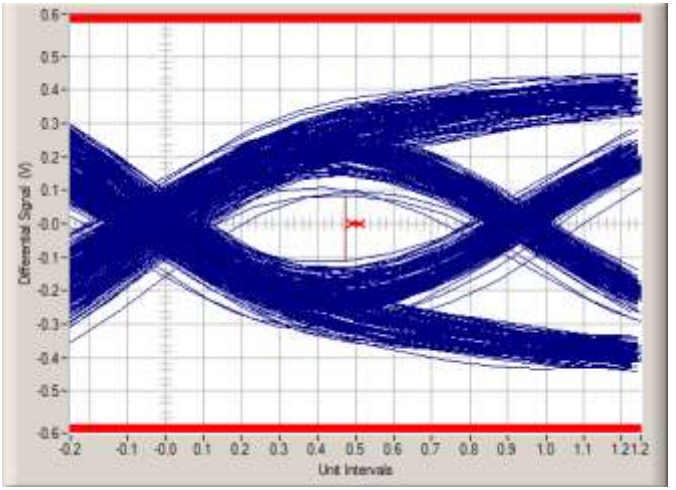
PCIe 5.0 ASIC/IC Custom
Breakout Board





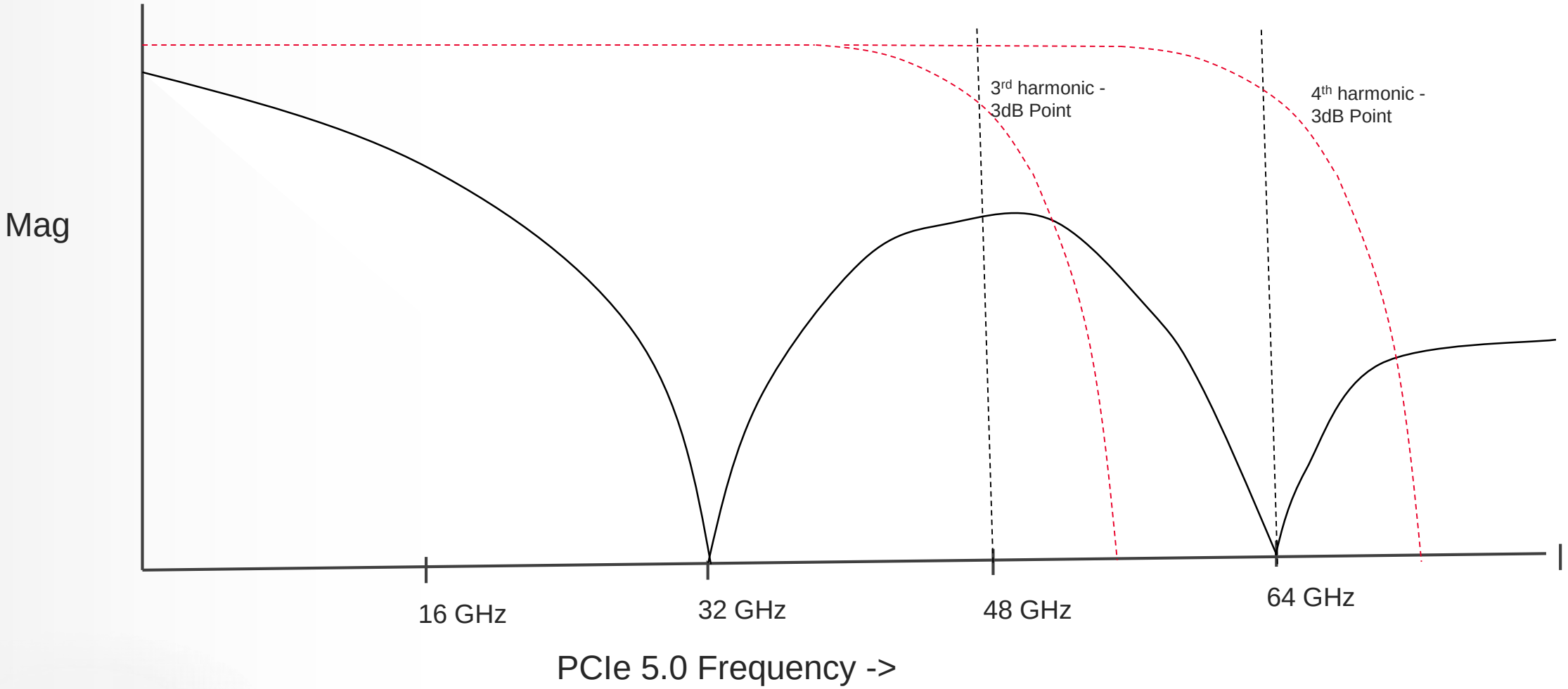
S-Parameters of Replica Ch.
Used to de-embed to pin or
Ref CTLE can be used (12dB).





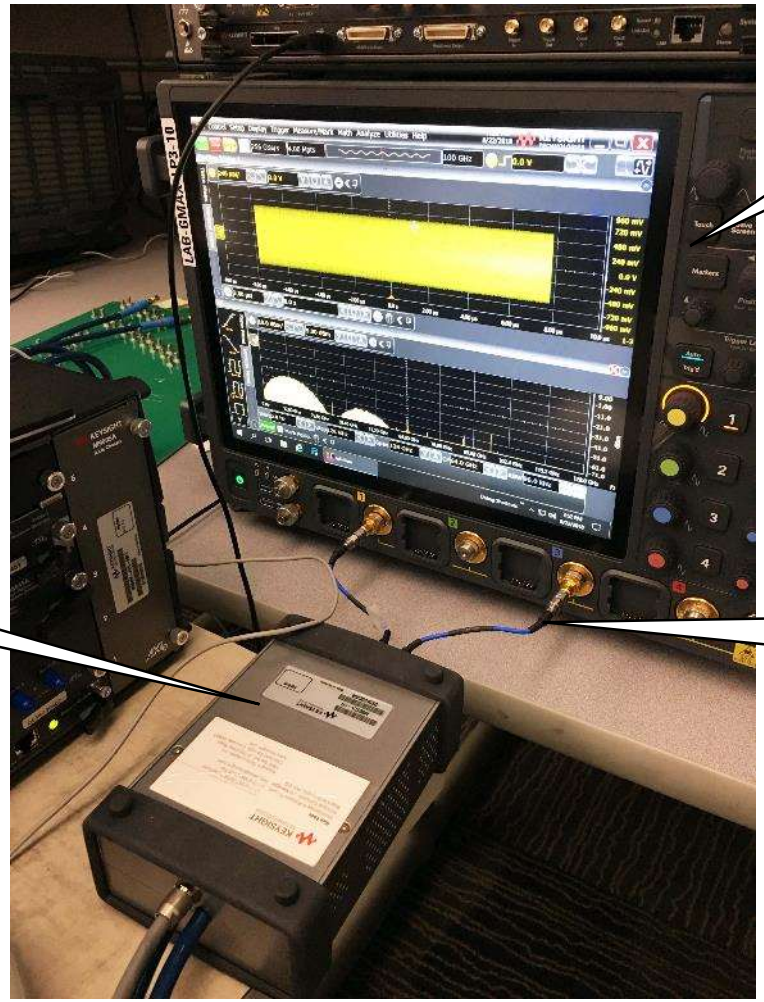
PCIe 5.0 Overview

PCI EXPRESS 5.0 HARMONICS



PCI Express 5.0 Spectral View

MEASUREMENT SETUP



UXR 110 GHz Scope
256 GSa/s

M8040A JBERT
800mV, 32 GT/s
P7

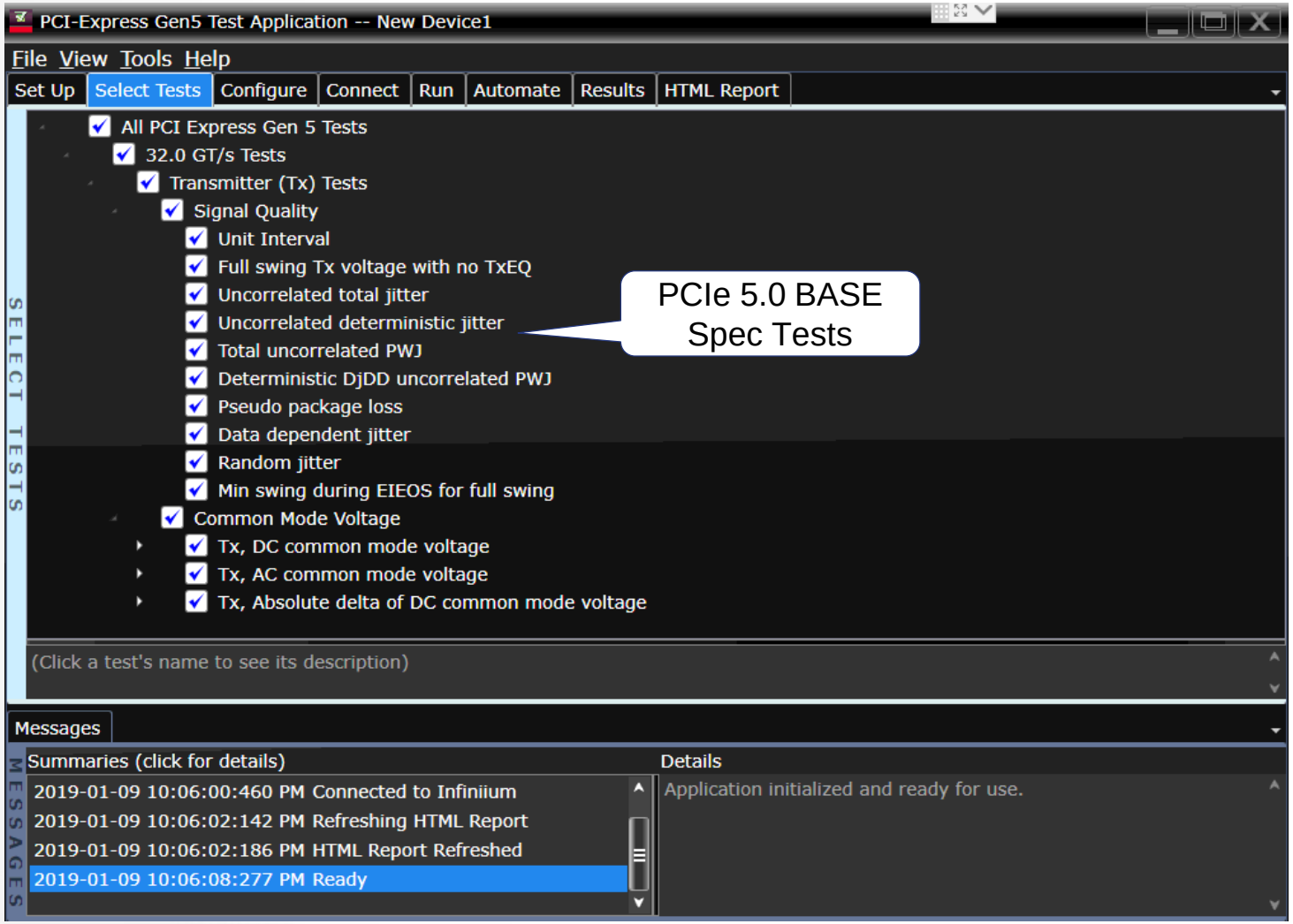
H&S 1.85mm
Connector/Cable
assembly

PCI Express 5.0 Spectral View

80 GHZ VIEW

Keysight D9050PCIC PCIe 5 (Gen5) Tx Test Application

5.0 BASE SPEC TESTS



Test Report

Overall Result: PASS

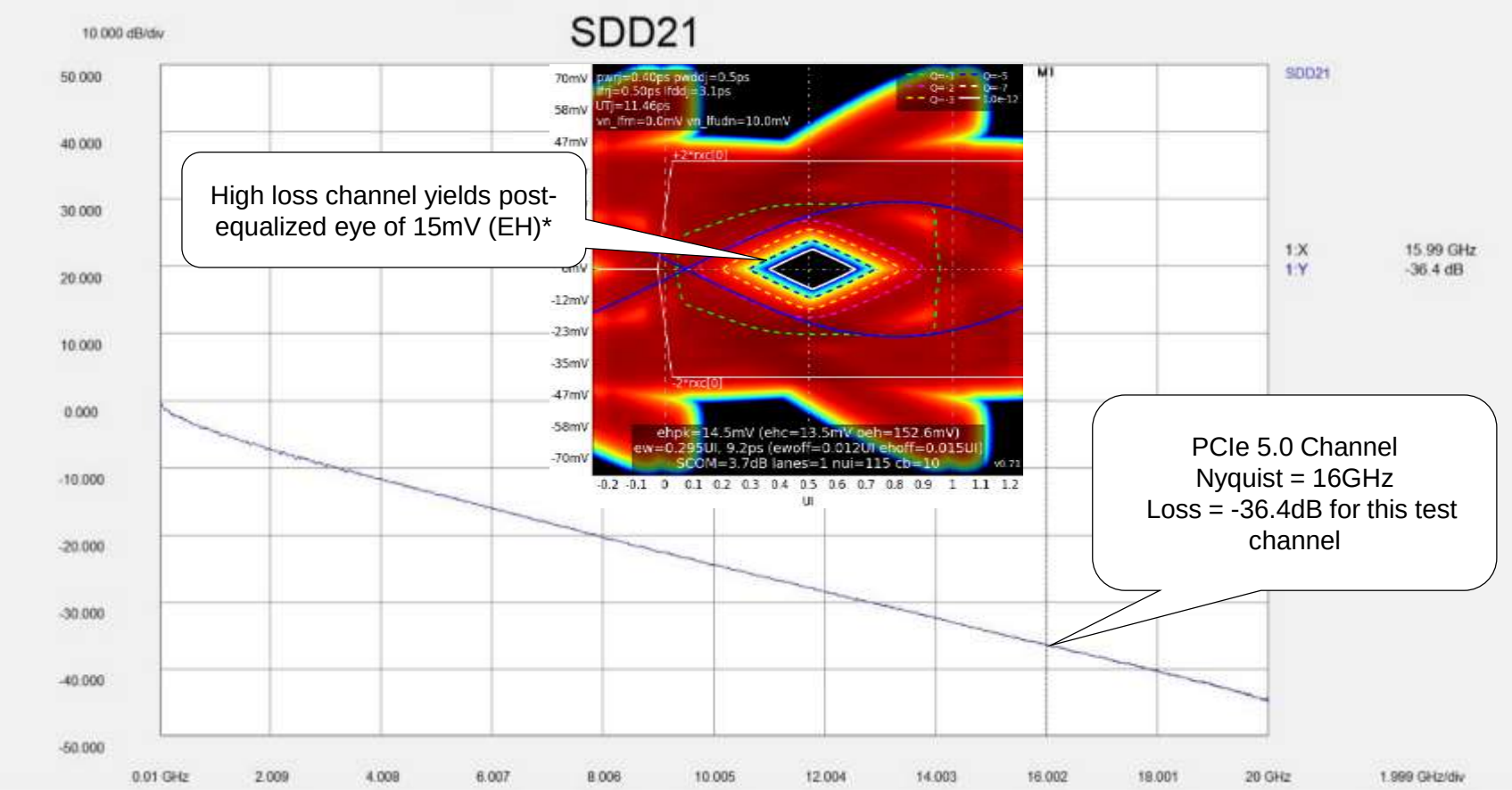
Test Configuration Details	
Device Description	
Data Channel +	ChannelR-1
Data Channel -	ChannelR-3
Device Name	New Device1
Test Session Details	
Infiniium SW Version	06.30.00701
Infiniium Model Number	DSAZ634A
Infiniium Serial Number	MY57220110
Application SW Version	0.99.9029.0
Debug Mode Used	No
Compliance Limits	PCI-Express Gen5 Test Application (official)
Last Test Date	2019-01-12 22:03:19 UTC -06:00

PCIe 5.0 BASE and CEM Scope Considerations

THE GREATER THE CHANNEL LOSS, THE GREATER THE BENEFIT DERIVED FROM LOW NOISE

UXR vs Z/V Series: PCIe 5.0 Channels

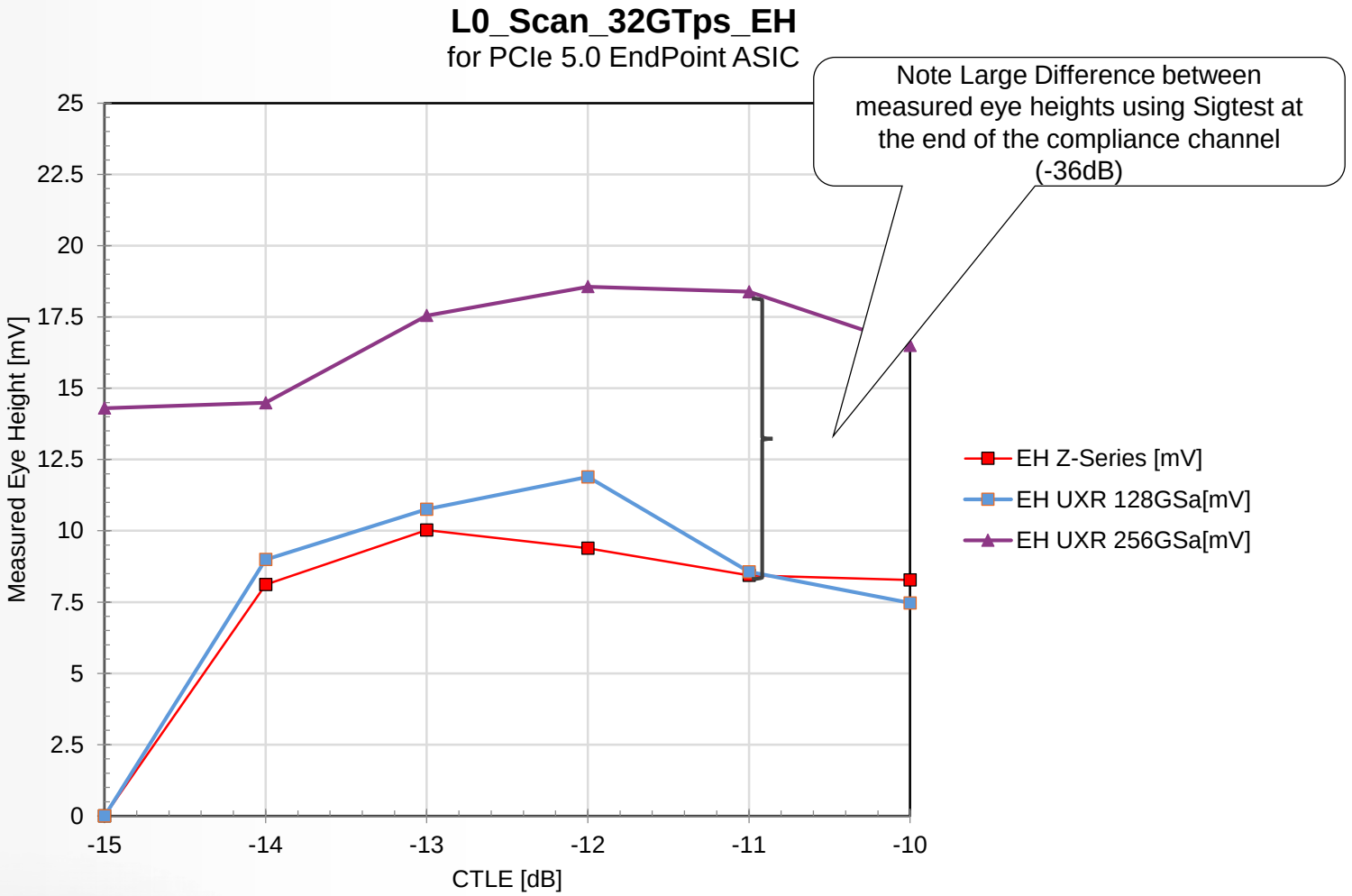
PCIE 5.0 CHANNELS ARE -36 DB TO -38 DB



* Based on statistical simulation using Seasim

UXR vs Z Series: End of Channel Results

NOISE FLOOR MATTERS: EYE HEIGHT* @ 32 GT/S



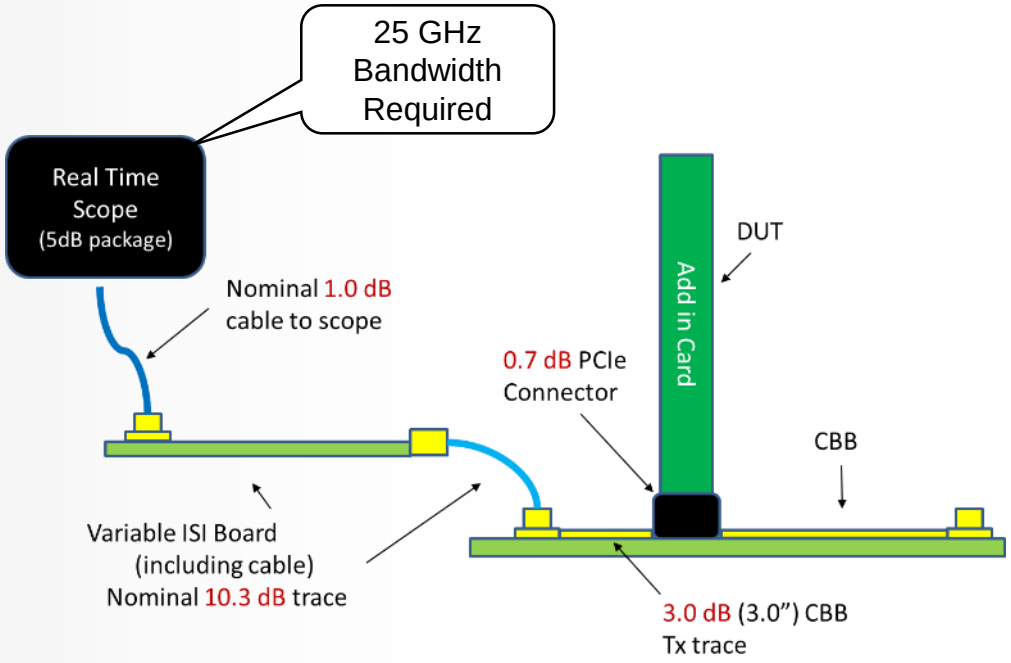
- Data Rate = 32 Gb/s
- Sigtest Composite Eye Height
  - 2M UI
  - CTLE -10 dB to -15 dB
- M8040A BERT
  - TX preset P5
  - Generator Launch =800 mV
  - DMSI=10 mV
  - CMSI=0 mV
  - RJ=0.5 ps
  - SJ=3.125 ps @ 100 MHz

* Based on waveform analysis using Sigtest

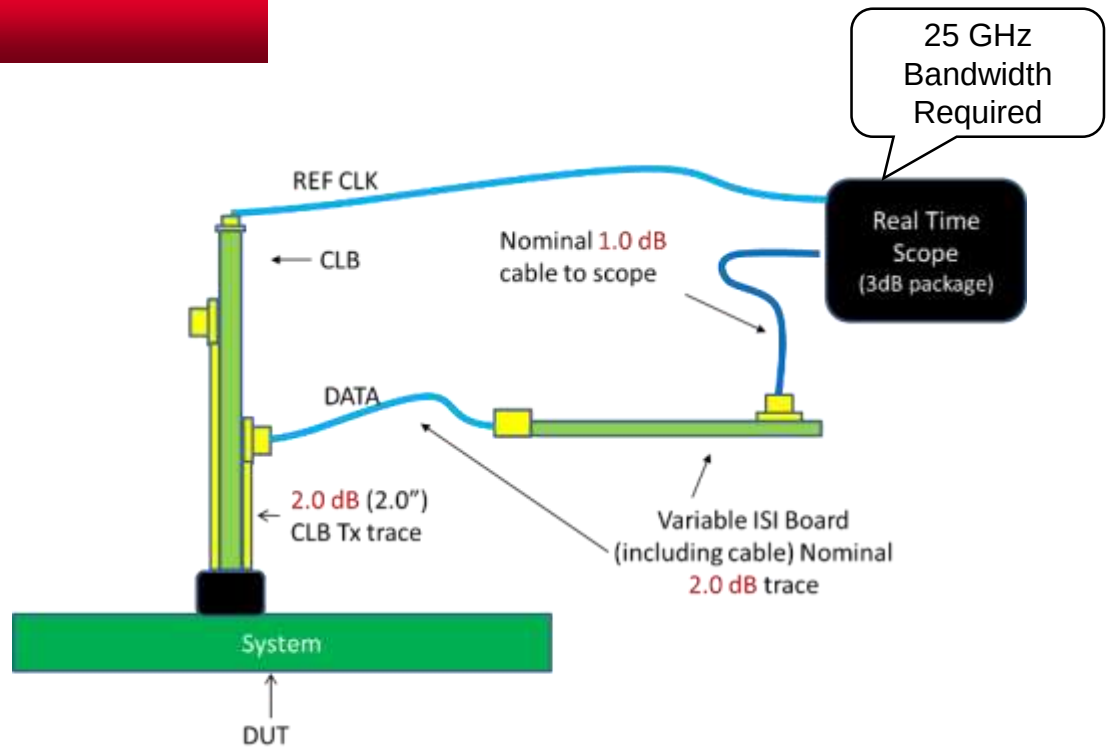
PCIe 4.0 CEM Dual Port Testing

PCIE 4.0 CEM Fixture Setup

PHY TX MEASUREMENTS



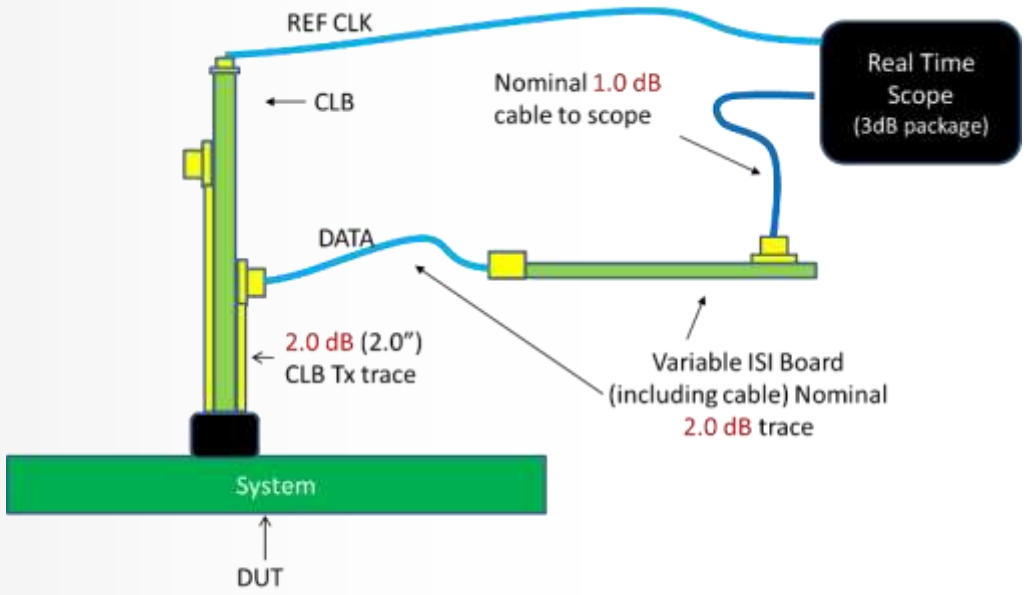
Add-in Card (end point)



System Board (root port)

PCIE 4.0 CEM Motherboard Tests

DUAL PORT TESTING IS THE REQUIRED METHOD



System Board (root port)

Appendix D. Alternate Method of System TX Signal Quality Test at 16GT/s

An alternate method of performing 16GT/s System Signal Quality test is provided in this note. The data and 100 MHz reference clock can be captured and post-processed separately. The data will be processed with SigTest using the 16GT/s Add-in Card Signal Quality template file (PCIe_4_16G_CEM.dat). The pass/fail limits for Eye Width at 1E-12 and Eye Height at 1E-12 will remain unchanged for 16 GT/s System Signal Quality Test. The reference clock will be post-processed with a separate clock tool to ensure the Random Jitter is less than or equal to 0.7 ps RMS as defined in the *PCI Express Base Specification*.

The signal quality test described in Section 2.7.5 is the required test method for System Tx Signal Quality testing at 16 GT/s. This alternate method is only to be used when the signal quality test described in Section 2.7.5 fails.

2.7.5 System Board Transmitter Electrical Compliance Test for 16.0 GT/s

1. Connect the Tx lane under test …

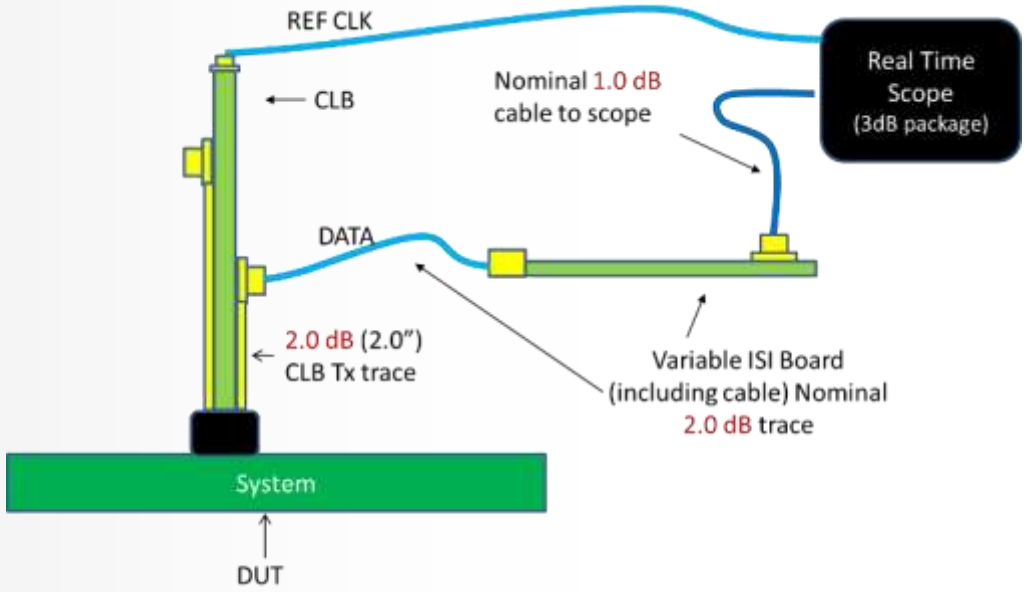
2. Connect the Reference Clock (REF CLK) on the CLB to a high-speed oscilloscope …

3. …push the compliance toggle button on the CLB until the correct Tx EQ is selected…

4. Measure transmitted clock and data waveforms simultaneously with a high-speed oscilloscope or equivalent data capture instrument with the maximum bandwidth set to 25GHz

PCIE 4.0 CEM Motherboard Tests

WHY HAVE TWO METHODS?



System Board (root port)

- Dual Port uses both clock and data and represents the AIC view of root port signal quality.
- System board vendors can trade off ref clock jitter for better TX jitter and still be compliant.
- For PCIe 5.0, Dual-Port test method for motherboards to be reconsidered.

PCIe 6.0 64GT/s Pathfinding

PCIe 5.0 to 6.0: From NRZ to PAM4

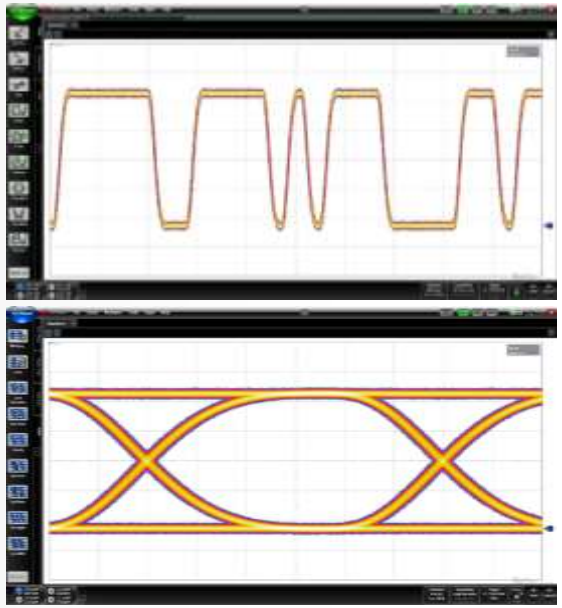
PCIe 6.0 Goals

WHAT MIGHT PCIE 6.0 LOOK LIKE?

PCIe 6.0 Category	Objective
Data Rate	64 GT/s, PAM4 (2x Gen5)
Latency	Low Latency FEC
Key Applications	800G Ethernet, AI, Co-Processors, Accelerators
Reliability	As good as Gen5
Channel reach	-36 dB at 16 GHz (Gen5 Channel)
Power Efficiency	As good as Gen5
Low Power	Keeps L1 sub state
Plug n Play	Backward compatibility w/ Gen1-5 (Form Factors for CEM, M.2, Other?)
Other wants for Gen6	Not cost prohibitive to implement (HVM). Testable. Simple
Spec Completion	2 years to develop and consense

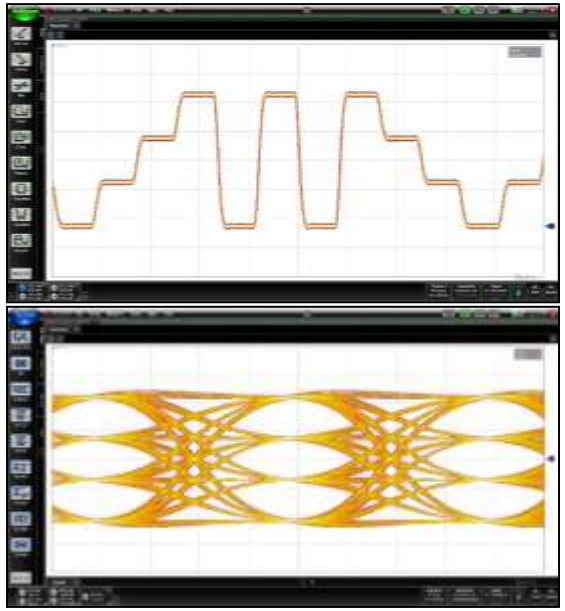
NRZ (Non-Return-to-Zero) vs. PAM (Pulse Amplitude Modulation)

NRZ (PAM2)



- 2 amplitude levels
- 1 bit of information in every symbol
  - ✓ 32 GBd NRZ = 32 Gb/s
  - ✓ PCIe 1,2,3,4,5 = NRZ

PAM4



- 4 amplitude levels
- 2 bits of information in every symbol
  - ✓ ~ 2x throughput for the same Baud rate (FEC required)
  - ✓ 32 Gbaud PAM4 = 64 Gb/s
- Lower SNR, more susceptible to noise, loss, and reflections
- More complex TX/RX design, higher cost
- Nyquist frequency = 0.5*baud rate
  - PCIe 5.0 Nyquist Frequency = PCIe 6.0 Nyquist

Why Does PCIe 6.0 Need PAM4?

ENABLES HIGHER DATA THROUGHPUT

- NRZ rates > 32 Gb/s
  - Limited channel reach unless channel BW is increased (and reflections/xtalk are properly managed)
  - Increasing (e.g. doubling) channel BW increases cost
- PAM4 yields 2 bits / symbol
  - ✓ Effectively halves the channel BW needs vs NRZ
- Allows designers to develop products to fit the cost structure of available channel technologies.

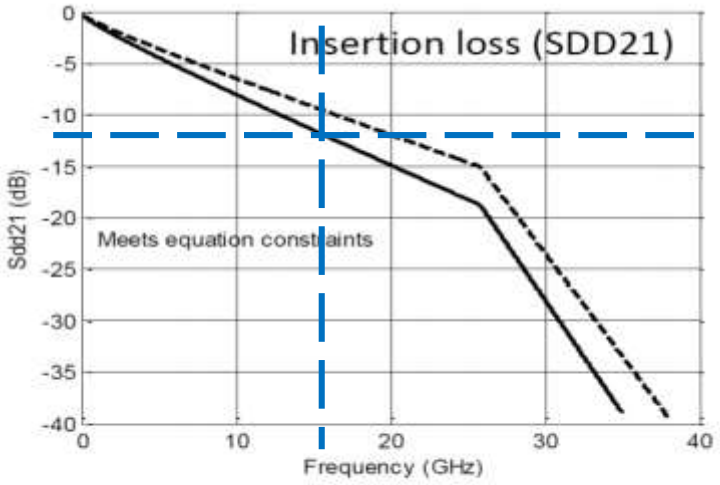
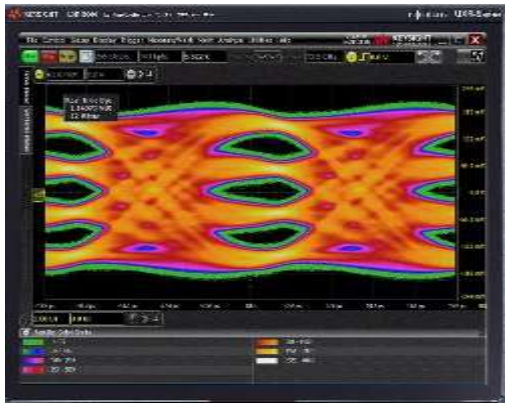
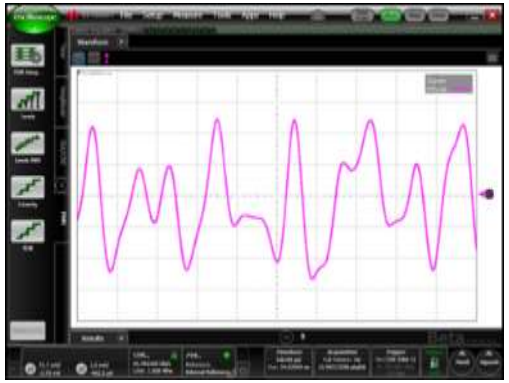


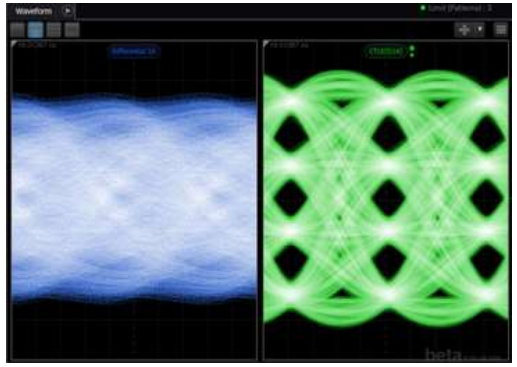
Figure 5: CEI-56G VSR NRZ channel

Clock Recovery for PAM4 Designs

- Clock recovery (CR)
  - Recovers a clock for the Rx to use in real systems
  - Standards require scopes to emulate most basic CR used in real Rx (track out low-frequency jitter, trigger the scope)
- PAM4 adds complexity
  - Transitions no longer only at 0V diff
  - CR Loop BW reduced from 10 MHz to ~ 4 MHz (IEEE 802.3bs/cd and CEI-56G-PAM4, same for proposed “112G” standards)
  - 1st Order PLL (no peaking, 20 dB/decade roll-off)
- Instrument clock recovery
  - Real-time oscilloscopes use software CR
  - Equivalent-time oscilloscopes (aka Sampling scopes) use hardware CR
  - CR needs to be able to lock onto “closed eyes”



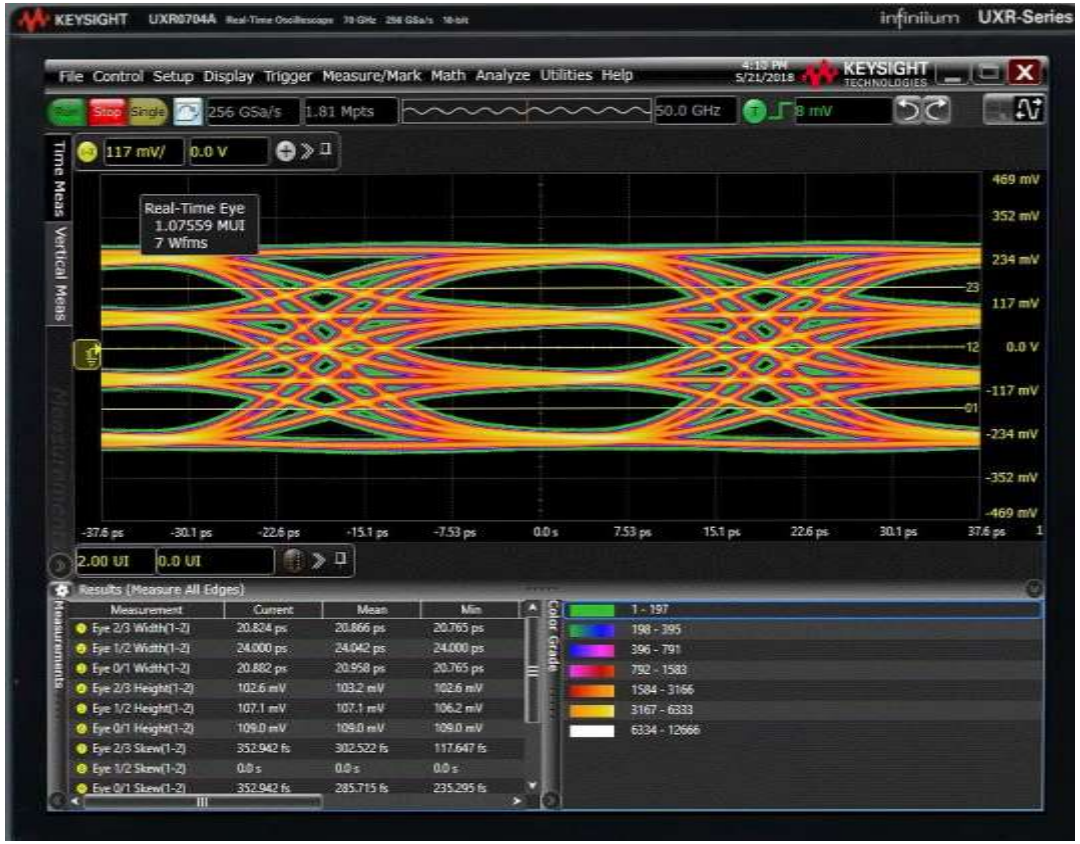




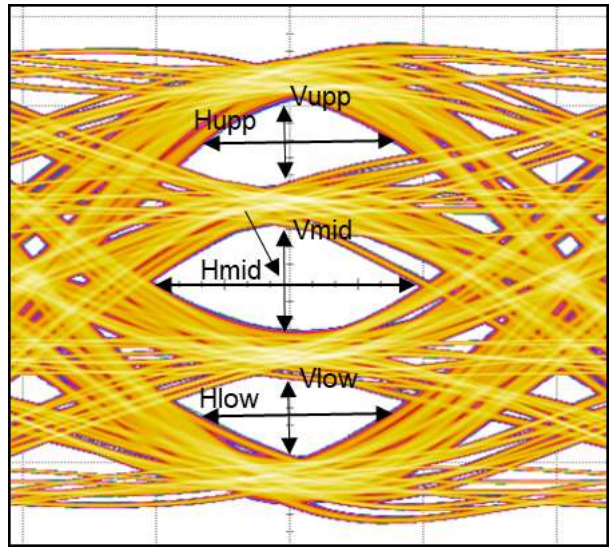
New Tx and Rx Measurements for PAM4

- Multiple eye width & eye height computations
- Eye symmetry mask width (ESMW)
- Transmitter linearity
- Tx output jitter
  - JRMS
  - J3u, J4u
  - Even-Odd Jitter (EOJ)

measured very differently compared to legacy NRZ signals

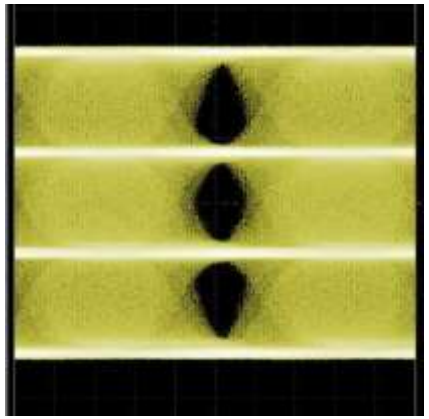


PCIe 6 & Spread Spectrum Clocks (SSC)

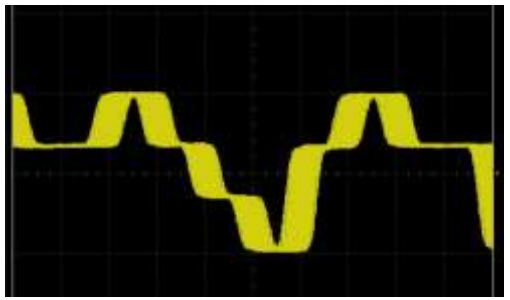


- PAM4 signals carry significant DDJ even **without** SSC
  (4 levels, 12 different transitions)

- PAM4 with SSC has not yet been implemented at these baud rates in other stds.



- SSC effects for PCIe 6.0 require further study
  - If SSC is not adequately tracked out, additional eye closure will occur (degrading link SER performance)
  - If a different CR model (BW, loop order) is required compared to IEEE/CEI (4 MHz, 20 dB/decade), how will it impact signals?
  - Need very tightly controlled CR loop bandwidths
  - Reduce max SSC deviation %?
  - Is SSC still required at these rates?



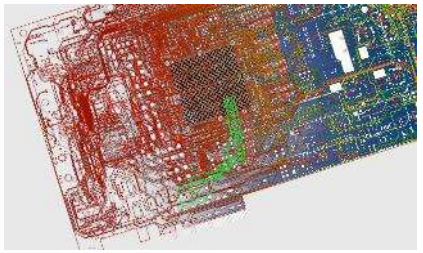
Measurement Challenges for PCIe 6.0

- What can be leveraged from test parameters and test methods developed for PAM-4 Signals established to-date by IEEE and OIF-CEI
- Choice of CDR model may be critical (higher PLL BW and Peaking could cause difficulty)
- Ensuring that measurements are performed at test points that have been equalized to achieve an open eye may be necessary
- SSC (Spread Spectrum Clocking) adds another layer of complexity
- FEC Performance and Native BER will be critical

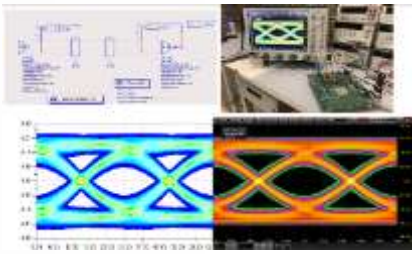
PCI Express® 6.0 – Keysight Total Solution

Physical Layer – System Simulation

ADS Design Software



SIPro/PIPro



Simulation to Measurement Correlation

Complete System Simulation
From Pre-layout analysis to Post-layout extraction

Physical layer – interconnect design

ADS design software

86100D DCA-X/TDR

N5227B PNA w/ PLTS

Verify PCIe 5.0 Compliant Channels
Verify Return Loss Compliance
Capture break-out channel S-Params

Physical layer-transmitter test

UXR-Series, Z-Series Real-Time Oscilloscopes

D9050PCIC PCI Express 5.0 TX Electrical compliance software

86100CU-400 PLL and Jitter Spectrum Measurement SW

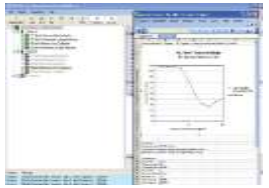
DSA UXR-Series & Z-Series Real-Time Oscilloscopes

Physical layer-receiver test

M8046A J-BERT High Performance BERT w/ integrated CDR + M80454A Interference Source

M8049A-1 Substitute PCIe 5 BASE Channel board

N5991PB5A
PCIe 5.0 32GT/s RX Test software



Automated RX Test software
- Accurate, Efficient
- Comprehensive RX Testing


KEYSIGHT
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