KEYSIGHT WORLD 2019

# SERDES and Memory Design on High Performance Computing

*Application Engineer / Keysight Technologies*

*Nash TU*

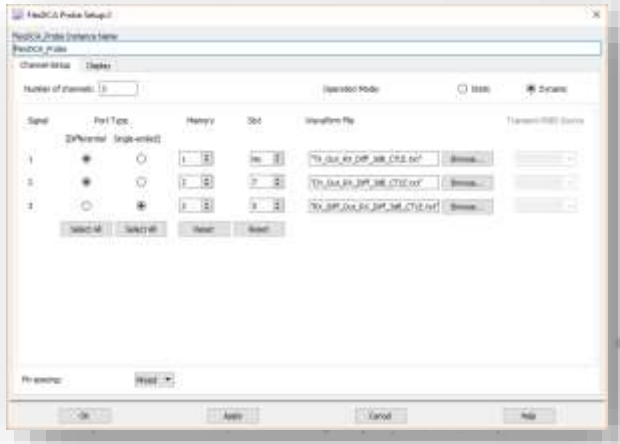
# ADS To FlexDCA Flow

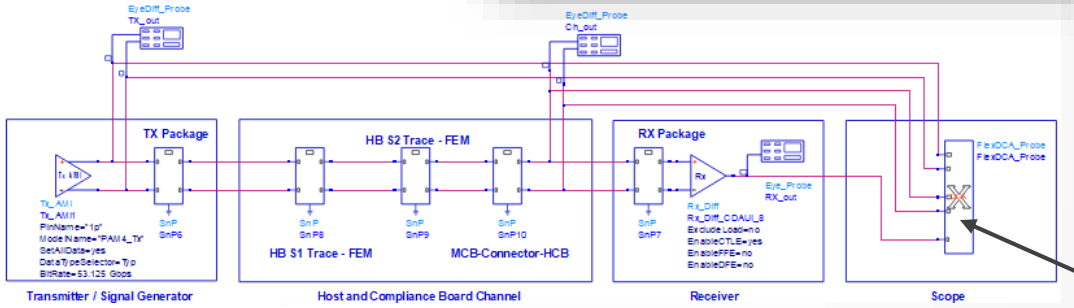
## CONNECTING SIMULATION AND MEASUREMENT DOMAINS

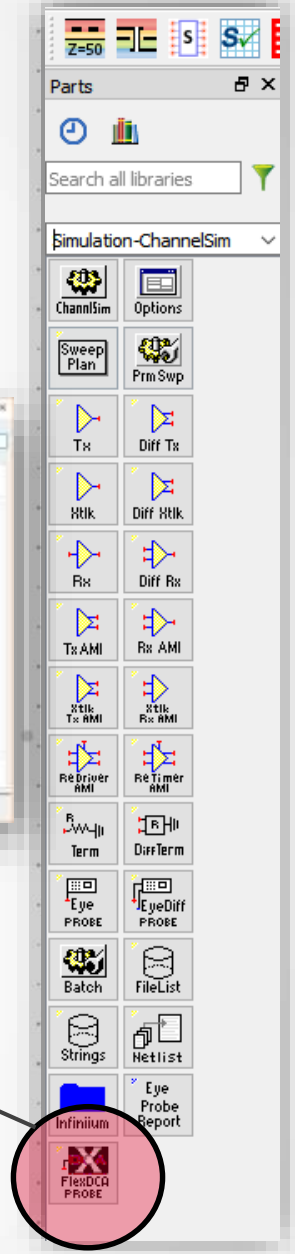
- FlexDCA_Probe connects ADS to FlexDCA (DCA software) - automatic invocation of FlexDCA
- FlexDCA_Probe unlocks comprehensive built-in PAM4 measurements, Jitter Analysis, DSP, and Math capabilities in FlexDCA to the waveforms from ADS
- Automatically populate the signal type such as PAM4 and NRZ as well as UI for FlexDCA
- Measured vs. simulated can be compared on the same software platform using FlexDCA
- Supports 8 memory and 8 slot channels
- Supports “Static” and “Dynamic” access methods

**DCA Scope**

**FlexDCA_Probe Dialog**





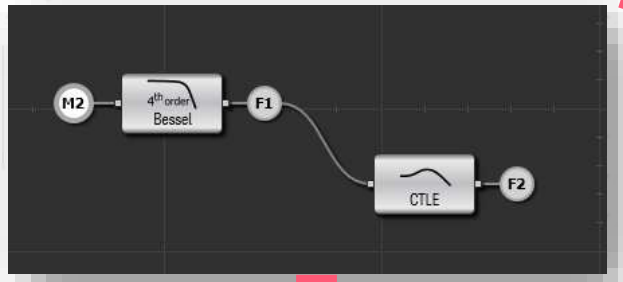

**FlexDCA_Probe**

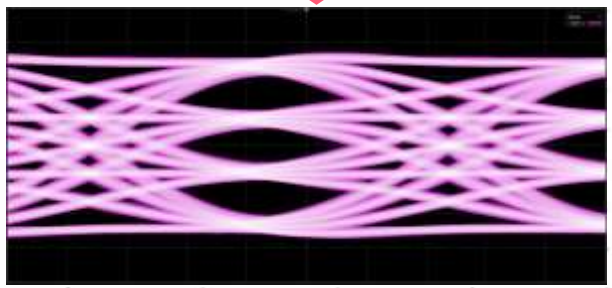
# Unlock Built-In Comprehensive FlexDCA PAM4 Analysis

## PAM4, JITTER, COMPLIANCE APPS

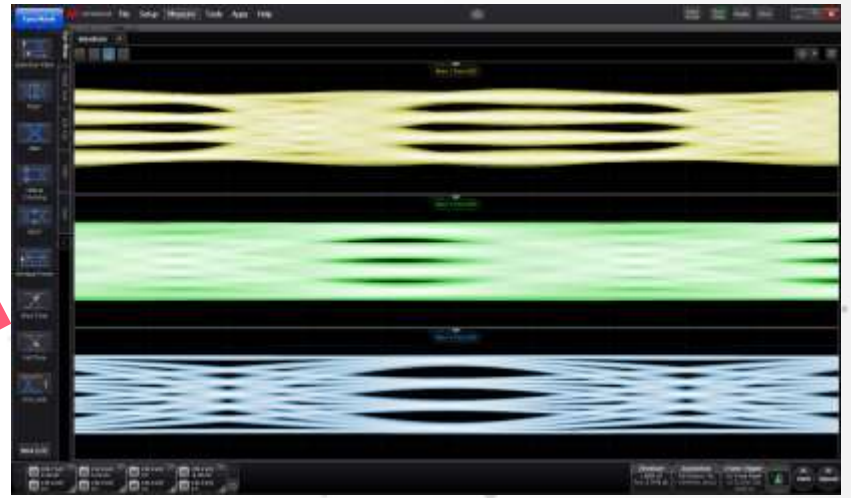
- ADS starts FlexDCA automatically
- Unlock all built-in comprehensive PAM4 analysis in FlexDCA
  - Eye contour
  - TDECQ (Transmitter Dispersion Eye Closure Quaternary)
  - Outer OMA
  - Linearity
  - Noise Margin
  - Partial SER
  - Partial TDECQ
  - Levels, Level Skews
  - Eye Skews, Height, and Width..
- Jitter Analysis
- Run Compliance Apps


**Math and DSP in FlexDCA**



**ADS Waveforms in FlexDCA**



**Jitter Analysis**

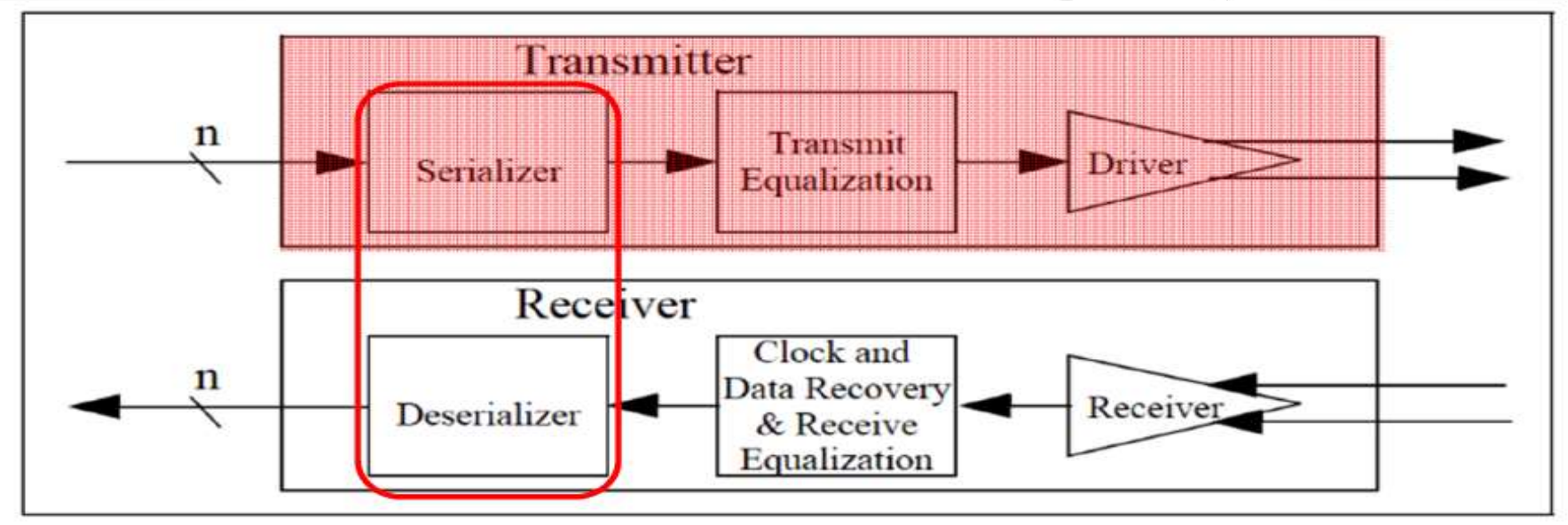
# SERDES vs DDR

| | SERDES | DDR |
|---|---|---|
| **Application** | PCIE, SATA, USB3… | DDR3, DDR4… |
| **Topology** | Point to Point | Point to Point, T Branch, Fly-By |
| **Signal** | Differential Pair | Differential Pair, Single-Ended |
| **Termination** | Fixed | Variable |
| **Channel Length** | Long | Short |
| **Coding** | Yes | No |
| **Equalizer** | Yes | No |
| **Clock** | Embedded | Outside |
| **SSN** | Weak | Strong |

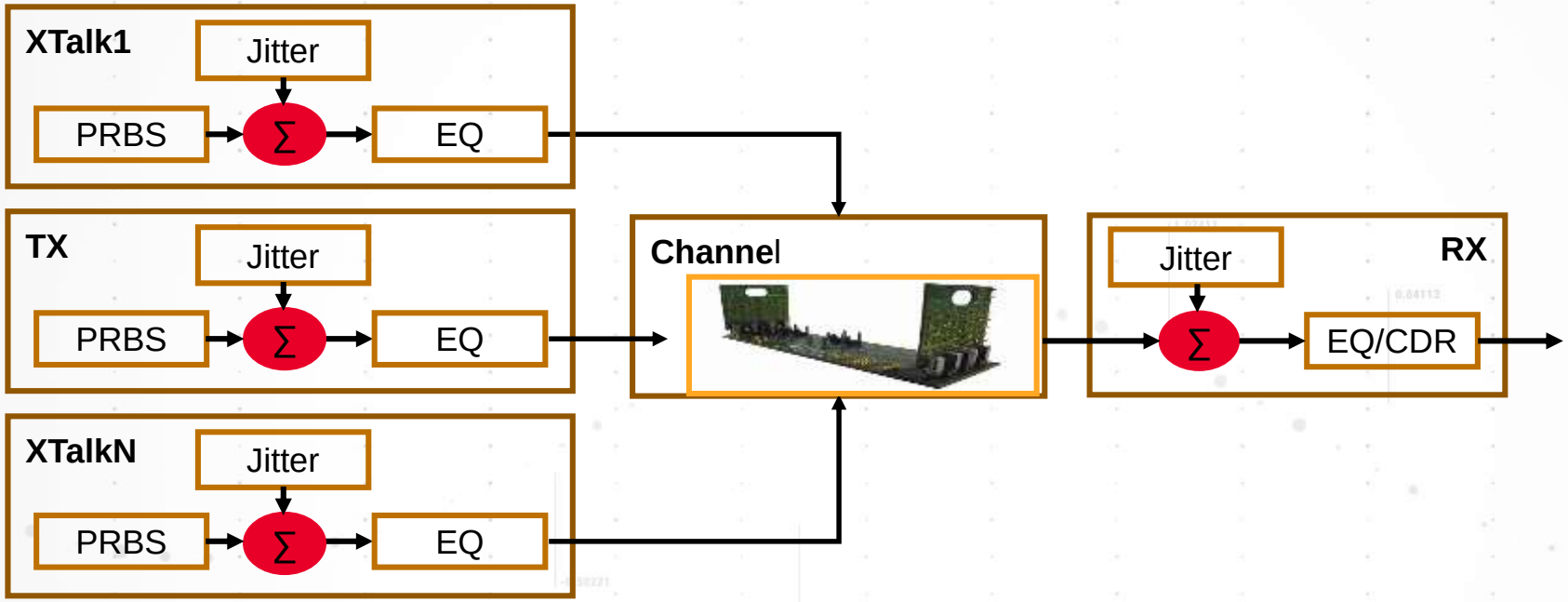
# What is SERDES ?

SERDES = SERializer - DESerializer

- Used to transmit high speed I/O data over a serial link in I/O interfaces
- SerDes TX: convert parallel data to series data and transmit to high speed link
- SerDes RX: receive data from serial link and deliver parallel data to next stage



# SERDES Link Introduction and Design Challenges




- Low BER performance (10e-12 or less)  used to imply long simulations
- Issues with interconnect models: limited frequency domains model leads to causal issue
- Multiple crosstalk channels
- Jitter modeling for TX &RX
- Equalization in TX &RX

# Tx & Rx Equalizer

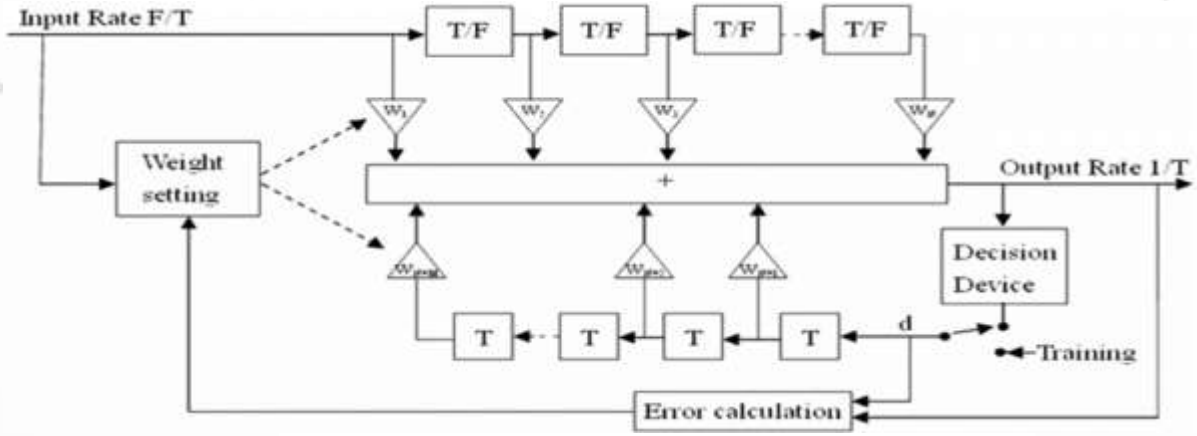
- **Feed-forward-equalizer (FFE)**

$$V_{out}(t) = a_0 V_{in}(t) + a_1 V_{in}(t-T) + a_2 V_{in}(t-2T) + \cdots$$

- **Continue-time-equalizer (CTE): pole-zero**

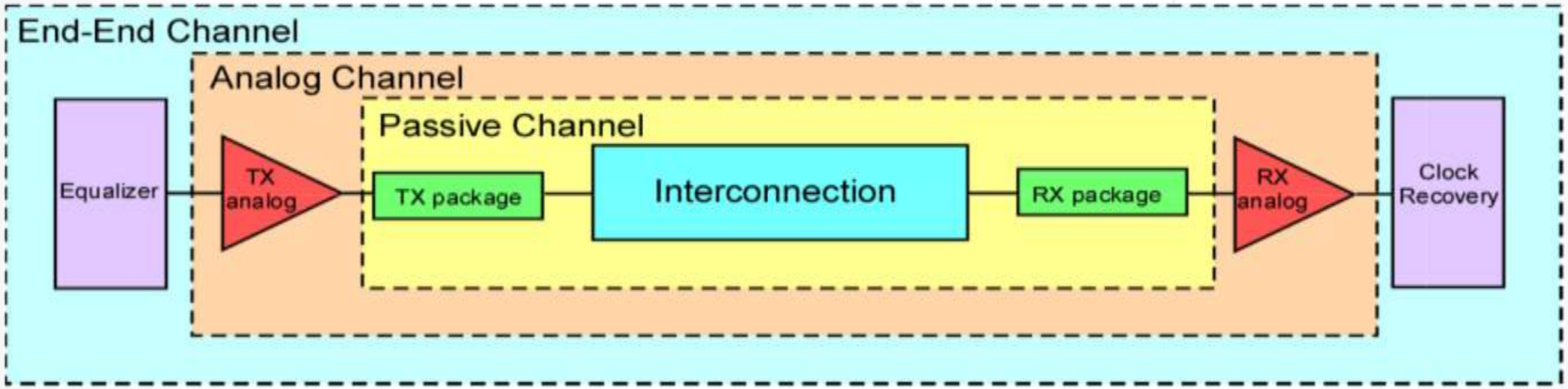
$$H(s) = A\frac{(s-z_1)(s-z_2)\cdots}{(s-p_1)(s-p_1)\cdots}$$

- **Decision-Feedback-equalizer**



# What is IBIS and AMI?

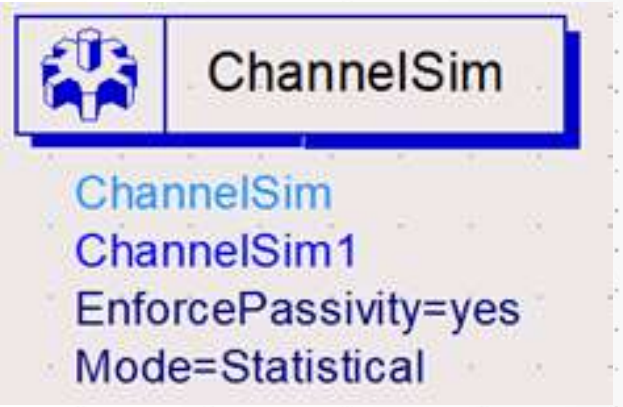
- IBIS is “Input/output Buffer Information Specification”
- AMI is “Algorithmic Modeling Interface”
- IBIS Open Forum added the AMI flow an alternate to the traditional (SPICE-based) flow in IBIS version 5.0
  - http://www.eda-stds.org/ibis/




- IBIS-AMI Modeling:
  - AMI model builders (typically IC vendors)
  - AMI model users (both IC vendors and OEMs)

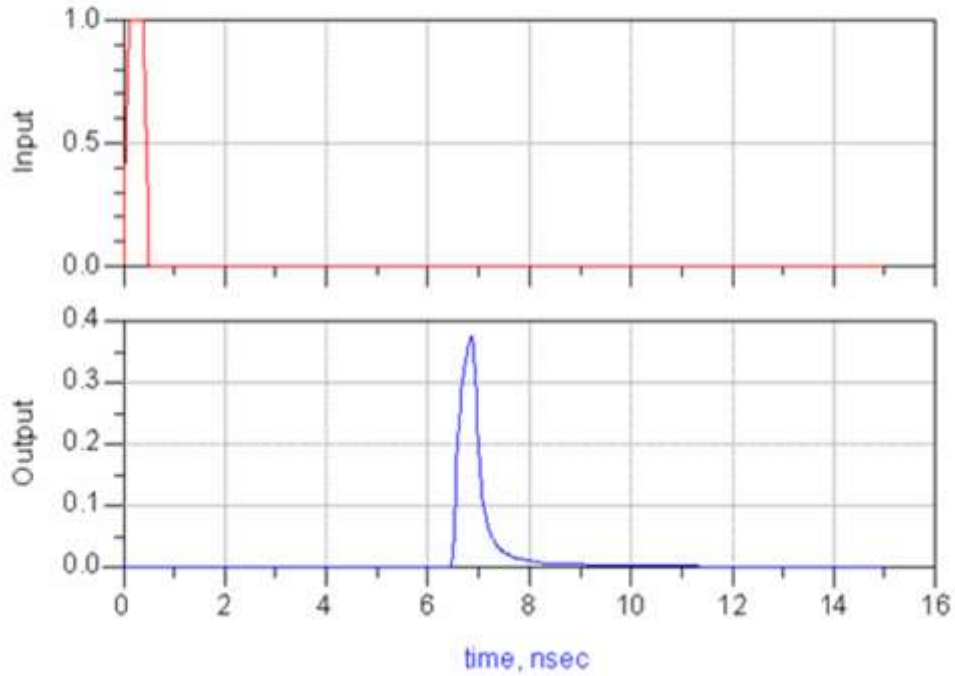
# Channel Simulator

- New Class of simulator to run FAST system analysis and display results about how signals will travel through the system.
- Channel must be Linear Time Invariant (LTI) in all cases
- Allows fast techniques:
  - convolution
  - Superposition
  - statistical methods
- Tx and Rx can be NLTV  in bit-by-bit mode
- Tx, Rx, and channel must also be LTI in statistical mode

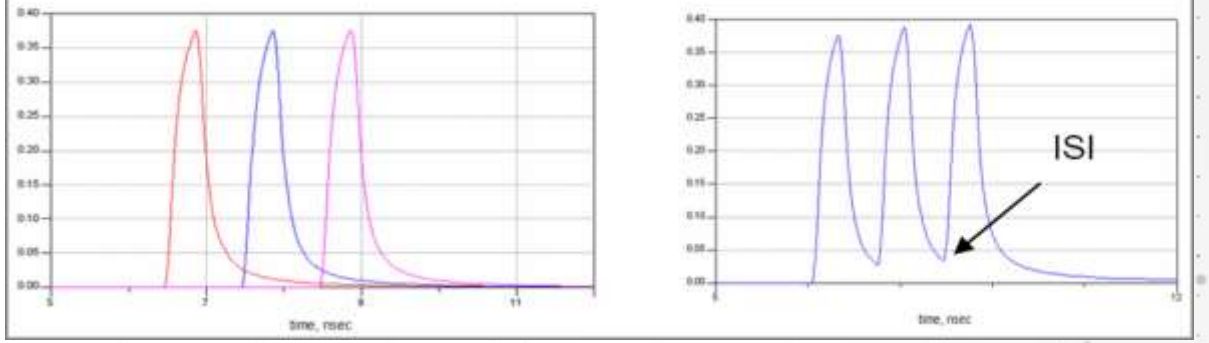


# Channel Simulator Methodology

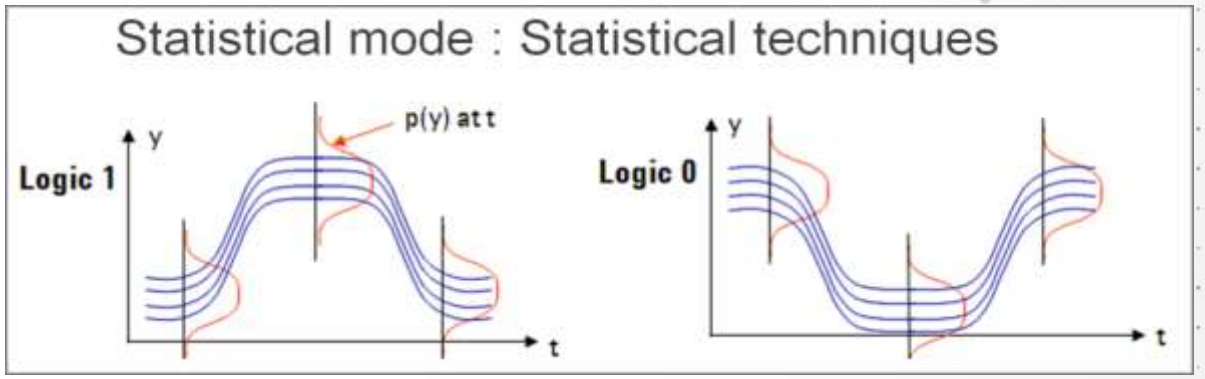
Impulse response is calculated using a short, traditional transient simulation




Bit by bit mode : Superposition of bits




Statistical mode : Statistical techniques



# Industry Golden Tool for AMI Simulation and Channel Sim

## INDUSTRY LEADING AMI SIMULATION BY ADS CHANNEL SIM

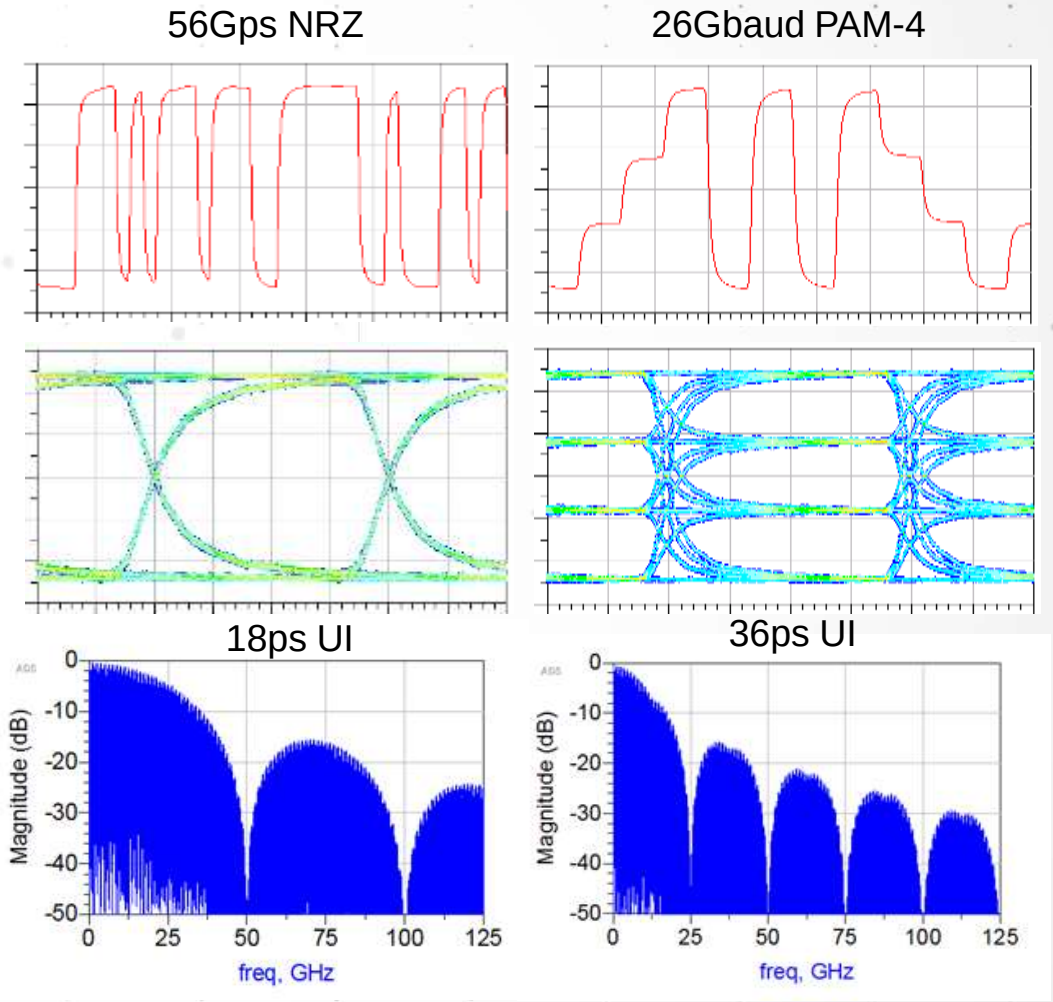
- Unique Treatment of Jitter Amplification in ADS
- The Rao Method Pattern
- PAM-4 Channel Simulation

**United States Patent** 7,962,541
*Rao* June 14, 2011

Optimization of spectrum extrapolation for causal impulse response calculation using the hilbert transform

**Abstract**

A causal impulse response function is calculated from a truncated spectrum by extending the real part of the spectrum beyond the truncation frequency and computing the imaginary part with the Hilbert transform to enforce causality. The out of band extrapolation is optimized to reduce the discrepancy between the computed and the original imaginary part in the in band frequency range so that the causal impulse response accurately represents the original spectrum. The technique can be applied to spectral with the delay phase subtracted to enforce delay causality. The Hilbert transform may be employed to maintain causality in S-parameter passivity violation correction. At frequencies where violation happens, the S-parameter matrix is scaled down by the inverse of the magnitude of the largest eigenvalue. Magnitudes at other frequencies are unchanged. An additional phase calculated by the magnitude phase Hilbert transform is added to the scaled spectrum to maintain the causality.



# PathWave ADS Memory Designer

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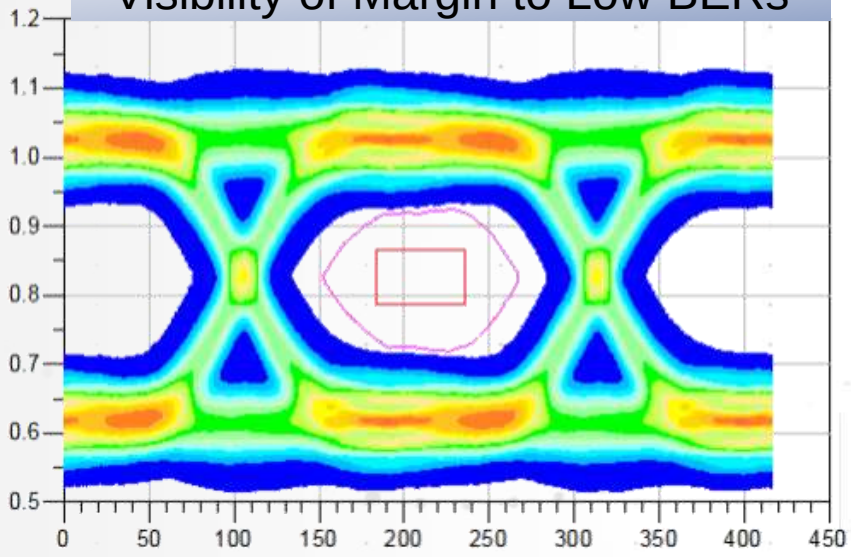
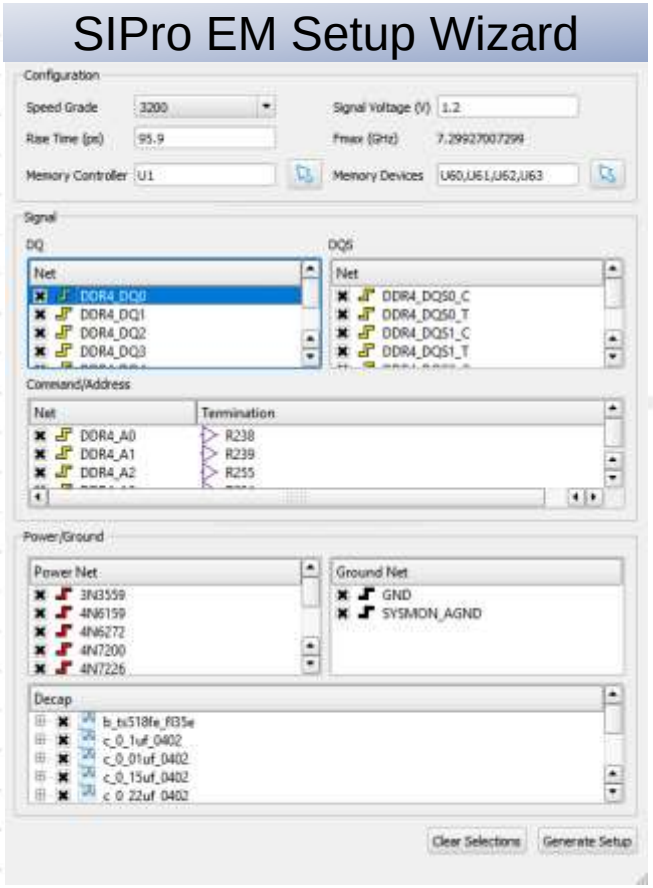
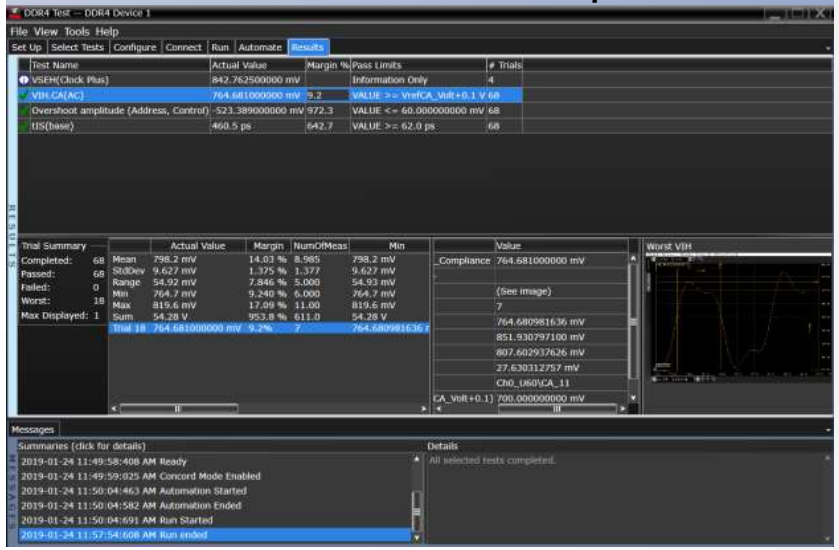
## Visibility of Margin to Low BERs




## SIPro EM Setup Wizard




## Automated DDR4 Compliance

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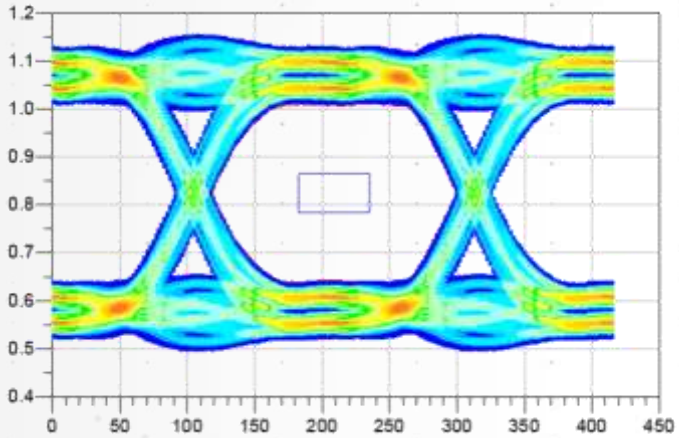
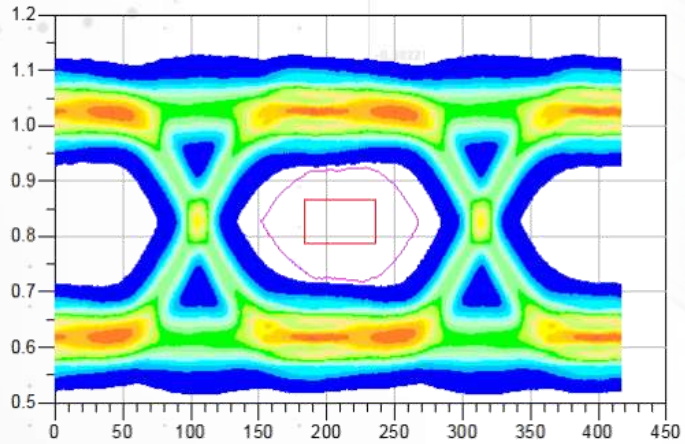
# Design with Your Eyes Wide Open

As DDR speeds increase – Random Jitter and Crosstalk become very significant




DDR5 – 4800
No Jitter or Xtalk




DDR5 – 4800
With Rj & Xtalk

Accurate EM simulation of the PCB +
DDR Statistical Bus Sim =
**Confident Prediction of Margin to Mask**

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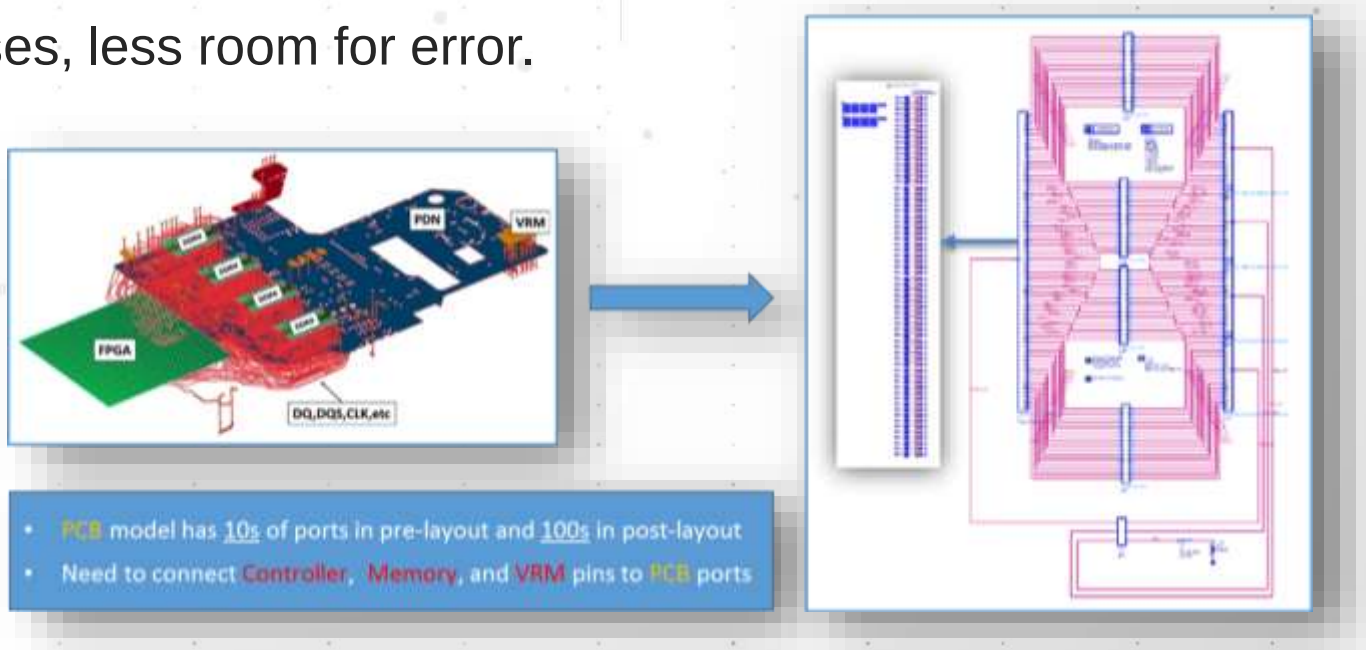
# DDR Memory Design Is Already Complex!

## THE CHALLENGE OF TODAY'S HARDWARE DESIGNER

- Hours of setup time before first simulation
- Topology and configuration changes require multiple schematics and many parameter values to sweep through
- Hard to collate results, hard to gather insights into the design, and hard to optimize the design
- Shrinking design margins as speed increases, less room for error.
- After small production run - difficult to troubleshoot issues found
- Uncertainty for product reliability and significant risk to design schedules

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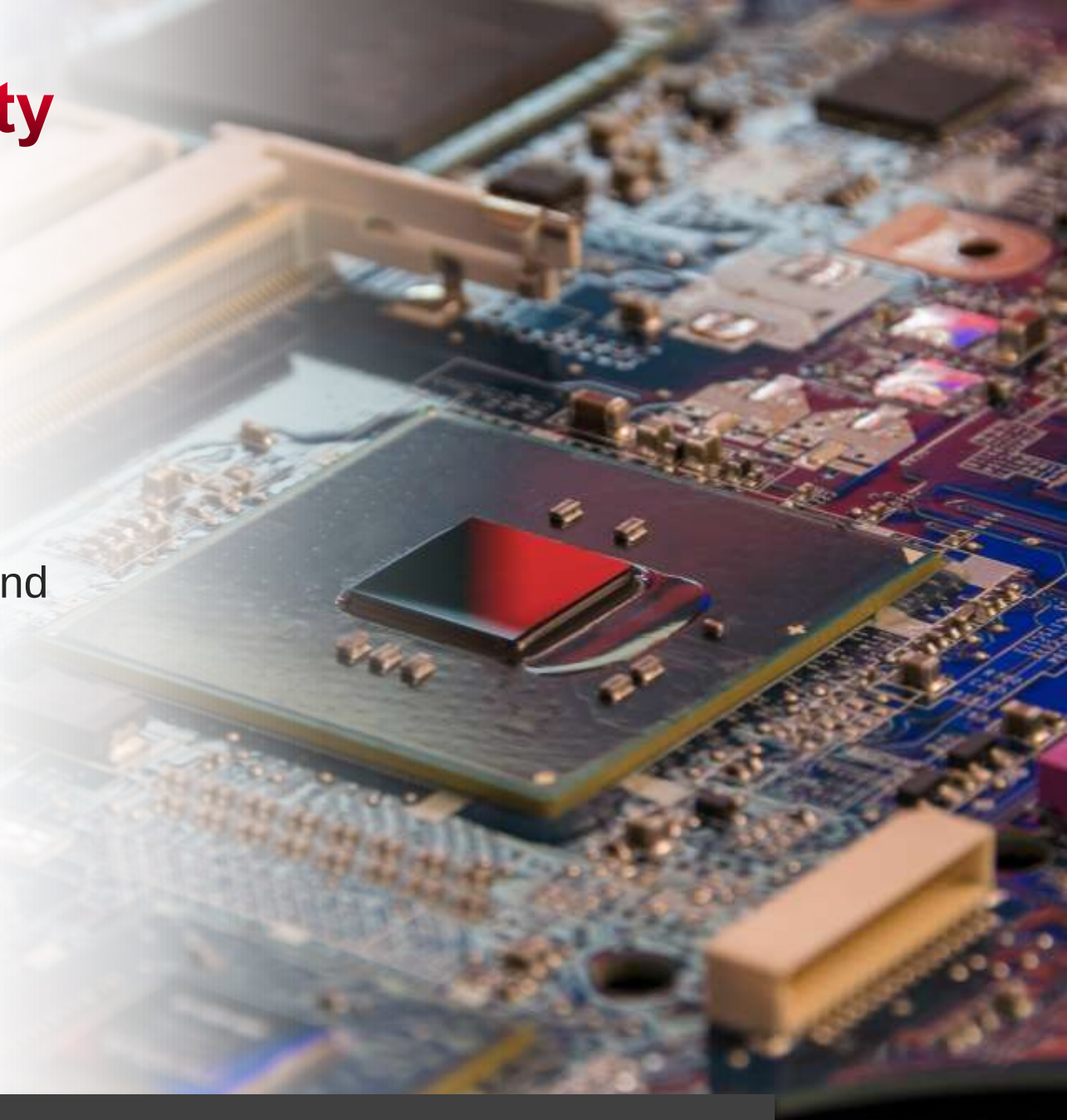
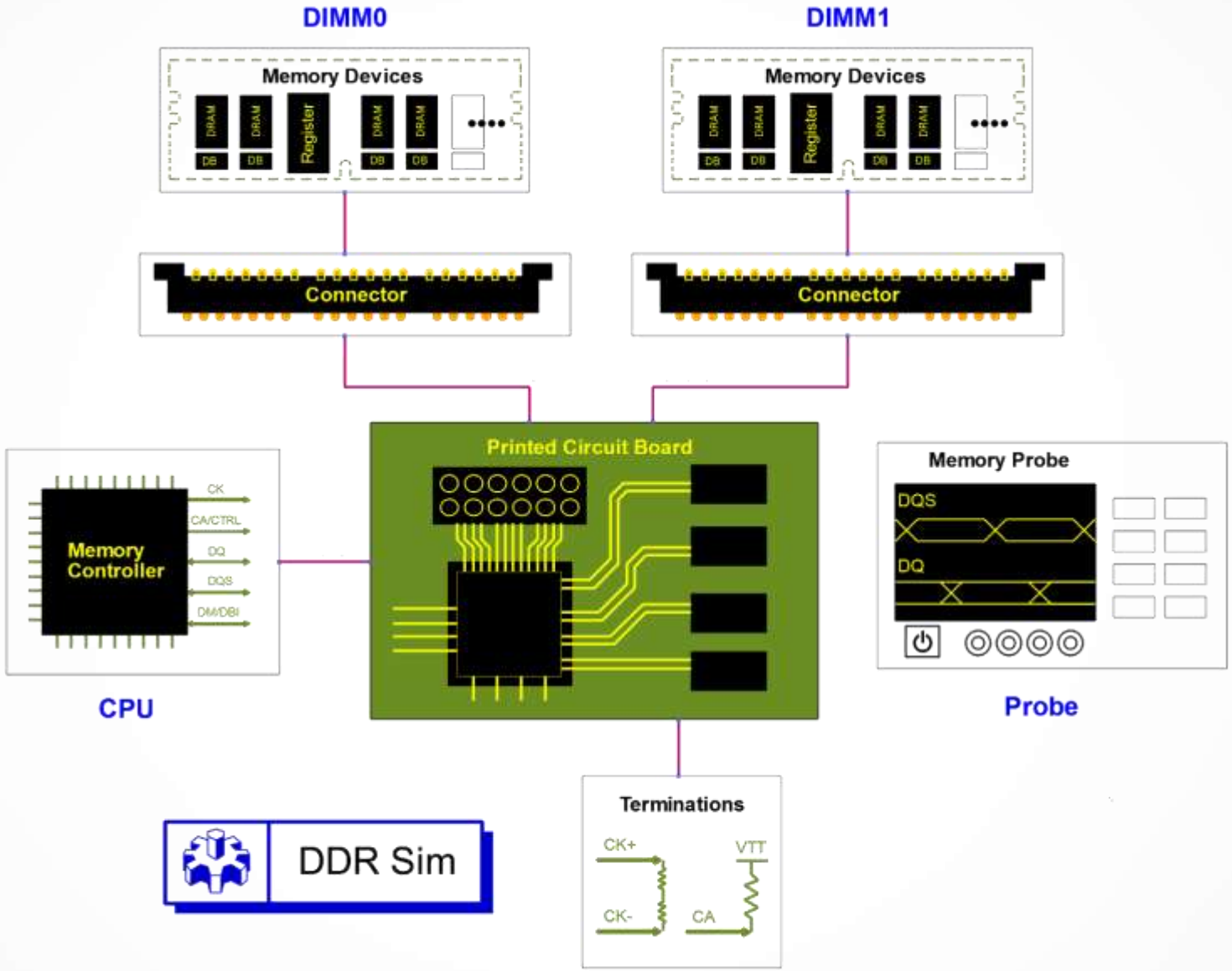
# Reduce Simulation Complexity

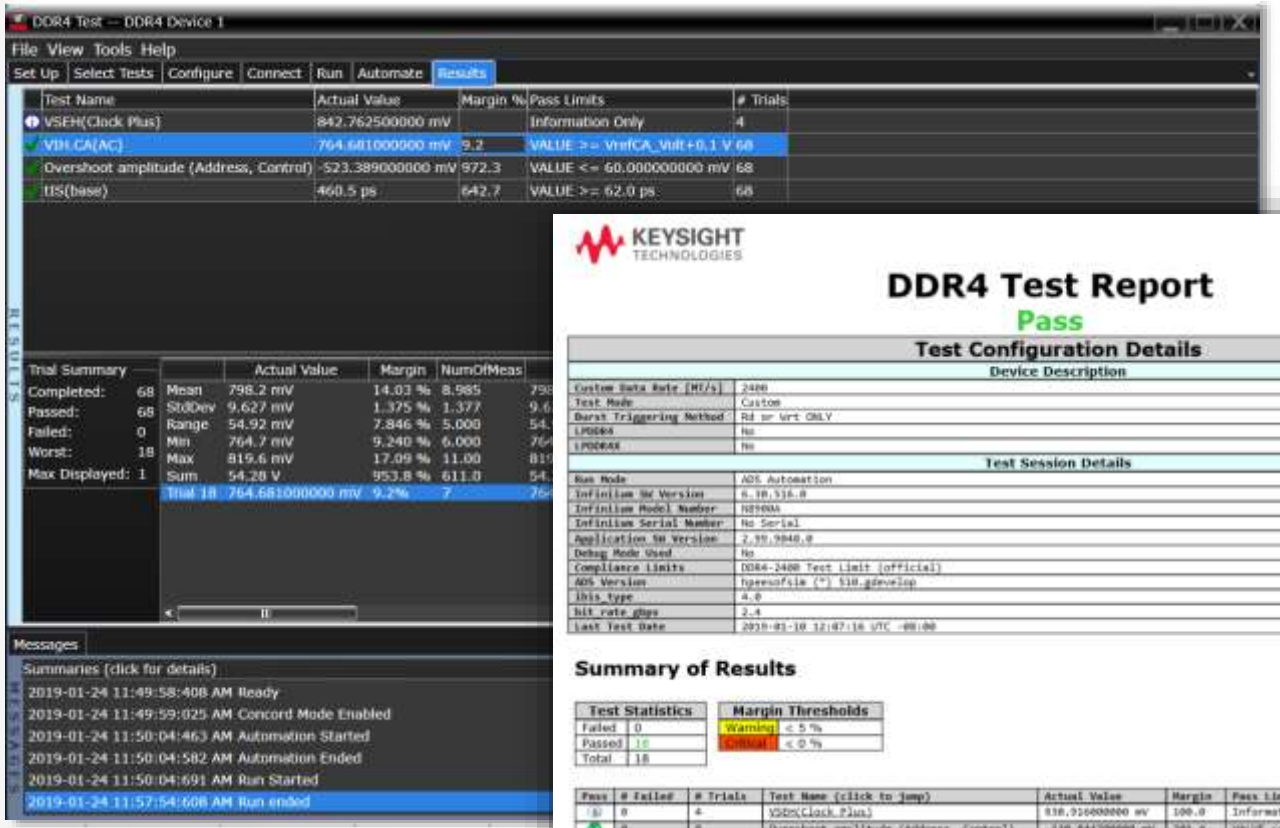
- From hours of setup time to minutes
- One schematic for both Transient & DDR Bus simulation
- Apply IBIS models for groups of signals as one
- One click connection - to automatically match and connect components
- Both pre-layout and post-layout flow
- SIPro DDR wizard for easy EM setup of many nets at once
- Apply measurements to groups of signals




DIMM0
DIMM1
Memory Devices
DRAM
DB
Register
Connector
Printed Circuit Board
Memory Controller
CK
CA/CTRL
DQ
DQS
DM/DBI
CPU
Memory Probe
DQS
DQ
Probe
Terminations
CK+
CK-
VTT
CA
DDR Sim

# Investigate Pre-Compliance for Sign-Off

## INDUSTRY PROVEN MEASUREMENT SCIENCE







Automatically invoked and controlled by ADS

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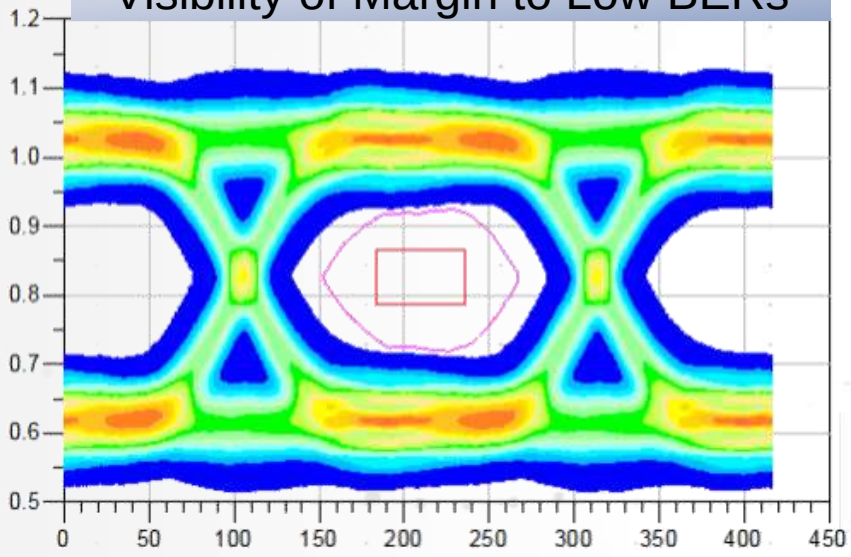


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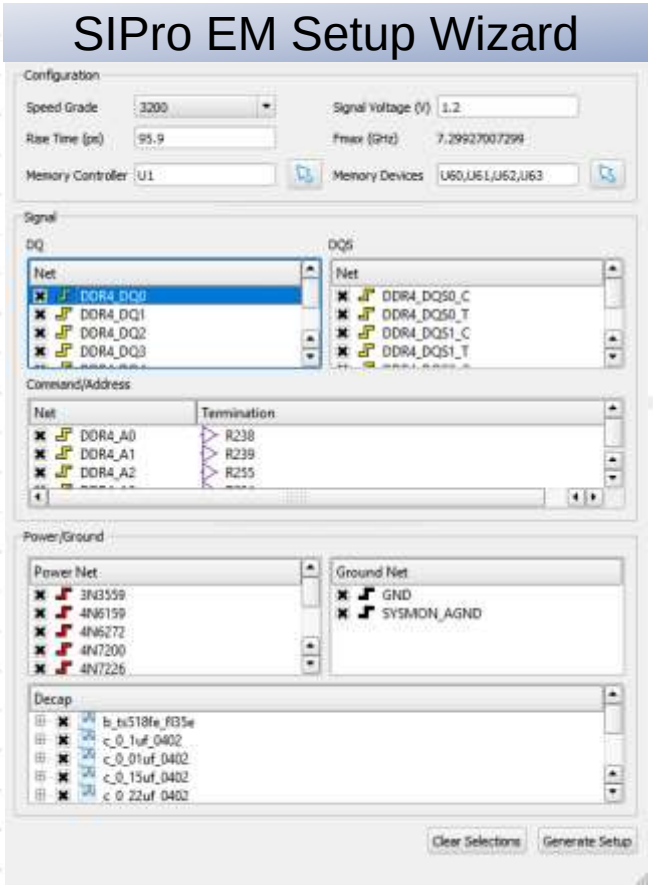


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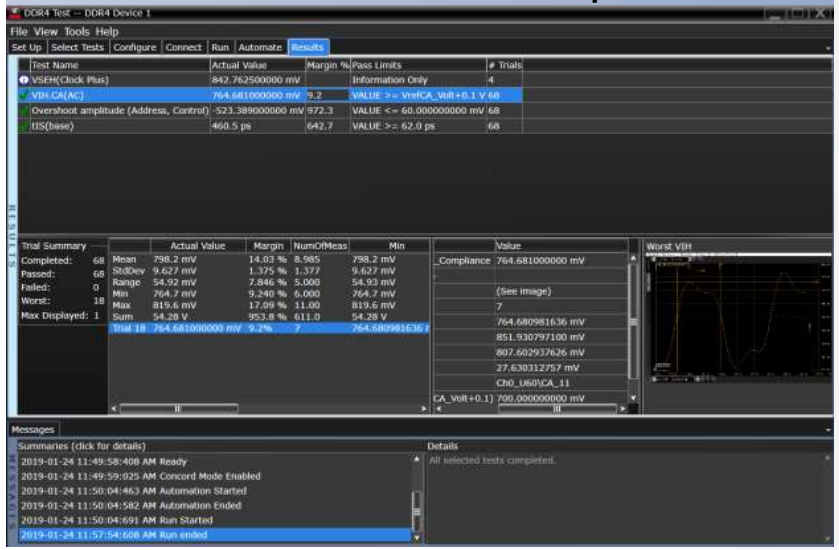


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