Test Challenges from DDR3 to DDR4 and DDR5

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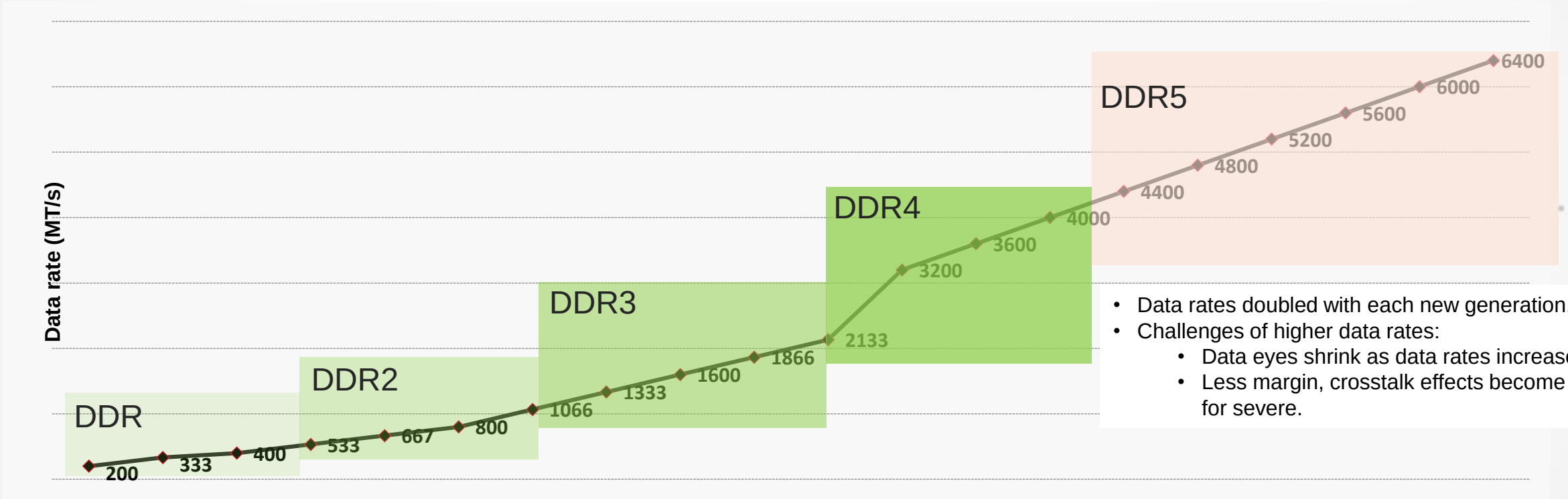
KEYSIGHT TECHNOLOGIES

Agenda

- DDR Trend and Signal Evolution
- Keysight DDR5 Solution
  - Tx
  - Rx
  - Protocol
- Summary

Technology Trends

DDR5 DOUBLE THE SPEED OF DDR4



- Data rates doubled with each new generation.
- Challenges of higher data rates:
  - Data eyes shrink as data rates increase.
  - Less margin, crosstalk effects become for severe.

Shrinking Margins

NEW CHALLENGES IN MAKING MEASUREMENTS

Full rate clock

- No Rx PLL needed

Wide, single ended

- Crosstalk dominated vs. loss dominated
- Increased emphasis on multi-channel Rx test impairments

Bidirectional

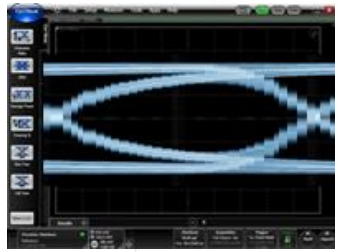
- Spec impact on both write and read training

Bursty

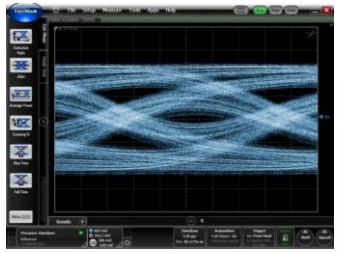
- ISI impact differs on preamble, first bits, rest of burst
- Emulation of hi-Z states

“Distributed Rx”

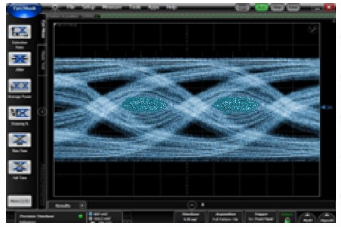
- Equalizer settings performed by DRAM controller
- DRAM/Buf/Reg retains Taps



1600 MT/s



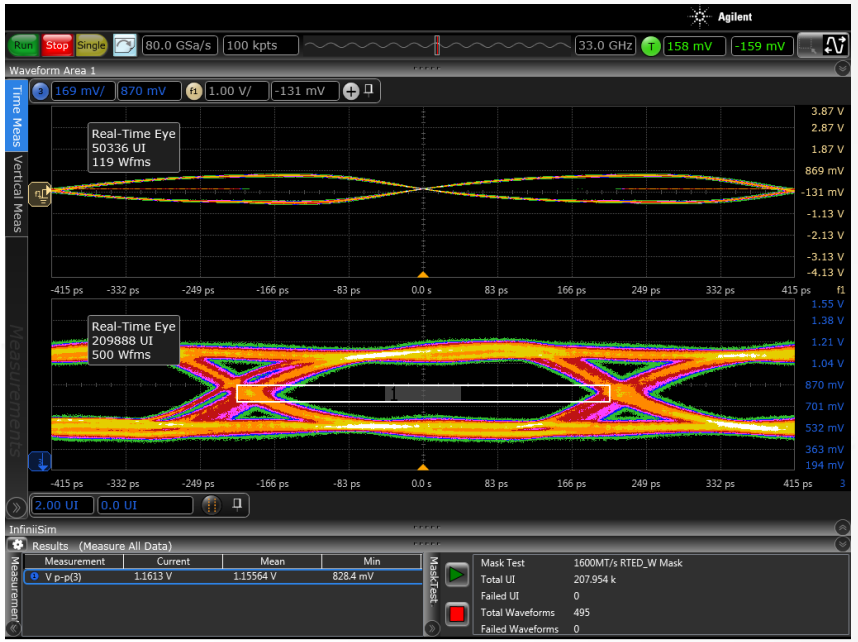
3200 MT/s



6400 MT/s

The Good Old Days

DDR3 AND DDR4 MEASUREMENT REQUIREMENTS



DDR3

- RW separation: DQS/DQ phase difference
- DQ validation: Setup/hold time tests

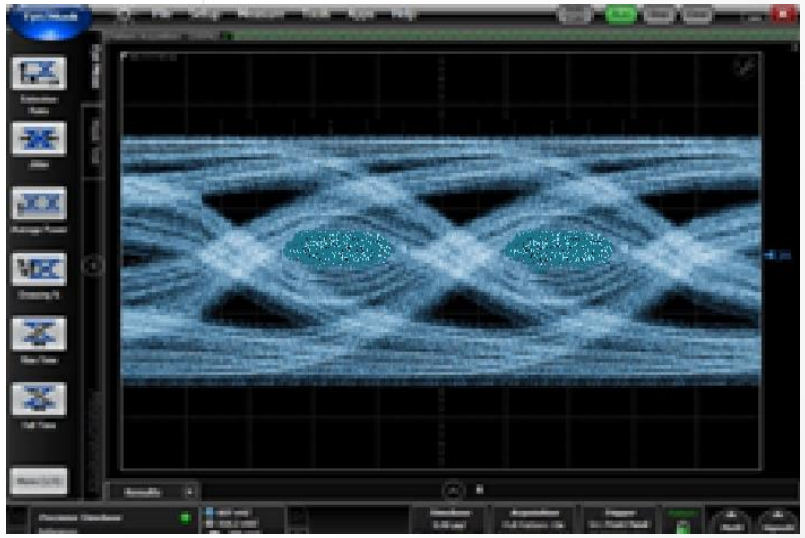
DDR4/ LPDDR4

- RW separation: DQS/DQ phase difference. Pre-amble pattern difference (LPDDR4).
- DQ validation: Rx mask test

DDR5 Disruption

THE FUZZY EYE TAKES OVER

- New measurement science for read/write separation.
  - No DQS-DQ phase difference.
  - Same pre-amble pattern on both read and write cycles.
- New DQS, DQ, CK nUI jitter tests.
- No DQ mask tests
- DFE may be required for speed above 3.6 GT/s.



DDR5 Receivers

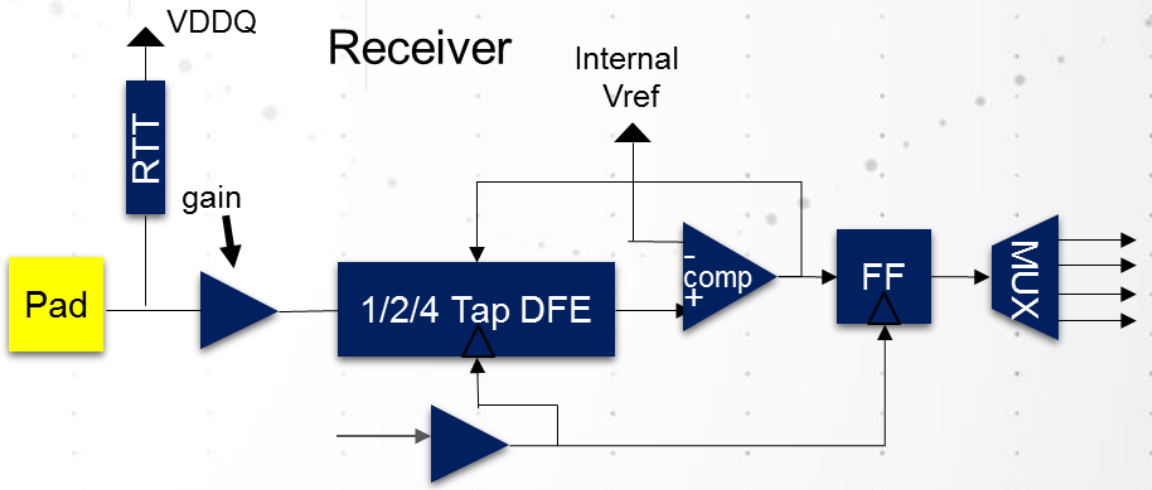
MEASUREMENT CHALLENGES

Uncorrelated Jitter

- Sinusoidal or Periodic Jitter – caused predominately by clock circuits
- Random Jitter (RJ) – caused by active components and other thermal effects

Level Interference

- Sinusoidal Interference – clock circuits, power supplies etc.
- Random Interference – thermal effects and caused by active components
- Cross-Talk

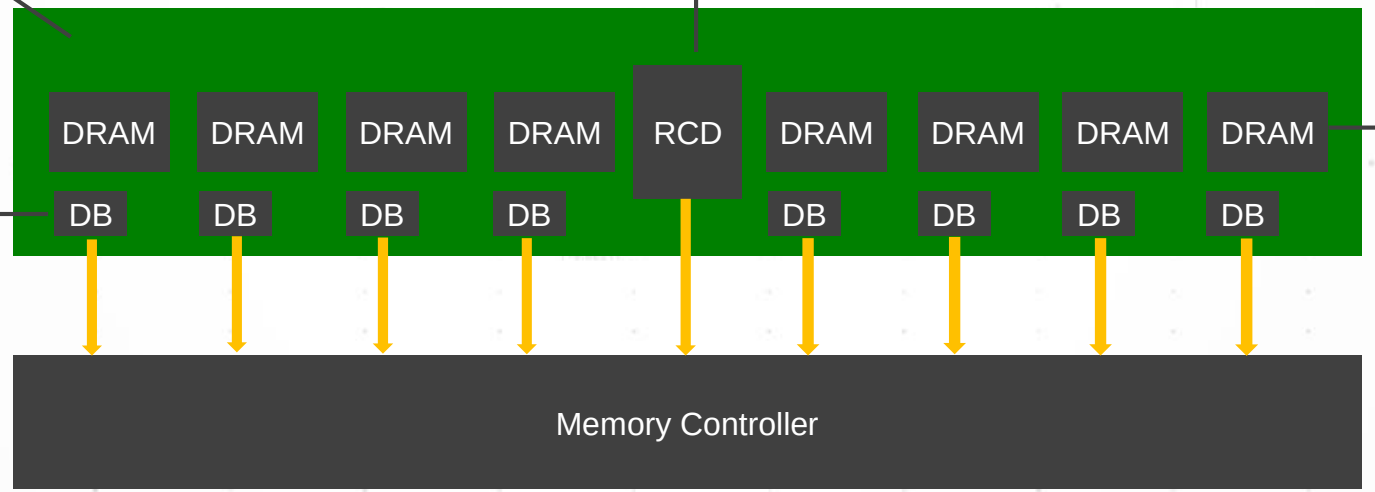


DDR5 Devices

System Integrators
- Tx test
- Rx test
- Protocol test

DIMM (RDIMM, LRDIMM, UDIMM, SODIMM)
- Rx test
- Protocol test

Register
- Rx test
- Protocol test



Data Buffer
- Rx test
- Protocol test

DRAM
- Rx test
- Tx test
- Protocol test

DDR5 Tx Solution

THE TOTAL SOLUTION APPROACH

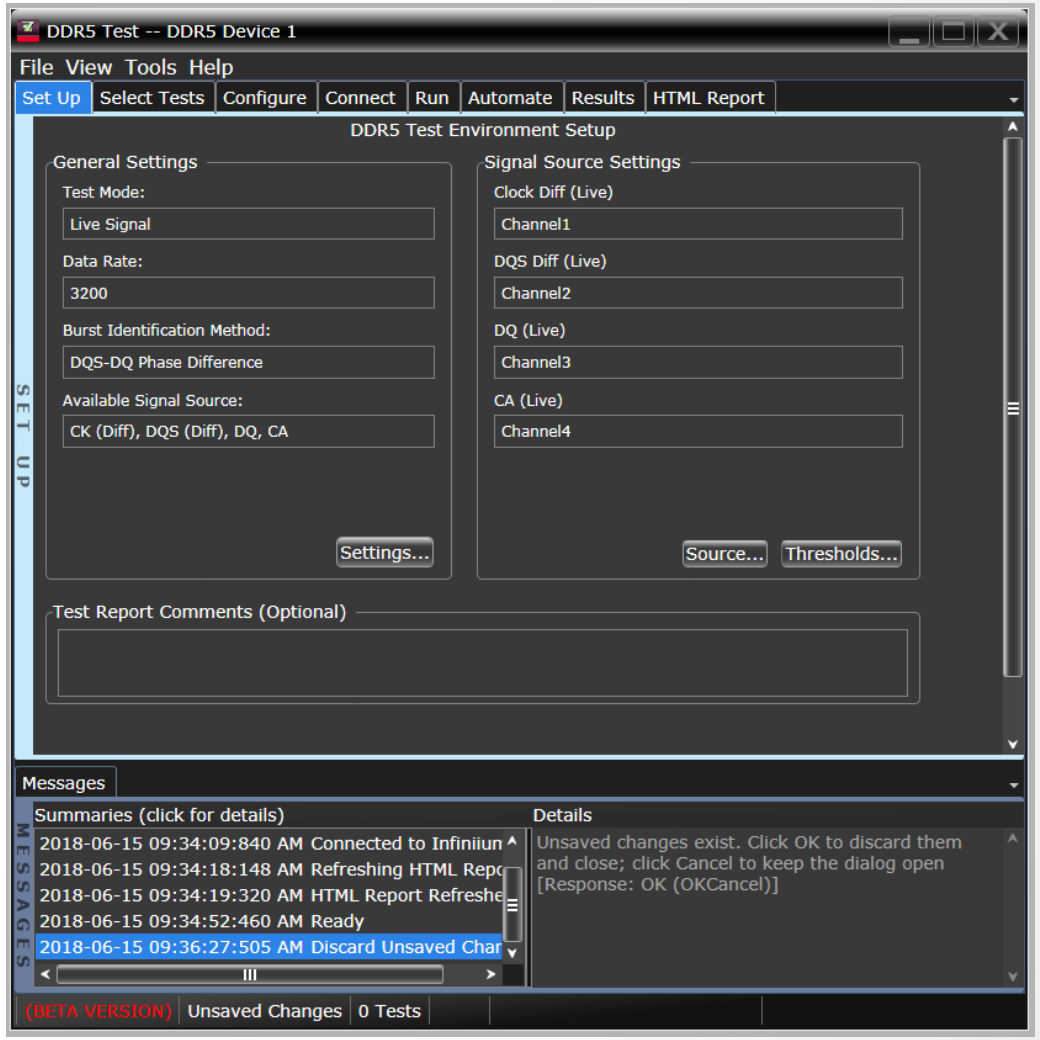
- New Measurement science for efficient and accurate measurement results
- Automated Compliance test for speedy test time.
- BGA interposer for easy access to signal for testing.
- New ADS framework for completeness of simulation to validation workflow.
- Seamless connection to data repository for quick test result analysis and decision making process.

DDR5 Tx Compliance App

IT'S ALL ABOUT THE TEST SPEED

Enable getting to market faster with high confidence in the measurement result:

- Complete test coverage:
  - Supports the latest DDR5 JEDEC draft spec.
  - Speed bin - from 3200 to 6400 MT/s.
  - Supports electrical, timing, jitter and eye diagram tests.
- New algorithm for fast test time. >60 % improvement vs legacy DDR3 and DDR4 apps.



DDR5 Test Lists

Electrical Test

VOH(AC)
VOH(DC)
VOL(AC)
VOL(DC)
SRQseR
SRQseF
Overshoot amplitude (Clock)
Overshoot area above VDD Abs Max(Clock)
Overshoot area between VDD and VDD Abs Max(Clock)
Undershoot amplitude (Clock)
Undershoot area below VSS(Clock)
VIHdiff.CK(AC)
VIHdiff.CK(DC)
VILdiff.CK(AC)
VILdiff.CK(DC)
SRIdiffR
SRIdiffF
Vix_CK_ratio
VOHdiff(AC)
VOLdiff(AC)
SRQdiffR
SRQdiffF

Timing Test

tDQSS
tDSS
tDSH
tWPRE
tWPST
tDQSCK
tRPRE
tRPST
tLZDQS
tHZDQS
tCKE

Eye-Diagram Test

tCIVW Margin
vCIVW Margin
CA VIHL(ac)
SRIN_cIVW
tCIPW

Jitter Test

tTx_DQS_Duty_UI
tTX_DQS_1UI_Rj_NoBUJ
tTx_DQS_1UI_Dj_NoBUIJ
tTX_DQS_NUI_Rj_NoBUJ
tTx_DQS_NUI_Dj_NoBUJ
tTx_DQ_Duty_UI
tTX_DQ_1UI_Rj_NoBUJ
tTx_DQ_1UI_Dj_NoBUIJ
tTX_DQ_NUI_Rj_NoBUJ
tTx_DQ_NUI_Dj_NoBUJ
tTX_DQS2DQ
tCK
tCK_Duty_UI
tCK_Duty_UI_Error
tCK_1UI_Rj_NoBUJ
tCK_1UI_Dj_NoBUJ
tCK_1UI_Tj_NoBUJ
tCK_NUI_Rj_NoBUJ
tCK_NUI_Dj_NoBUJ
tCK_NUI_Tj_NoBUJ

New Probes for new Technology

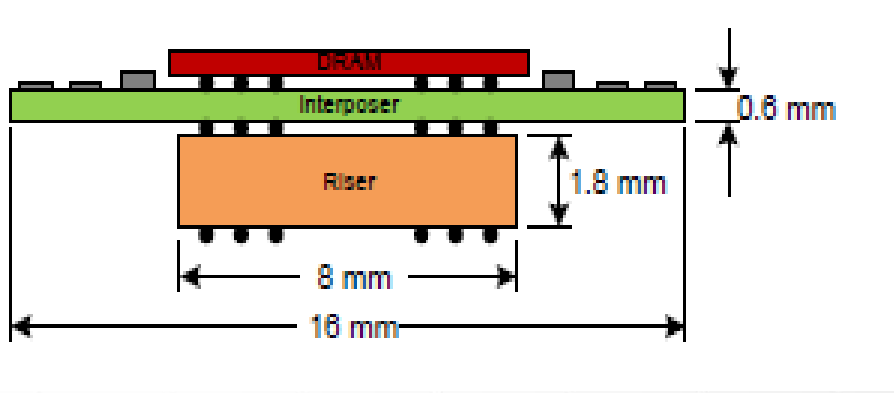
KEY PIECE TO COMPLEMENT THE TX SOLUTION

We want to solve these challenges:

- **Existing BGA interposer design can't handle top speeds in DDR5.**
- **Homegrown interposer requires engineering resource, which is expensive.**

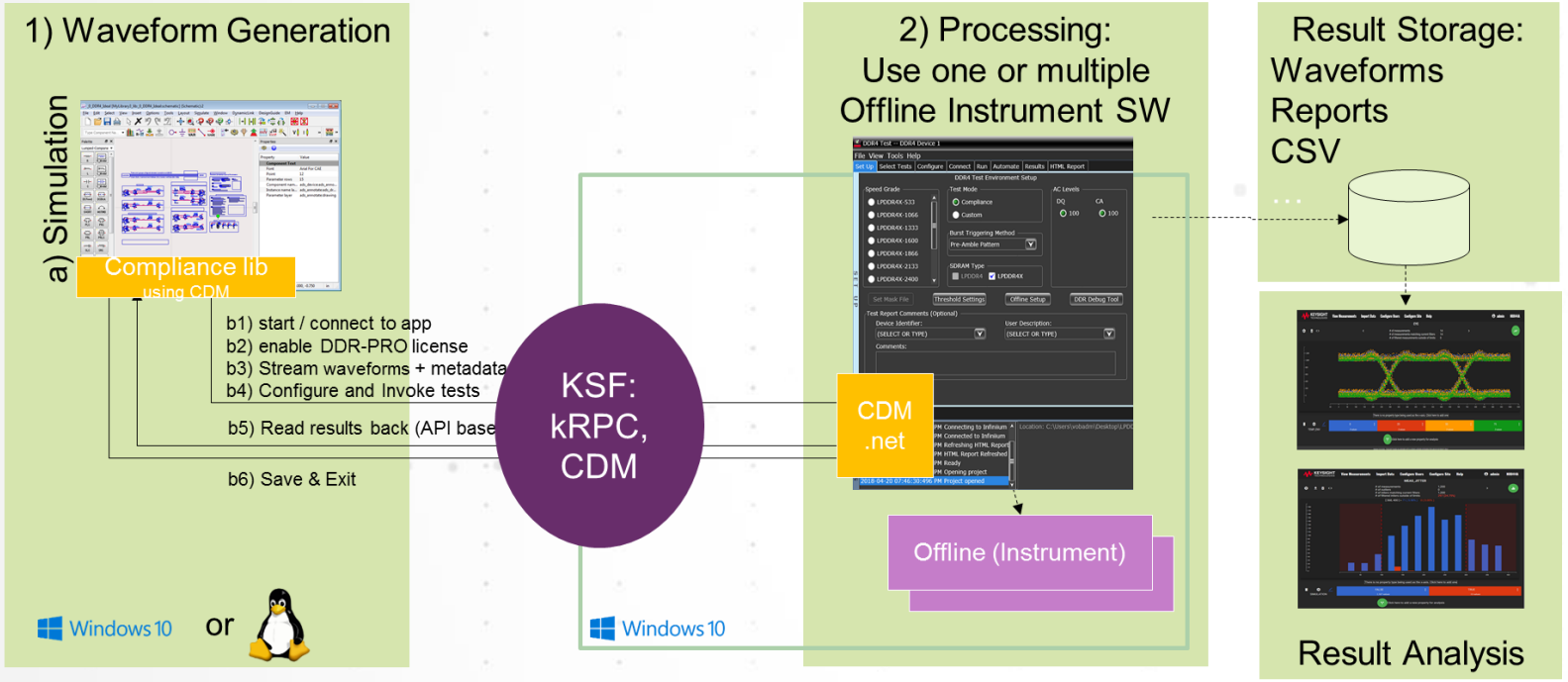
The DDR5 BGA Interposer plan:

1. Design and build an initial DDR5 x4/x8 High Performance SI Interposer and riser.
2. Re-spin the DDR5 HP SI Interposer for improved bandwidth
   - …as dictated by market conditions
3. Develop an integrated Riser + Interposer
   - Better performance than separate parts
   - Easier attachment to DUT



ADS Integration

INCREASE CONFIDENCE IN THE DESIGN

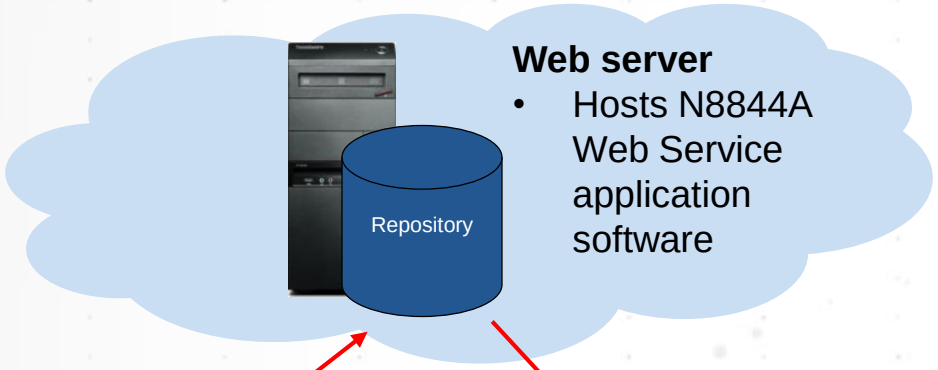


Enable better-correlated compliance measurements (from simulation to test). Fewer surprises, shorter time to market.

- Streamlined integration between ADS and Infiniium Offline with DDR5 compliance test app.
- ADS automates the configuration and control of the compliance test, and receives measurement results back.

Data Analytics

ENABLE SHORTER TIME TO MARKET

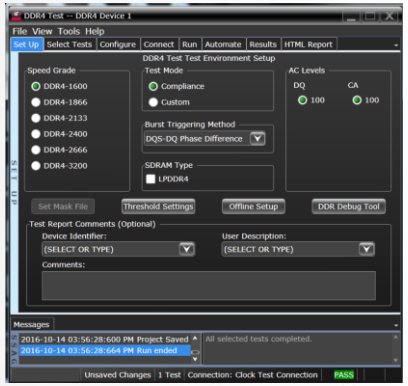


Web server

- Hosts N8844A Web Service application software

Data Import

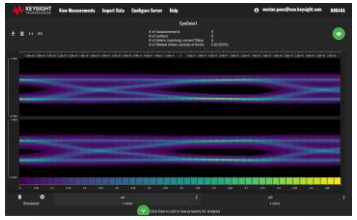
- Test result with test condition



Keysight compliance software

Data Retrieval

- N8844A Web Visualization tool

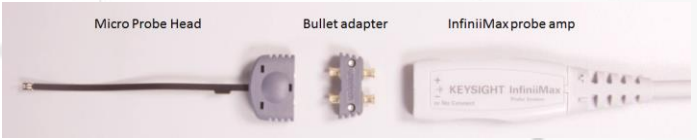


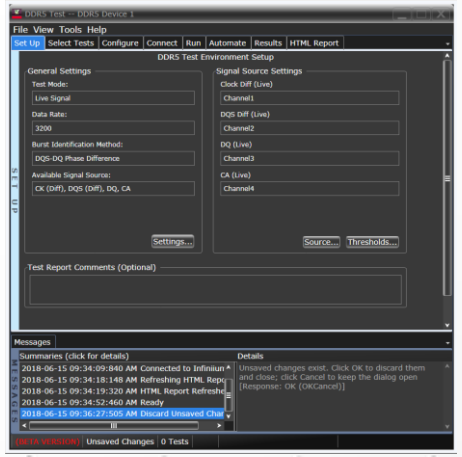
- **Enable your customer:**
  - **Save at least $1M chip redesign cost.**
  - **Increase at least 20% in productivity.**
- Seamless connection to the N8844A Data analytics software:
  - Offers enterprise class repository to store the data.
  - Allows real time data retrieval with modern visualization tool.

Configuration Guide

TX TESTS REQUIREMENTS

Model number	Description	Quantity
Oscilloscope (16 or 20 GHz scope – V or the new UXR series)		
UXR0204A	20 GHz Infiniium scope	1
Probes (20 GHz)		
TBD	InfiniiMax II RC probe amplifiers	4
MX0100A	Micro probe head	1 (5 heads, 1 bullet adapter)
TBD	Bullet adapter	3
TBD	DDR5 BGA interposer	1
Software		
N6475A	DDR5 Tx Validation software	1
E2688A	Serial Data Analysis	1
N8823A	EZJIT Complete	1
N5461A	Equalization tool	1
N5465A	InfiniiSim software	1





DDR5 Rx Solution

PROVIDE LEADERSHIP IN NEW MEASUREMENTS

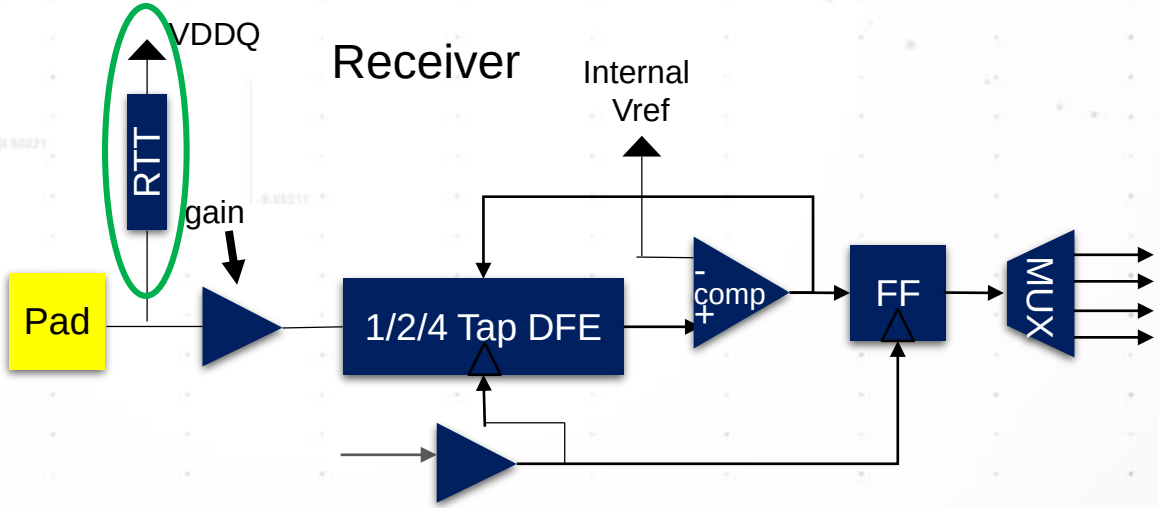
- JEDEC is defining key Rx measurement requirements.
- Keysight is taking the leadership in helping to define the measurement methodologies.
  - The DDR5 Rx compliance test application
  - DDR5 Rx Test Fixtures

DQ RX characterization dependency

IMPACT OF ODT ON DQ RX BEHAVIOR

- ODT is used to optimize the signal quality for the signal that is presented to the Receiver
  - In the test setup we will shape the signals by BERT setting for level and jitter
- We can assume, that the quality of the RX (e. g. Loss compensation by the DFE taps) is independent of RTT setting
- Proposal is to use 48 Ohm for this characterization to minimize mismatch to standard test equipment

Proposal: Do RX characterization 48 Ohm RTT Setting



DDR5 Rx Test Compliance Application

KEY FEATURES

Measurements

- DQS Voltage Sensitivity
- DQ Voltage Sensitivity
- DQS Jitter Sensitivity
- DQ Stressed Eye
- CA Voltage Sensitivity
- CA Stressed Eye
- DQS2DQ
- Tap setting characterization (to be investigated)

Calibrations

- Amplitude Calibration
- Jitter Calibration
- Xtalk Calibration
- Stress Eye Calibration
- DFE calibration

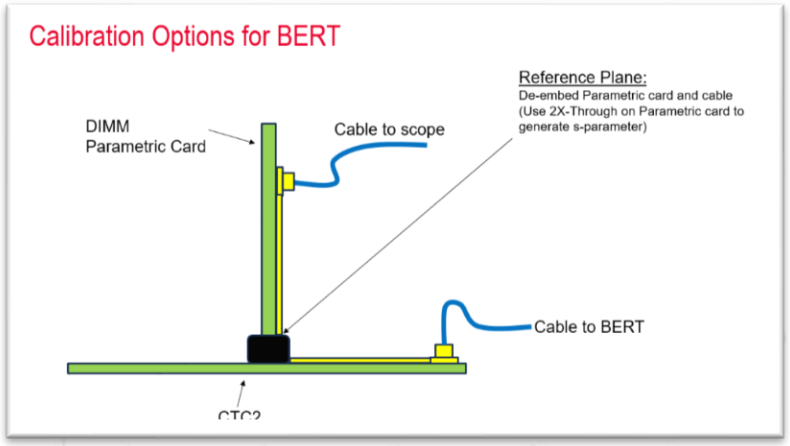
Other Features

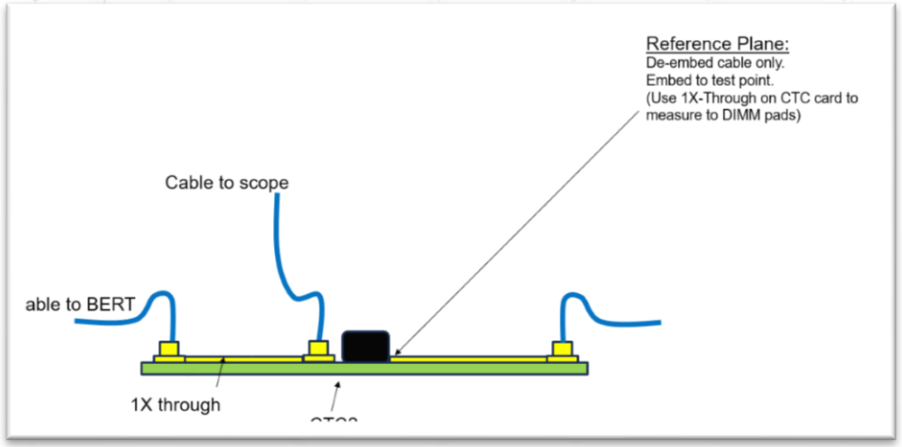
- Supporting Data Analytics with N8844A
- BER extrapolation down to 1E-18
- Analyze on De-mux and full speed loop back pins
- Analyze on built-in error counters

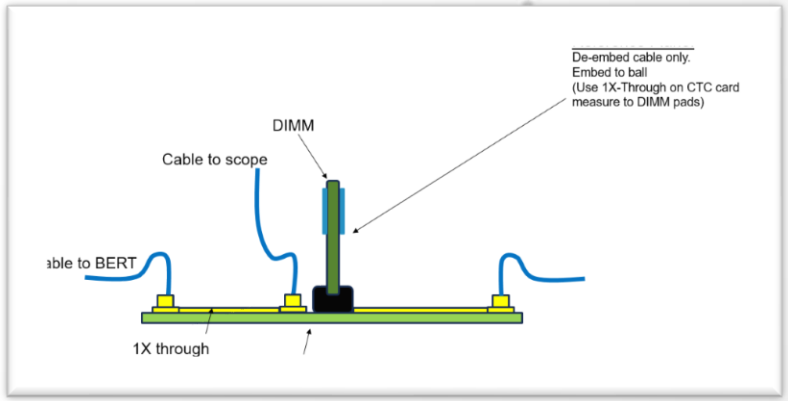
DDR5 Rx Calibrations

CALIBRATION OPTIONS FOR BERT

- DQS/DQ Calibrations
  - DQS2DQ Skew Calibration
  - DQS Amplitude Calibration
  - DQ Amplitude Calibration
  - DQS DCD Calibration
  - DQS RJ Calibration
  - DQ RJ Calibration
  - DQ SJ Calibration
  - DQ Crosstalk Calibration
  - DQS2DQ Calibration
- CK/CA Calibrations
  - CK CA Skew Calibration
  - CK Amplitude Calibration
  - CA Amplitude Calibration
  - CK DCD Calibration
  - CK RJ Calibration
  - CA RJ Calibration
  - CA SJ Calibration
  - CA Crosstalk Calibration
  - CK CA Alignment Calibration
- DQS/DQ Tests
  - DQS Voltage Sensitivity Test
  - DQ Voltage Sensitivity Test
  - DQS Jitter Sensitivity Test



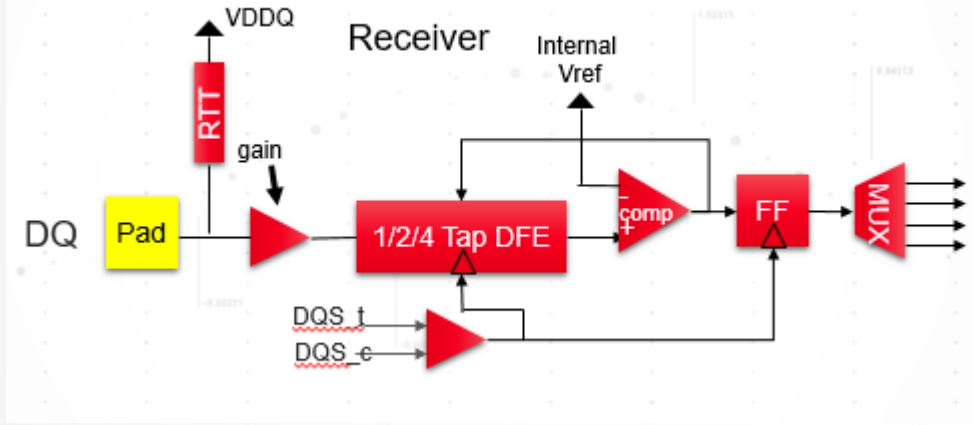




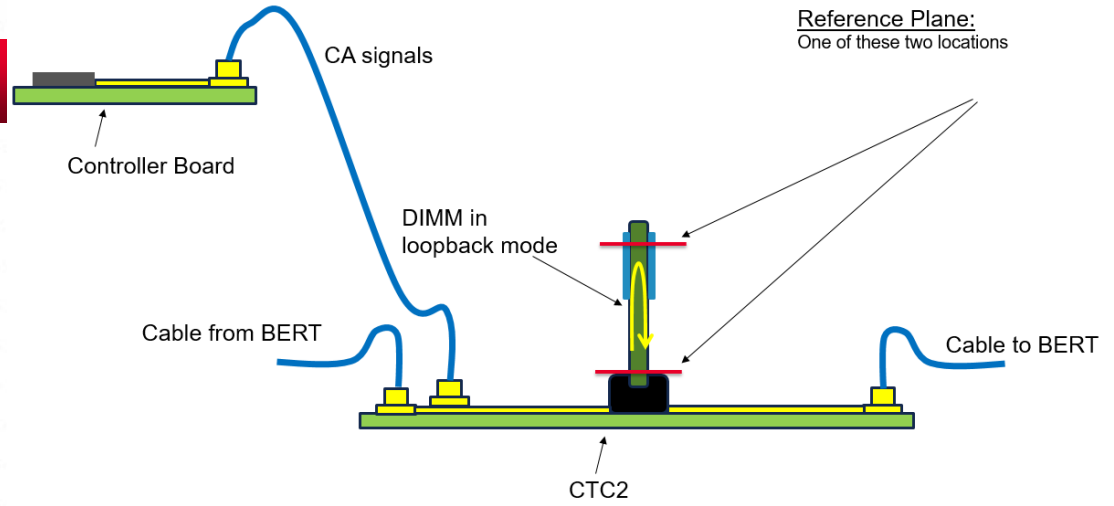
DDR5 Rx Tests

RX TESTS

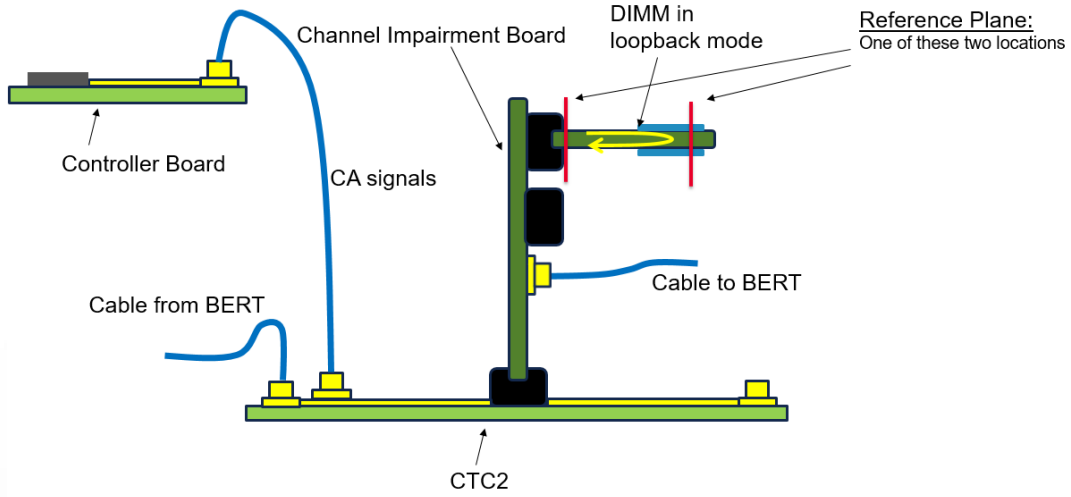
- DQS/DQ Tests
  - DQS Voltage Sensitivity Test
  - DQ Voltage Sensitivity Test
  - DQS Jitter Sensitivity Test
  - Rx Stressed Eye Test
  - DQS2DQ Test
  - DFE Characterization



Rx Measurement (DQ, non-stressed eye)

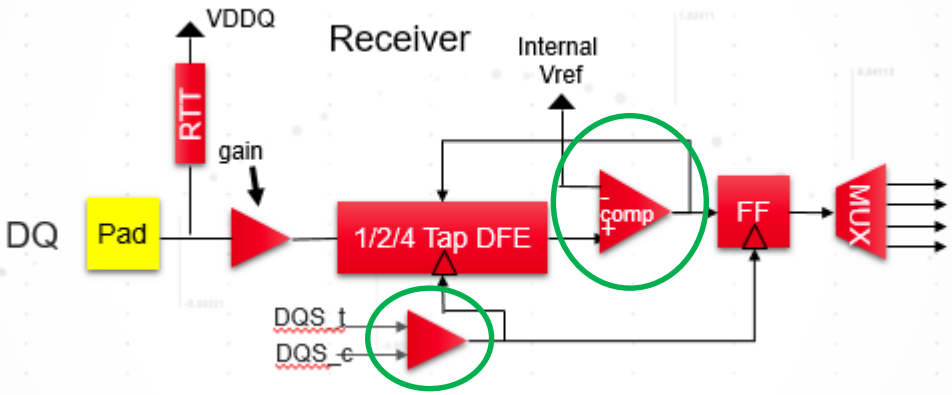


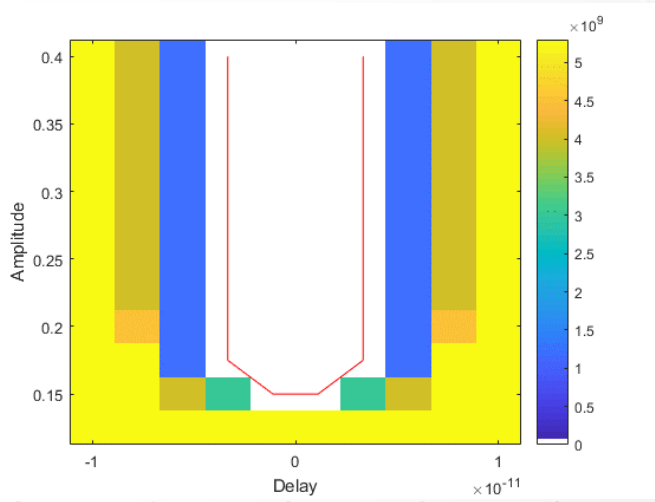
Rx Measurement (DQ, stressed eye)



DQS and DQ Voltage Sensitivity

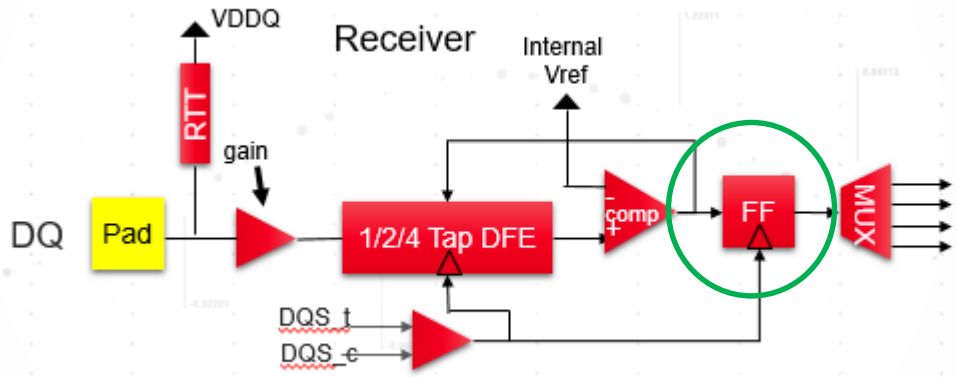
Test	DQ	DQS	CLK	DFE	Fixture
DQS voltage sensitivity (CLK)	Clean	Sweep V (clean)	Clean	Off	CTC2 1 slot
DQ voltage sensitivity (CA)	Sweep V (clean)	Clean	Clean	Off	CTC2 1 slot





DQS Jitter Sensitivity and DQS2DQ

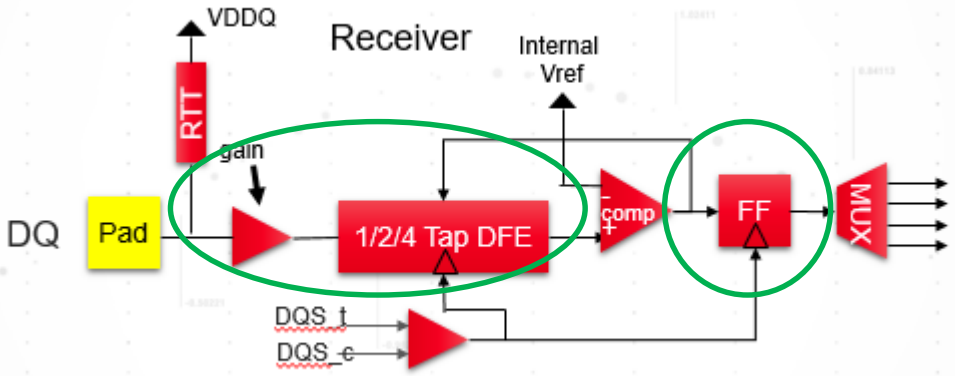
Test	DQ	DQS	CLK	DFE	Fixture
DQS jitter sensitivity - MEAS1	Clean	Sweep phase (clean)	Clean	Off	CTC2 1 slot
DQS jitter sensitivity - MEAS2 (DCD)	Clean	Sweep phase (specified DCD)	Clean	Off	CTC2 1 slot
DQS jitter sensitivity - MEAS3 (Rj)	Clean	Sweep phase (specified Rj)	Clean	Off	CTC2 1 slot
DQS jitter sensitivity - MEAS4(DCD+Rj)	Clean	Sweep phase (specified DCD+Rj)	Clean	Off	CTC2 1 slot
DQS2DQ	Clean	Clean	Clean	Off	CTC2 1 slot

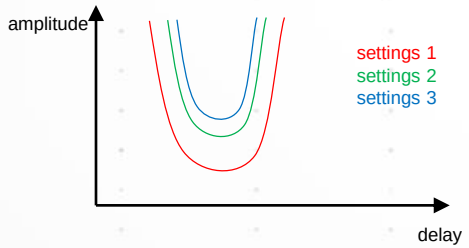


Internal delay alignment of DQS to DQ

DQS Stressed Eye and DFE Characterization

Test	DQ	DQS	CLK	DFE	Fixture
DQ stressed eye (CA)	Stress	Clean	Clean	Optimal (scope algo Or Ref Rx, OR specific per vendor?)	CTC2 1 slot with Channel Impairment board
Tap Characterization	ISI,reflections	Clean	Clean	Start with Optimal and characterize various settings	CTC2 1 slot with Channel Impairment board



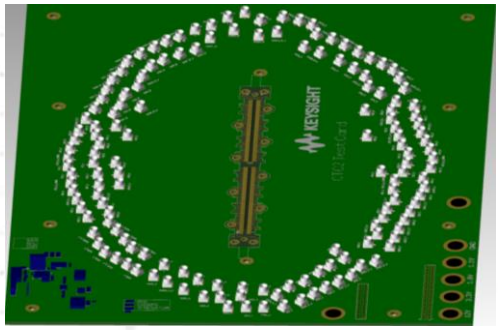


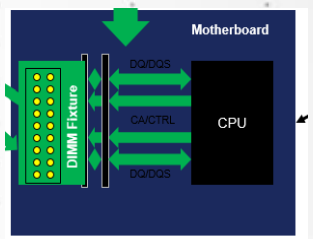
Test fixtures

KEY PIECES TO RX TESTS

Keysight developing “CTC2”

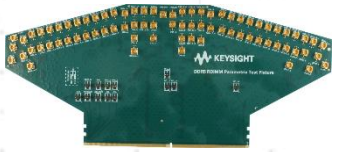
- USB control of DRAM / logic test modes
- Parametric grade DIMM connector
- Configurable for wide Xtalk / DUT stimulus w/ FPGA, ATE, AWG, custom
- Low cost 3rd party sourcing
- Open source design





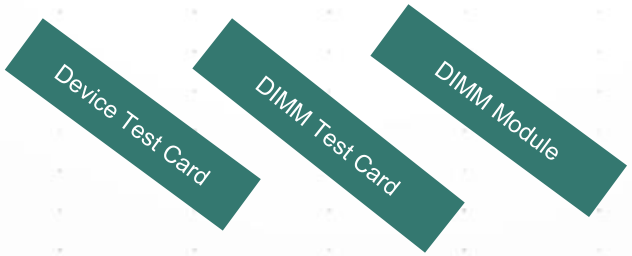
Keysight parametric DIMM probe

- For CPU/controller AV
- Low cost 3rd party sourcing
- Open source design



Intel / Partner DIMM Test cards

- Intel designed buffer test cards
- Installed in CTC2 for testing



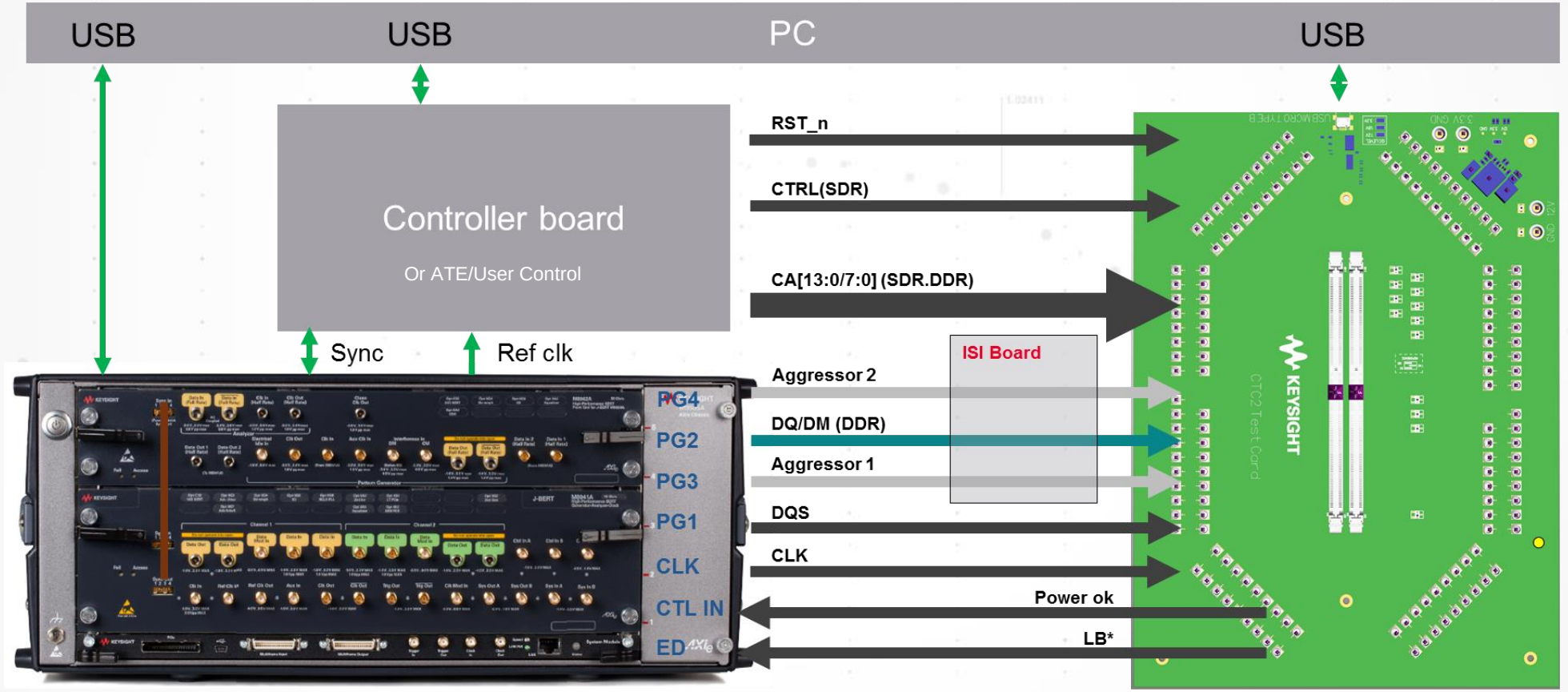
System Configurations

INITIAL RELEASE

- 2-ch BERT (No Aggressor Configuration)
  Customer supplies external channels for testing (e.g. ATE) OR
  Controller board to initialize memory and program DRAM Mode Registers
  Crosstalk is fully emulated using sinusoidal noise
- 4-ch BERT (Narrow Aggressor Configuration)
  Customer supplies external channels for testing (e.g. ATE) OR
  Controller board to initialize memory and program DRAM Mode Registers
  Crosstalk is generated using 1 or 2 more BERT channels

- Note: Different or wider configurations handled on per customer basis

4-ch BERT (Narrow Aggressor Configuration)



* There can be one or two loopback signals depending on the device under test

System Configurations

BASE VICTIM & NARROW AGGRESSOR

#	Product	Description
Base Victim		
1	M8041A-C08	BERT one channel, data rate up to 8.5 Gb/s
1	M8041A-0G2	Second channel for pattern generator
1	M8041A-0G3	Advanced jitter sources, module wide license
1	M8041A-0G4	Multi-tap de-emphasis, module wide license
1	M8041A-0G5	Adjustable Intersymbol Interference (ISI), module wide license
1	M8041A-0G6	Reference clock input with multiplying PLL, clockgroup-wide license
1	M8041A-0G7	Advanced interference sources for receiver characterization, module-wide license
1	M8041A-0A3	Analyzer equalization, module-wide license
Software & Platform		
1	M8070A-0TP	System software for M8000 BER test solutions, transportable license, perpetual
1	M8070A-1TP	DUT Control Interface, Transportable, Perpetual License
1	M8020A-BU2	Bundle consisting of one M9505A 5-slot AXIe chassis with USB

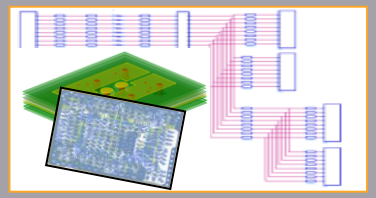
#	Product	Description
Narrow Aggressor extension		
1	M8051A-G08	Pattern generator one channel, data rate up to 8.5 Gb/s
1	M8051A-0G2	Second channel for pattern generator
1	M8051A-0G3	Advanced jitter sources, module wide license
1	M8051A-0G4	Multi-tap de-emphasis, module wide license
1	M8051A-0G5	Adjustable Intersymbol Interference (ISI), module wide license
1	M8051A-0G7	Advanced interference sources for receiver characterization, module-wide license

Design, Debug, Test, and Validation Solutions

Design

Keysight EEsof ADS

Simulation Measurement Correlation



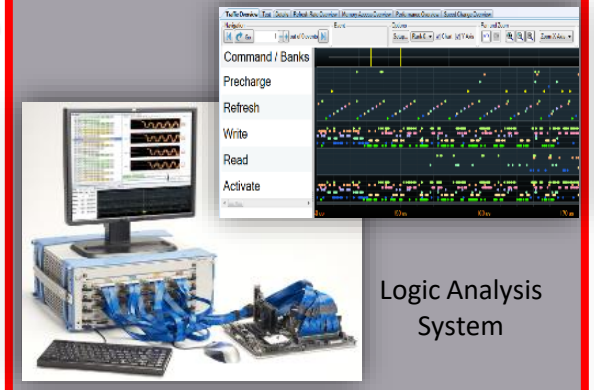
Signal Integrity

Infiniium V-Series Scope

Software Compliance Applications for all generations of DDR and LPDDR memory

M8020 High-Performance JBERT

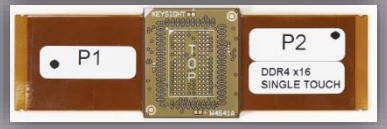
Protocol/Bus Level SI



Logic Analysis System

This presentation is about protocol solutions

Custom & Standard Probing & Interposer Solutions



Why Test and Perform Protocol Validation?

MEMORY SYSTEMS DON'T ALWAYS BEHAVE AS EXPECTED.

Debug – something is wrong with your system.

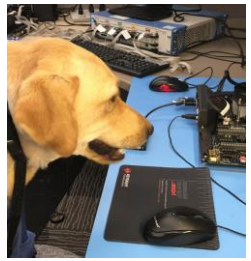
- See the flow of the traffic between the memory controller and memory device to get to the root cause of system issues
- Correlate memory traffic to scope capture of:
  - Signal integrity of specific signals
  - Power integrity

Test

- Test and monitor your system under variable conditions.

Functional Compliance Validation

- Validate system is within JEDEC specifications.
- If not…..risk of system failures



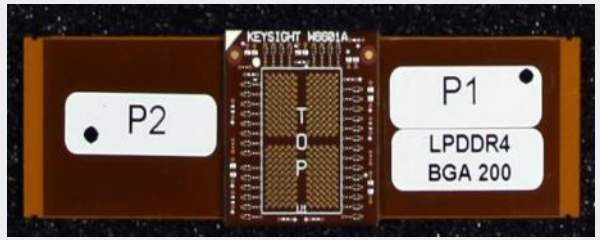
Choose Probing for Memory Form Factor

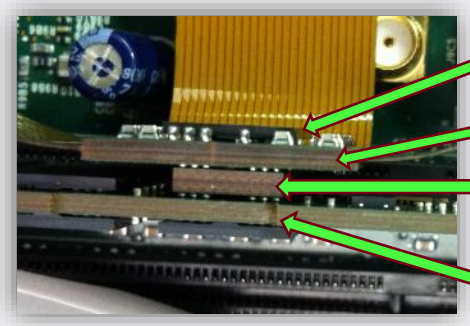
ACCURATE, RELIABLE PROBES TO CONNECT TO ANY SYSTEM

DIMM and SODIMM Interposers

For chip down applications

BGA Interposers



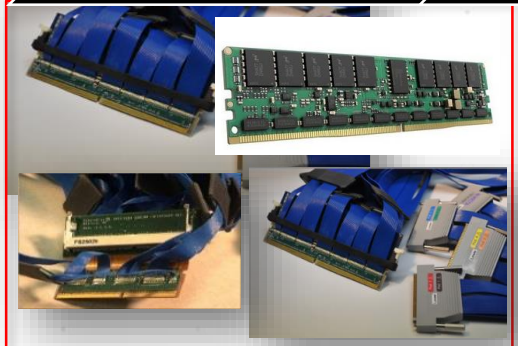


Mid-Bus Probing
(footprint must be designed into system under test)

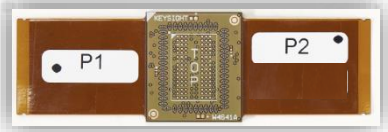
Custom probes to meet unique requirements are also possible.

Protocol Debug, Test, and Compliance Validation

Connect



DDR4/5 RDIMM/LRDIMM,
UDIMM and SODIMM
Interposers
FuturePlus Systems



Keysight DDR BGA
Interposers

DDR5, LPDDR5 or ONFi (Oopen NAND Flash interface) common footprint probing or custom probing

Acquire

Capture highest data rates!
Address, command, DQ
DDR4 captures proven at 4200 MT/s

Capture smallest eyes
100mV x 100ps at probe point.

Sequential Triggers up to 2.5GHz or
4200Mb/s

12.5GHz Timing Zoom
256k deep

Up to 400M deep traces

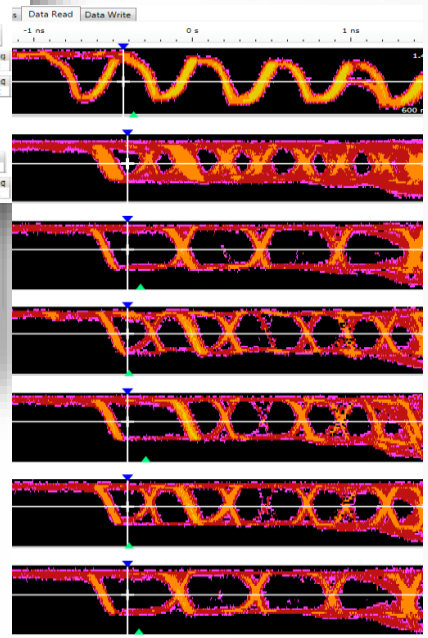
U4164A Logic Analyzer Module

View & Analyze

Memory Analysis
Traffic Overview
Protocol Compliance
Performance Analysis
Waveforms
Correlation to scope SI and Power Integrity traces.

DDR5 Analysis and Compliance Validation.

LPDDR5 Analysis and Compliance Validation.

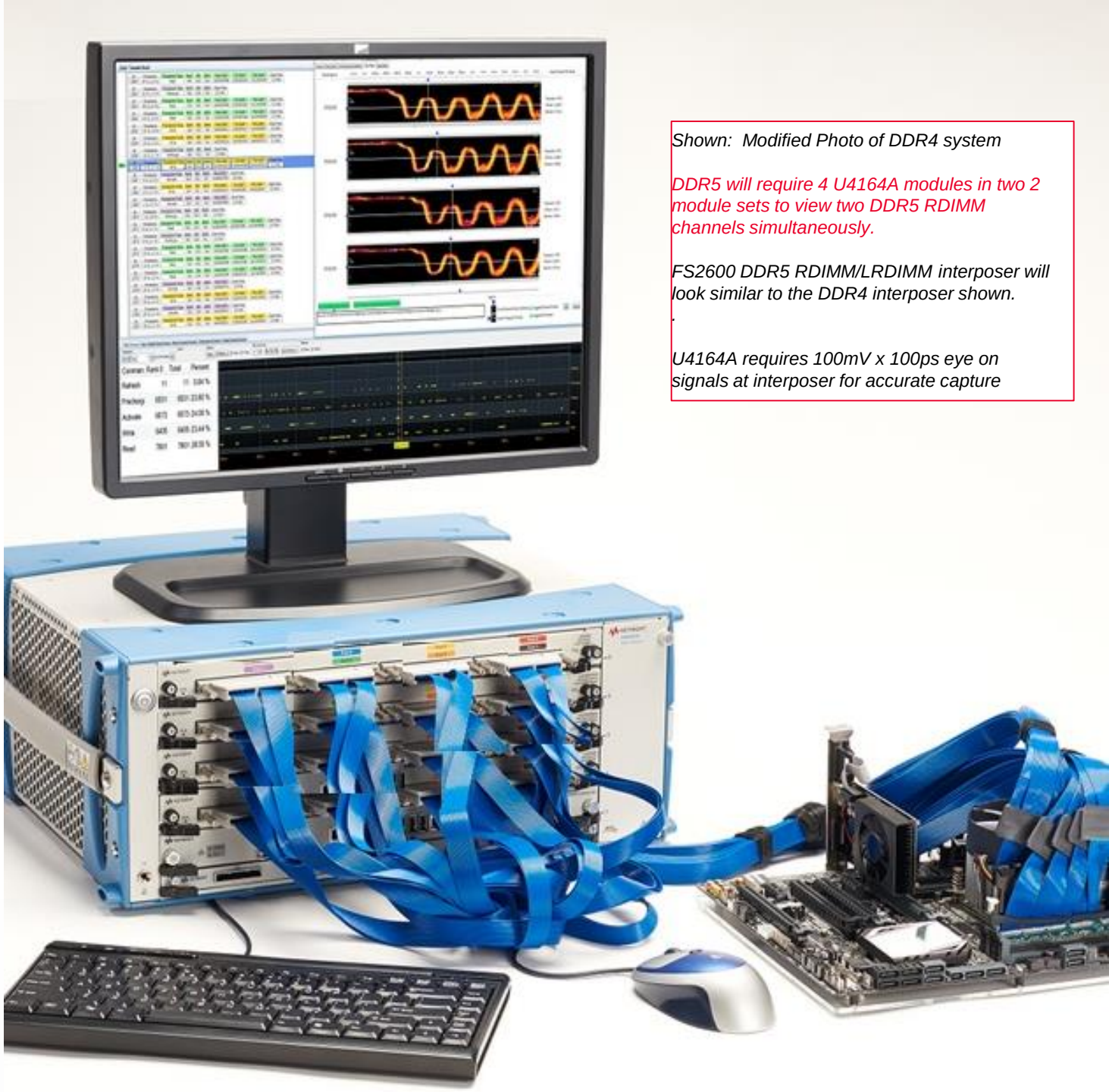


Bus Level Signal Integrity Insight

Example: DDR4
4200MT/s Read DQ

DDR5 configuration for RDIMM or LRDIMM

- Qty (4) U4164A logic analyzer modules qty (2) sets of 2 modules
  - Qty (4) option -02G speed grade option
  - Qty (4) optional customer choice of memory depth options
- Qty (1) M9505A chassis
- Qty (1) M9537A embedded controller
- Qty (1) FS2600 DDR5 RDIMM/LRDIMM Interposer
- Qty (1) B4661A Memory Analysis SW
  - Qty (1) B4661A-5FP/5TP/5NP
    DDR5 Analysis and Compliance Validation



Shown: Modified Photo of DDR4 system

DDR5 will require 4 U4164A modules in two 2 module sets to view two DDR5 RDIMM channels simultaneously.

FS2600 DDR5 RDIMM/LRDIMM interposer will look similar to the DDR4 interposer shown.

U4164A requires 100mV x 100ps eye on signals at interposer for accurate capture

KEYSIGHT TECHNOLOGIES

DDR4 configuration for RDIMM, LRDIMM or UDIMM

- U4164A logic analyzer modules
  - Qty (3) each with option -02G for all ADD/CMD/DQ
- M9505A chassis
- M9537A embedded controller
- PS-X10-650-3PH Interposer FS2520 DDR4 4Gb/s 288 pin DIMM
- B4661A Memory Analysis SW
  - B4661A -1TP/1FP/1NP DDR Decoder
  - B4661A - 2TP/3FP/3NP Compliance Analysis
  - B4661A - 4TP/4FP/4NP Performance Analysis

Proven to 4.2GT/s!

KEYSIGHT TECHNOLOGIES

Accelerate Debug Test & Compliance Validation

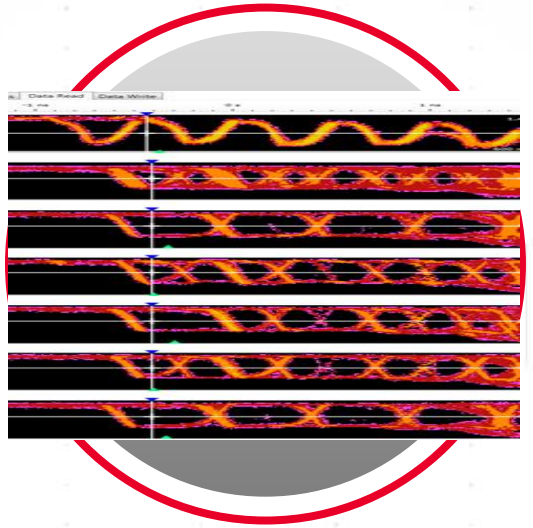
Memory Analysis

Follow the Signal flow

Rapid navigation

Performance Insight

Compliance Validation



Setup Tools for Memory Solutions

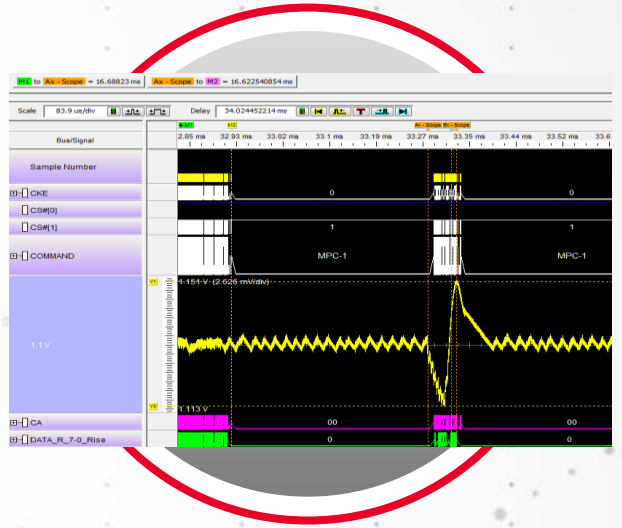
DDR Setup Assistant

Enables semi-automated setup

DDR Eyescan

Bus Level Signal Integrity Insight

Qualitative view of all eyes



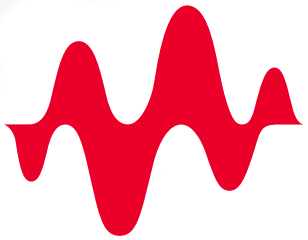
Correlate memory analysis to Power Integrity or signal integrity probing

Visualize noise on power or signal integrity issues correlated to LPDDR5 bus activity

Summary

- Keysight is working with JEDEC and early adopters to lead the definition of the measurement methodologies.
- Keysight's goal is to ensure that our customers can be confident that they are testing all the parameters required for their device to interoperate and that the measurement method used is consistent to what is agreed in the industry.
- Keysight offers the most comprehensive solution package which includes best performance test equipment for making the most accurate measurements.

Q&A



KEYSIGHT
TECHNOLOGIES