Advanced Techniques for Validating the Latest Generation of PCIe Transmitters and Receivers

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KEYSIGHT TECHNOLOGIES

Agenda

- PCI Express 4.0 Timeline and 5.0 Roadmap
- PCI Express 4.0 TX / LTSSM Link EQ / RX Testing
- PCI Express 5.0 Preview

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- **PCI Express 4.0 Timeline and 5.0 Roadmap**
- PCI Express 4.0 TX / LTSSM Link EQ / RX Testing
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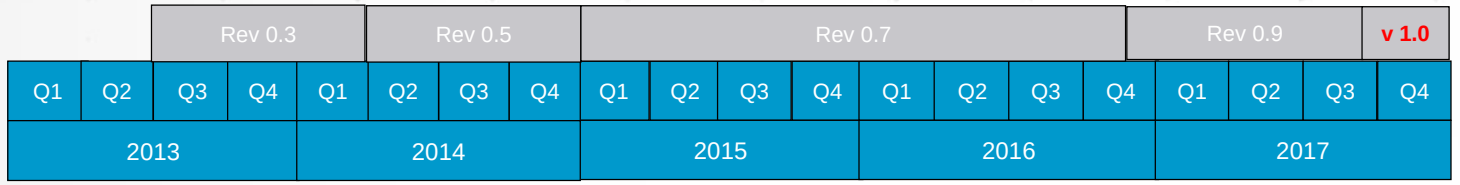
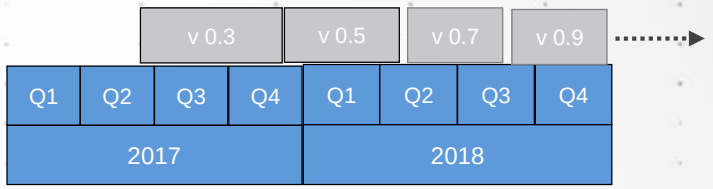
PCI Express 4.0 Timeline & 5.0 Roadmap

PCIe 4.0



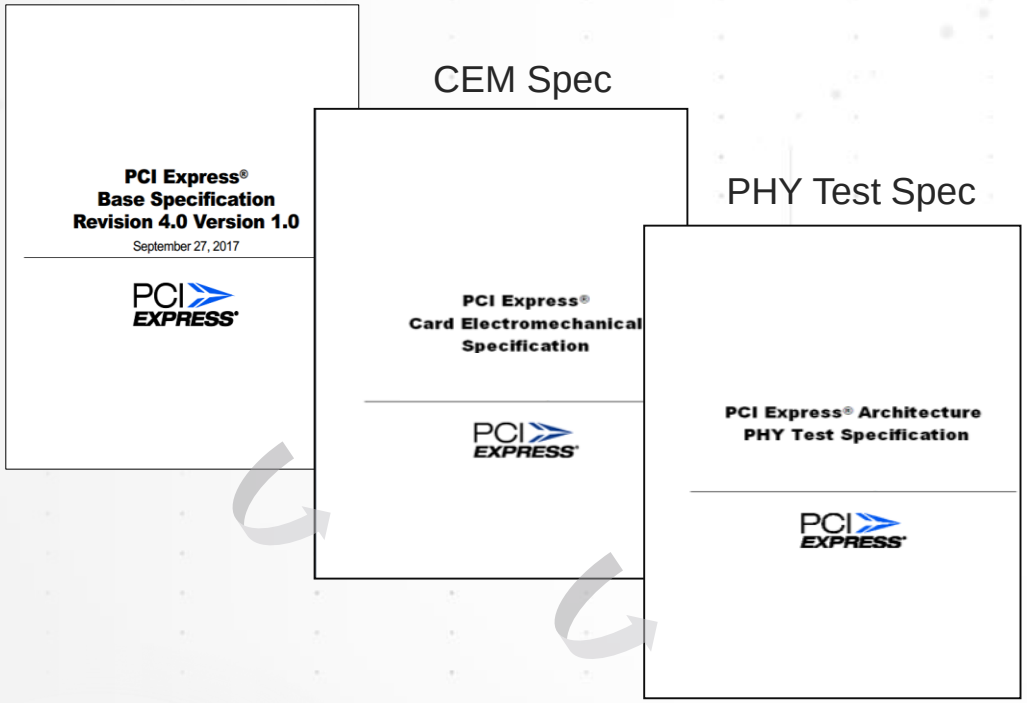
PCIe 5.0

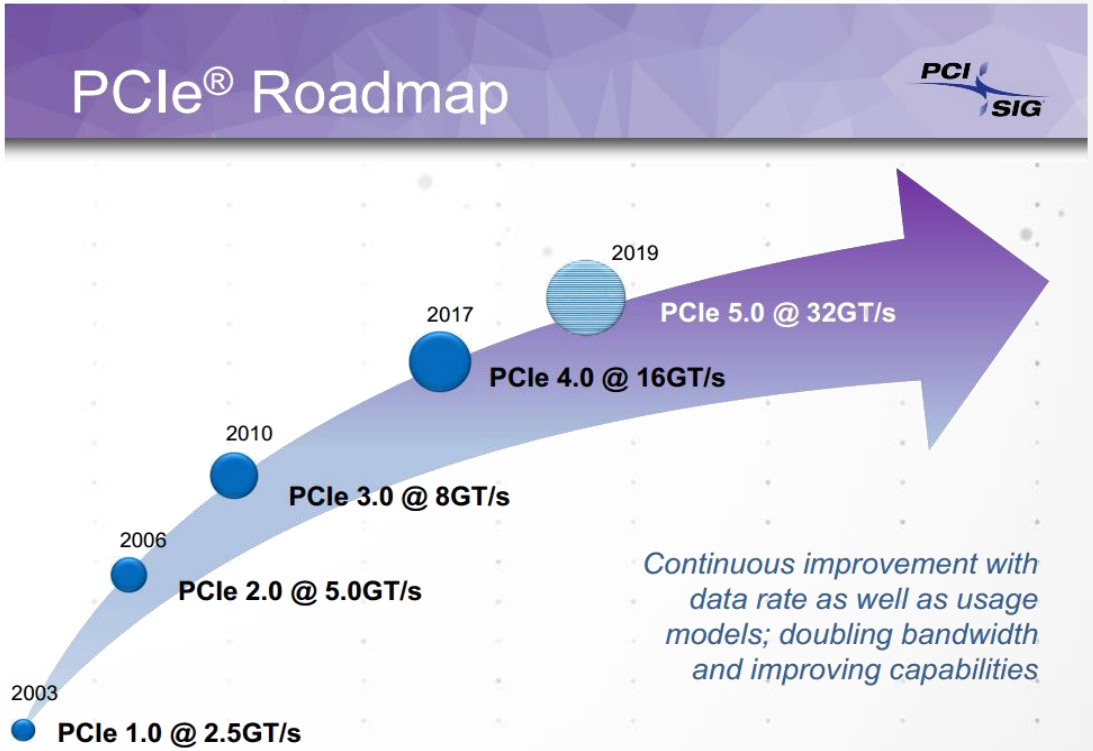


Base Spec

CEM Spec

PHY Test Spec





Continuous improvement with data rate as well as usage models; doubling bandwidth and improving capabilities

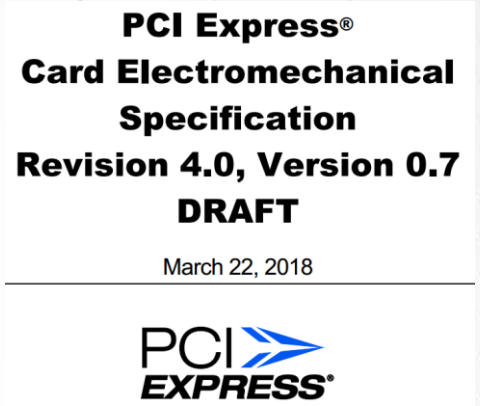
PCI Express 4.0 New Features

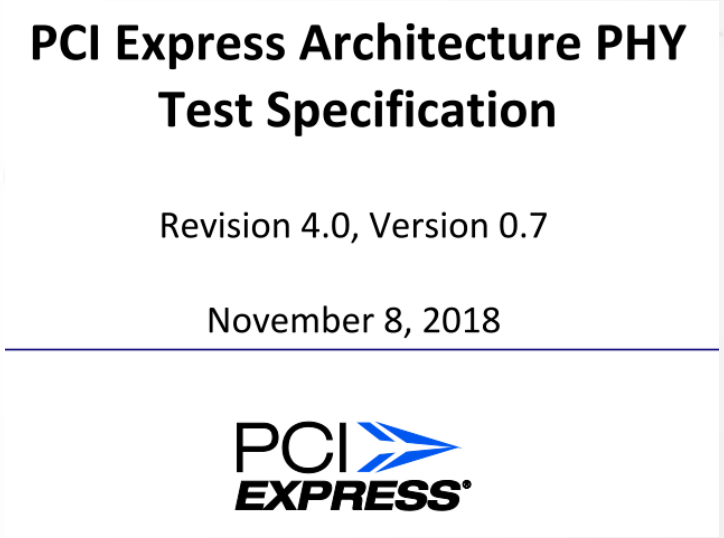
Based on PCIe v1.0 BASE specification

- **New data rate:16GT/s**
  - Requires an output stages capable of providing pre-shoot and de-emphasis with fast enough rise-times.
- **Link Equalization protocol similar to PCIe 3.0**
  - TxEQ P0-P10
  - RxEQ CTLE (2 pole 1 zero) + 2tap DFE
- **Max Channel Loss -28dB @ 8GHz & 1 connector**
  - Re-timers used for longer channels or for channels with >1 connector
- **RX clocking architectures: CC and IR**
  - CC -> Common RefClock -> synchronous RX and TX w/ or w/o SSC
  - IR -> Independent RefClock -> asynchronous RX and TX w/ or w/o SSC
- **Initial LinkEQ speed selection: 2.5GT/s -> 8GT/s with link equalization**
  - if successful -> Then transitions to 16GT/s with another round of link equalization
- **TX Jitter Analysis: Similar to PCIe 3.0**
- **RX Lane Margining added.**

CEM 4.0 and Compliance Testing

- **CEM 4.0 currently at v0.7**
  - V0.7 in CEM Review
- **PCIe 4.0 Compliance Requirements**
  - CEM Spec completion at v0.7 (v0.9 optimal)
  - Completion of Test Specifications
    - Config Test Spec
    - Link Transaction Test Spec
    - System Firmware (BIOS) Test Spec
    - Electrical Test Spec
    - Retimer Test Spec
  - Availability of Gen4 Compliance Test Fixtures for Purchase
    - New order collection in Nov.
  - Estimated Schedule
    - First Gen4 FYI testing commenced April 2017
    - Official FYI Testing to begin 2018
    - PCI-SIG Developers Conference 2018 is returning to Santa Clara, June 5-6, 2018
    - Official Integrators list test to start mid 2018





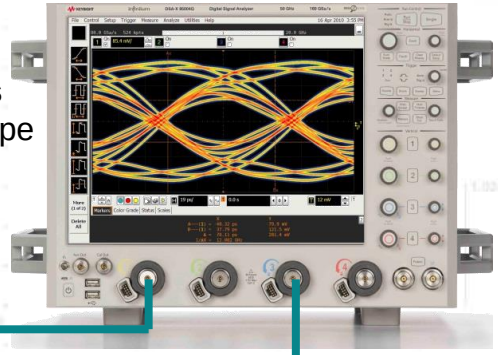
Agenda

- PCI Express 4.0 Timeline and 5.0 Roadmap
- **PCI Express 4.0 TX / LTSSM Link EQ / RX Testing**
- PCI Express 5.0 Preview

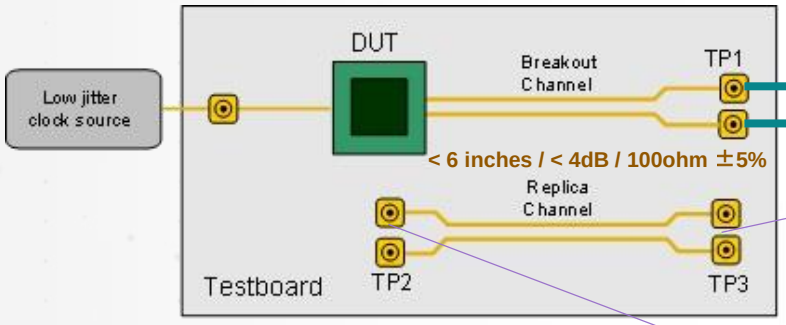
PCIe 4.0 Base Spec TX Measurement Basic Test Setup
Tx Test Scope Bandwidth Requirement

BASE SPEC (V1.0)

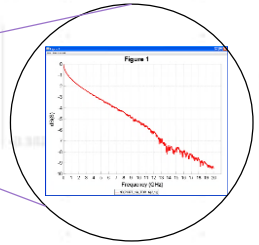
Keysight Z-Series
Real Time Oscilloscope



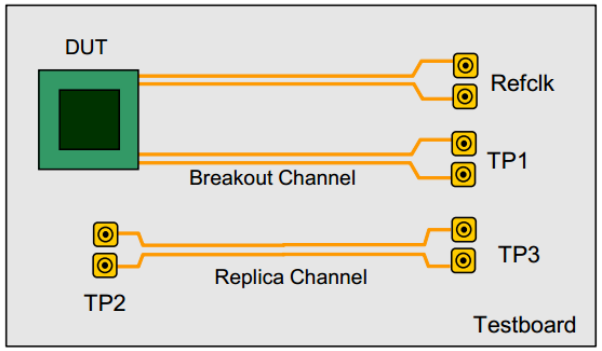
PCIe 4.0 ASIC/IC
Custom Breakout Board



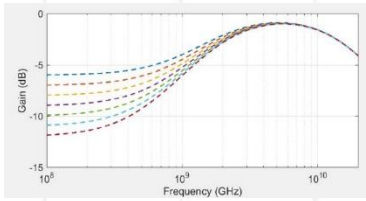
Tx Test Board for Non-Embedded Refclk



S-Parameters of Replica Ch.
Used to de-embed to pin.



Tx Test Board for Embedded Refclk



Ref CTLE can be used (12dB).

8.3.5.2 *Applying CTLE or De-embedding*

Direct probing at a Transmitter's pins is not generally feasible, so data is instead measured at TP1 of the breakout channel. By means of the replica channel it is possible to determine the loss vs. frequency characteristics of the breakout channel and de-embed this channel, resulting in measurements that are effectively referenced to the DUT's pins. Note that since de-embedding amplifies HF noise there is a practical frequency cutoff limit to de-embedding. As de-embedding amplifies HF channel and measurement noise, an HF cutoff limit of 8GHz-12GHz and 20 GHz (3dB point) must be applied to de-embedding, depending on data rate as shown in Table 8-5.

Table 8-5: Recommended De-embedding Cutoff Frequency

Data Rate	HF Cutoff limit for (
8GT/s	8GHz-12 GHz
16GT/s	20GHz

20GHz
De-embed limit

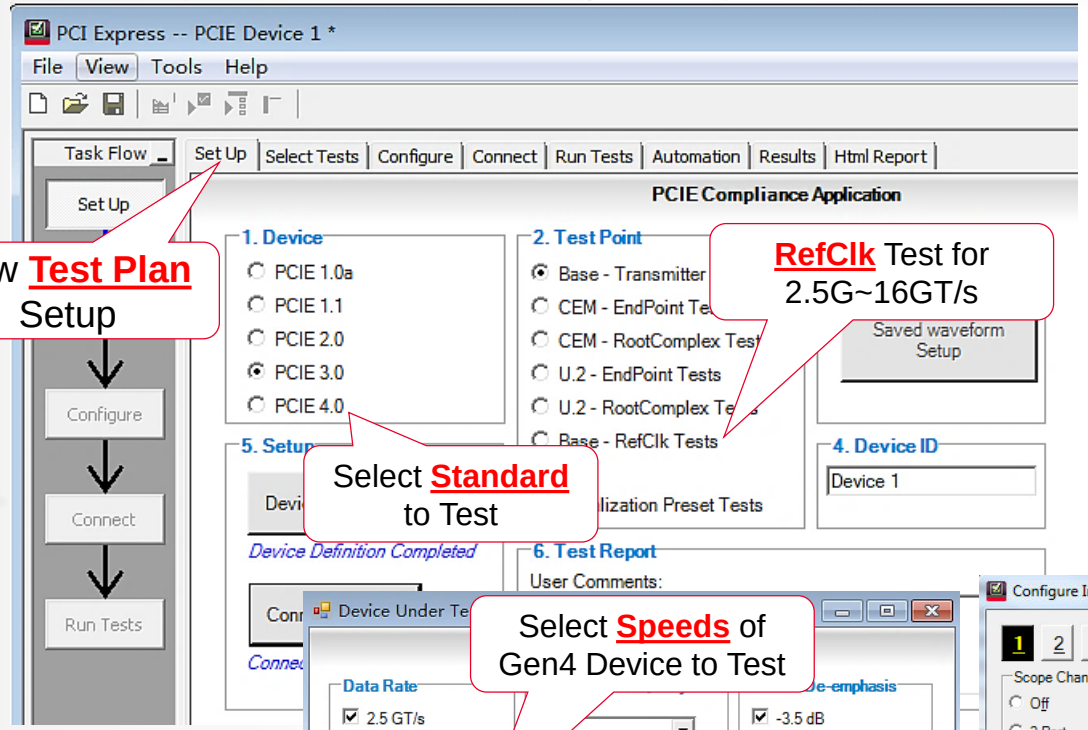
8.4.2.1 *Procedure for Calibrating a Stressed EH/EW Eye*

As the calibration procedure of the signal generator output contains steps where the generator is connected directly to measurement instrumentation, the transition time of the output waveform can be very fast. Therefore, it is important that the bandwidth of instrumentation used to calibrate the generator be matched appropriately to the edge rate of the generator output. This specification requires the use of a generator whose outputs have a rise time of 14ps-19ps (20% / 80%) which also requires a minimum oscilloscope bandwidth of 25GHz. This oscilloscope bandwidth is also the minimum required bandwidth for transmitter measurements.

25GHz
Min Scope BW

PCIe 4.0 TX Test with Keysight N5393F Application

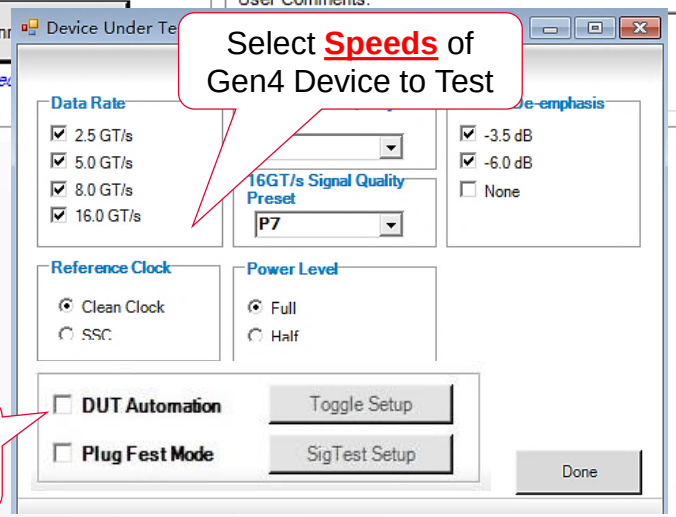
Compliance Test SW Features



New **Test Plan** Setup

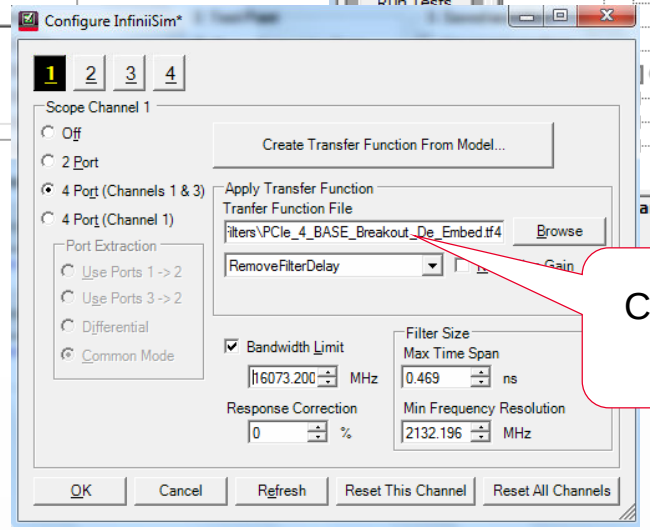
RefClk Test for 2.5G~16GT/s

Select **Standard** to Test

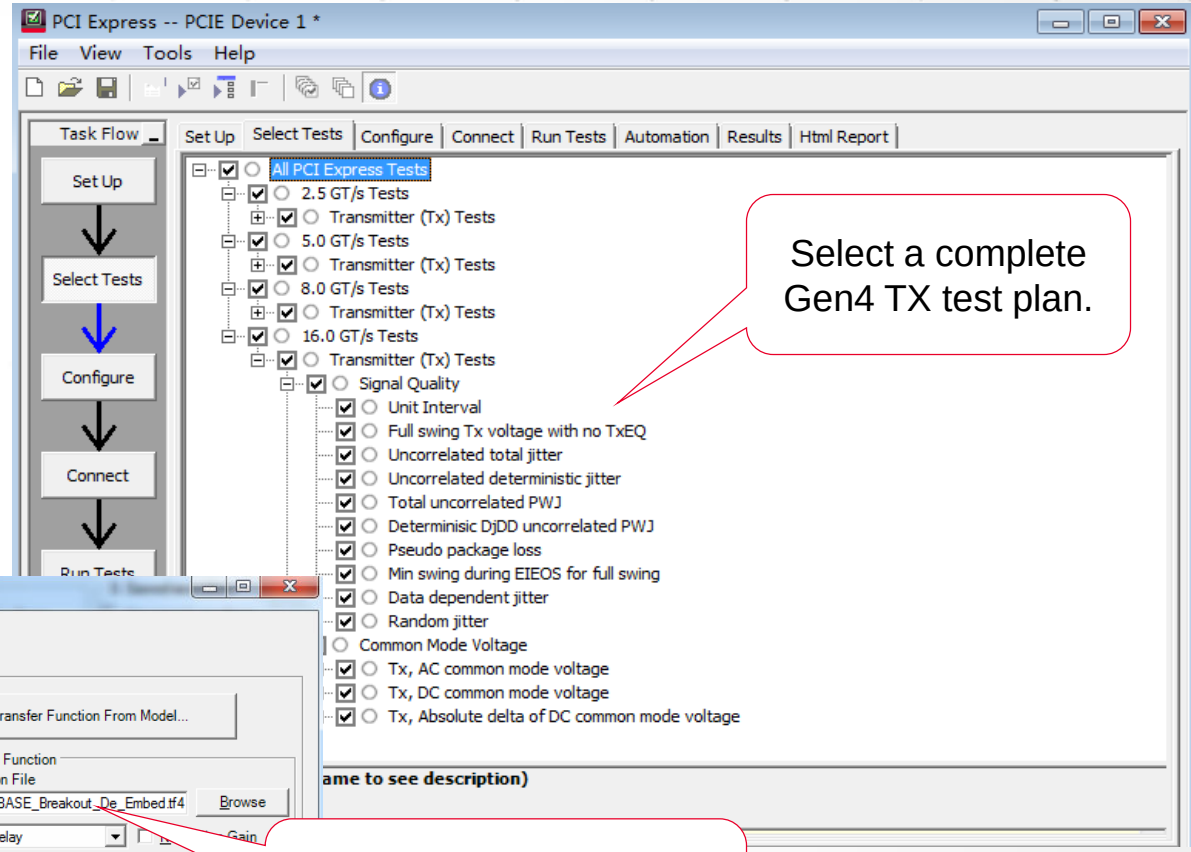


Select **Speeds** of Gen4 Device to Test

Automatic DUT control for toggle signal



Choose your **de-embed** transfer function



Select a complete Gen4 TX test plan.

PCIe4.0 Reference Clock Measurement

Show Spec in Report

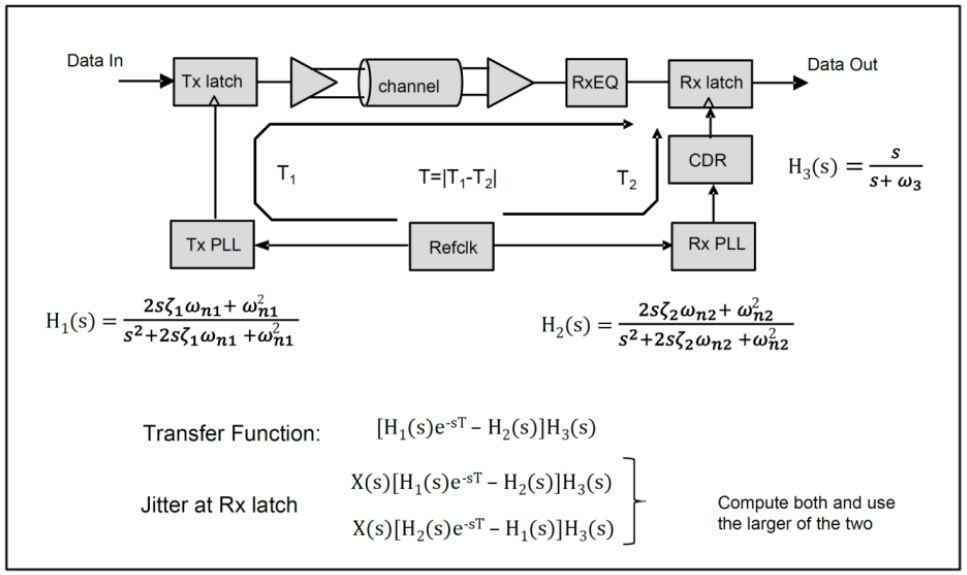
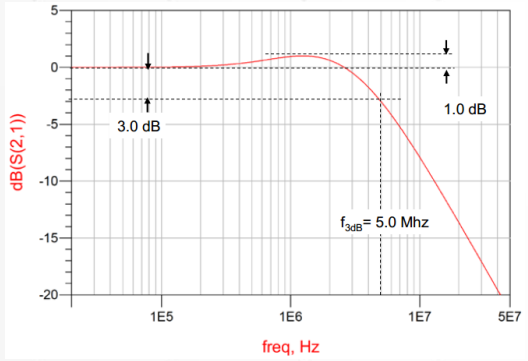


Figure 8-57: Common Refclk Rx Architecture

Table 8-21: Common Refclk PLL and CDR Charact istics for 8.0 and 16.0 GT/s

PLL #1	0.01 dB peaking	2.0 dB peaking	PLL #2	0.01 dB peaking	1.0 dB peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n1}= 0.448 Mrad/s ζ_1 = 14	ω_{n1}= 6.02 Mrad/s ζ_1 = 0.73	BW_{PLL}(min) = 2.0 MHz	ω_{n2}= 0.448 Mrad/s ζ_2 = 14	ω_{n2}= 4.62 Mrad/s ζ_2 = 1.15
BW_{PLL}(max) = 4.0 MHz	ω_{n1}= 0.896 Mrad/s ζ_1 = 14	ω_{n1}= 12.04 Mrad/s ζ_1 = 0.73	BW_{PLL}(max) = 5.0 MHz	ω_{n2}= 1.12Mrad/s ζ_2 = 14	ω_{n2}= 11.53 Mrad/s ζ_2 = 1.15
BW_{CDR}(min) = 10 MHz, 1st order	64 combinations			8.0, 16.0 GT/s	

REF Clock 8G TX Phase Jitter									
		PLL1				PLL 2			
		ATX	BTX	CTX	DTX	ATX	BTX	CTX	DTX
PLL 1	ARX								
	BRX								
	CRX				0.3 ps	7.9ps	0.99		
	DRX								
PLL 2	ARX								
	BRX								
	CRX								
	DRX								



PLL Jitter Transfer Function Example

If user right clicks on a curve, pop up menu shows curves related to the calculation of that value.

Color code fields for PASS/Fail/Margin

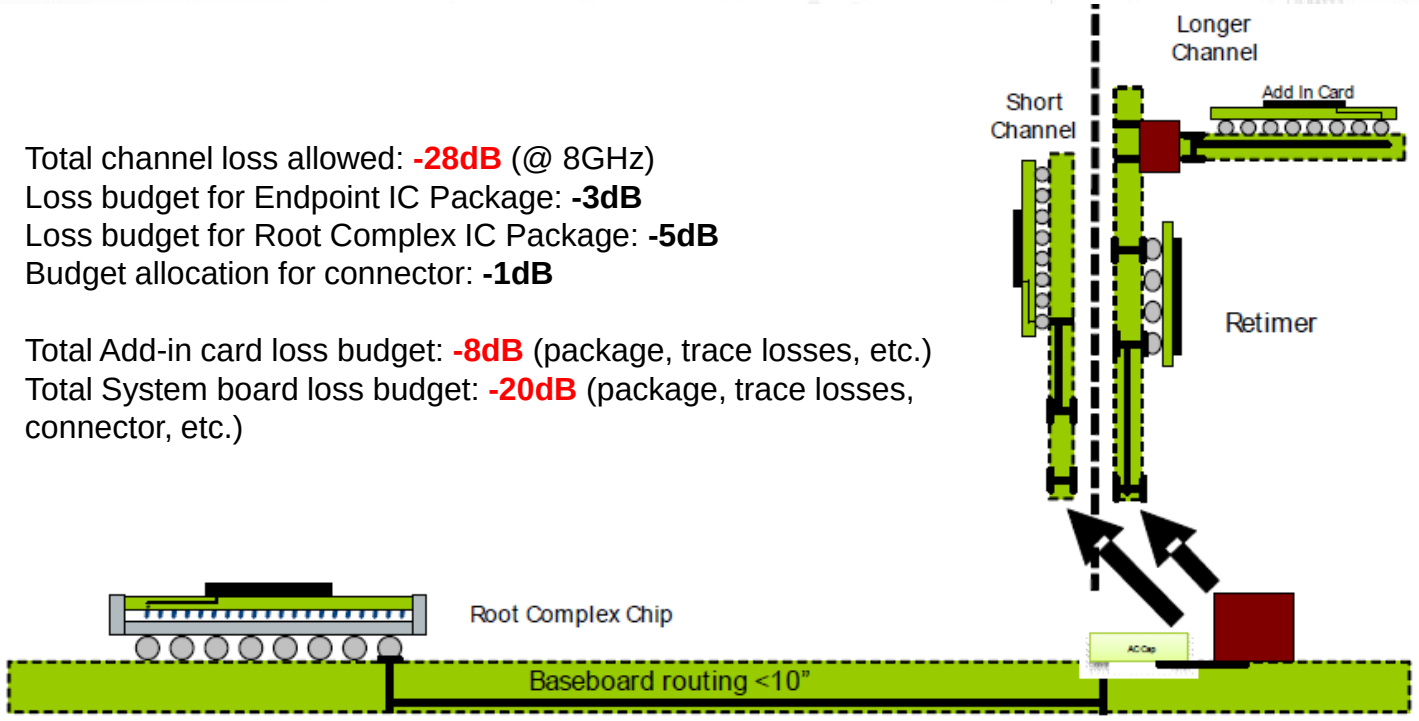
Report Results in a Matrix

PCI Express Channels for PCIe 4.0

- Card Electromechanical (CEM) form factor
  - ✓ Channel length limited to ~12 inches and one connector.
  - ✓ Retimer required if longer channel or more than 1 connector required.
  - ✓ Maximum 2 Retimers are permitted between Upstream and Downstream.

- Total channel loss allowed: **-28dB** (@ 8GHz)
- Loss budget for Endpoint IC Package: **-3dB**
- Loss budget for Root Complex IC Package: **-5dB**
- Budget allocation for connector: **-1dB**

- Total Add-in card loss budget: **-8dB** (package, trace losses, etc.)
- Total System board loss budget: **-20dB** (package, trace losses, connector, etc.)



PCIe 4.0 CEM TX Test Requirements

PCIe 4.0 (System) Tx Signal Quality Test at 16 GT/s

Scope BW is set to **25GHz** for CEM compliance

- **Channel Setup**
  - CLB plugs into system -> Variable ISI Board -> Scope
  - 8dB at 8GHz of additional loss (including package em… ing)
- **Power on System**
- **Scope bandwidth = 25GHz**
- **3dB package model embedded on scope**
- **Toggle DUT to transmit 16GT/s Compliance Pattern**
  - 1ms pulse of 100MHz clock signal into Rx Lane0
- **Capture 2.0M UI waveform for every Tx EQ Preset**
- **Waveforms post processed using SigTest**
  - Ref clock captured with data waveform and used for clock recovery
  - Behavioral Rx …
  - Eye width & Ey…
  - Each lane mus…
    - EW > 0.3UI
    - EH > 15mV

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PCIe 4.0 (Add-in Card) Tx Signal Quality Test at 16 GT/s

Scope BW is set to **25GHz** for CEM compliance

- **Channel Setup**
  - Add-in Card plugs into CBB -> Variable …
  - 20dB at 8GHz of additional loss (includi… kage embedding)
- **Power on CBB**
- **Scope bandwidth is 25GHz**
- **5dB package model embedded on scope**
- **Toggle DUT to transmit 16GT/s Compliance Pattern**
  - 1ms pulse of 100MHz clock signal into Rx Lane0
- **Capture 2.0M UI waveform for every Tx EQ Preset**
- **Waveforms post processed using SigTest**
  - Time Domain CDR algorithm used to recover clock
  - Behavioral Rx Equalization applied
  - Eye width & Eye height @ E-12
  - Each lane must pass SigTest analysis for at least one Tx EQ Preset
    - EW > 0.3UI (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)
    - EH > 15mV (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)

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The system board Transmitter path measurements at 16.0 GT/s are made using a two-port measurement methodology. Figure 33 shows a functional block diagram for a system board and Add-in Card that shows the measurement points for the two-port method.

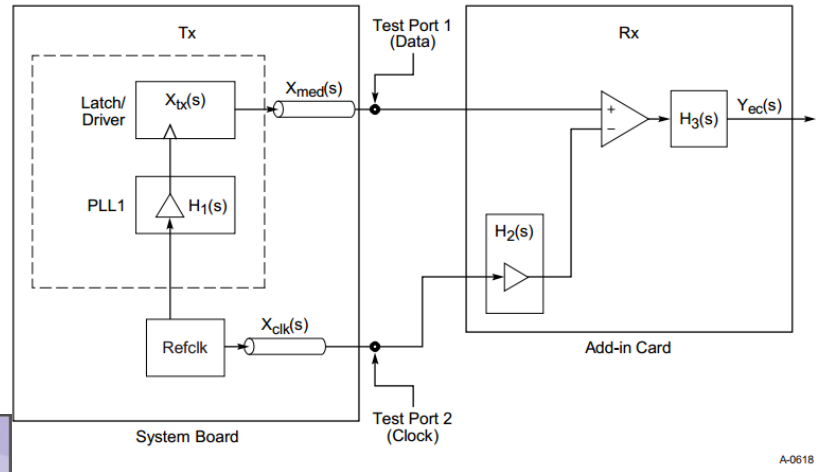


Figure 35: 16 GT/s Two Port Measurement Functional Block Diagram

Keysight Z-Series 25GHz RT Oscilloscope

Dual Port Test (4 Channels) with 25GHz BW
D+ D- CLK+ CLK- Capture Simultaneously

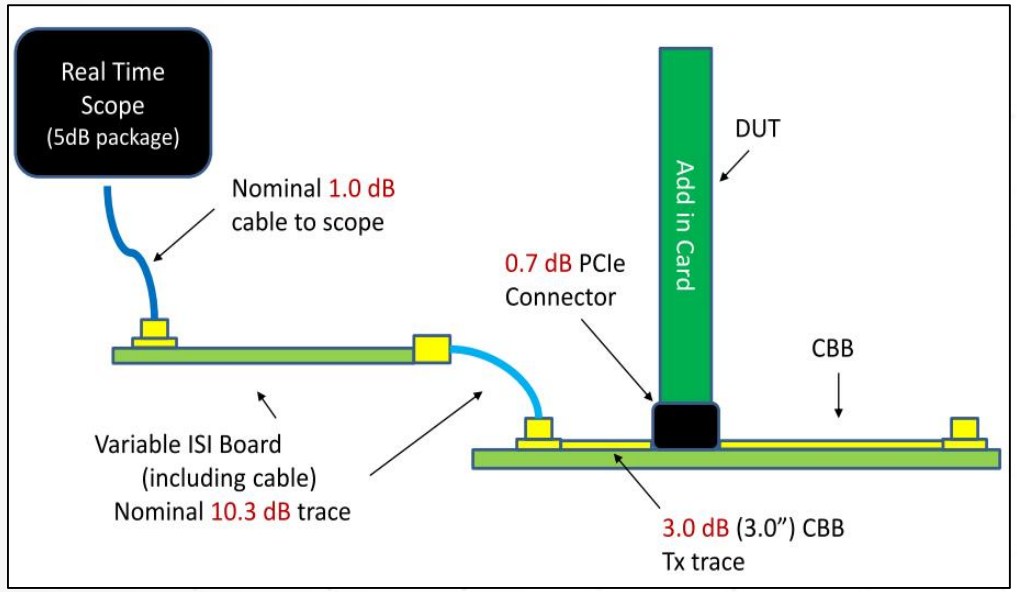
2.8.3. System Board Transmitter Electrical Compliance Test for 16.0 GT/s s

1. Connect the Tx lane under test to the input of the CBB Variable ISI board (choosing the lane which gives a total loss of 15dB @ 8GHz). Connect the output of the CBB Variable ISI board to a high speed oscilloscope or equivalent data capture instrument via low loss SMA cables.
2. If the correct Transmitter Equalization setting is known, push the compliance toggle button on the CLB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the motherboard under test) until the correct Tx EQ is selected, otherwise push the compliance toggle button until the initial 16 GT/s Tx EQ preset is selected.
3. Measure transmitted clock and data waveforms simultaneously with a high speed oscilloscope or equivalent data capture instrument.
4. Confirm that the waveform is the correct compliance pattern.
5. Capture 1.6 million unit intervals of data (2.0 X 10^6 X 62.5ps = 100.0µs).

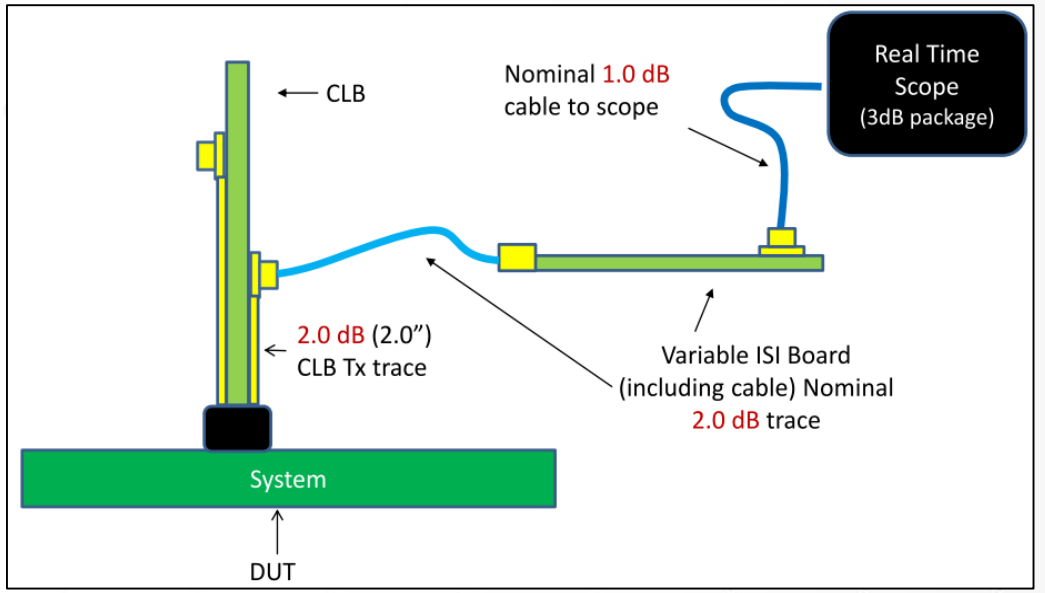
PCIe 4.0 CEM TX Test Setups

AIC and Motherboard Test Proposals

Add-in Card TX Test



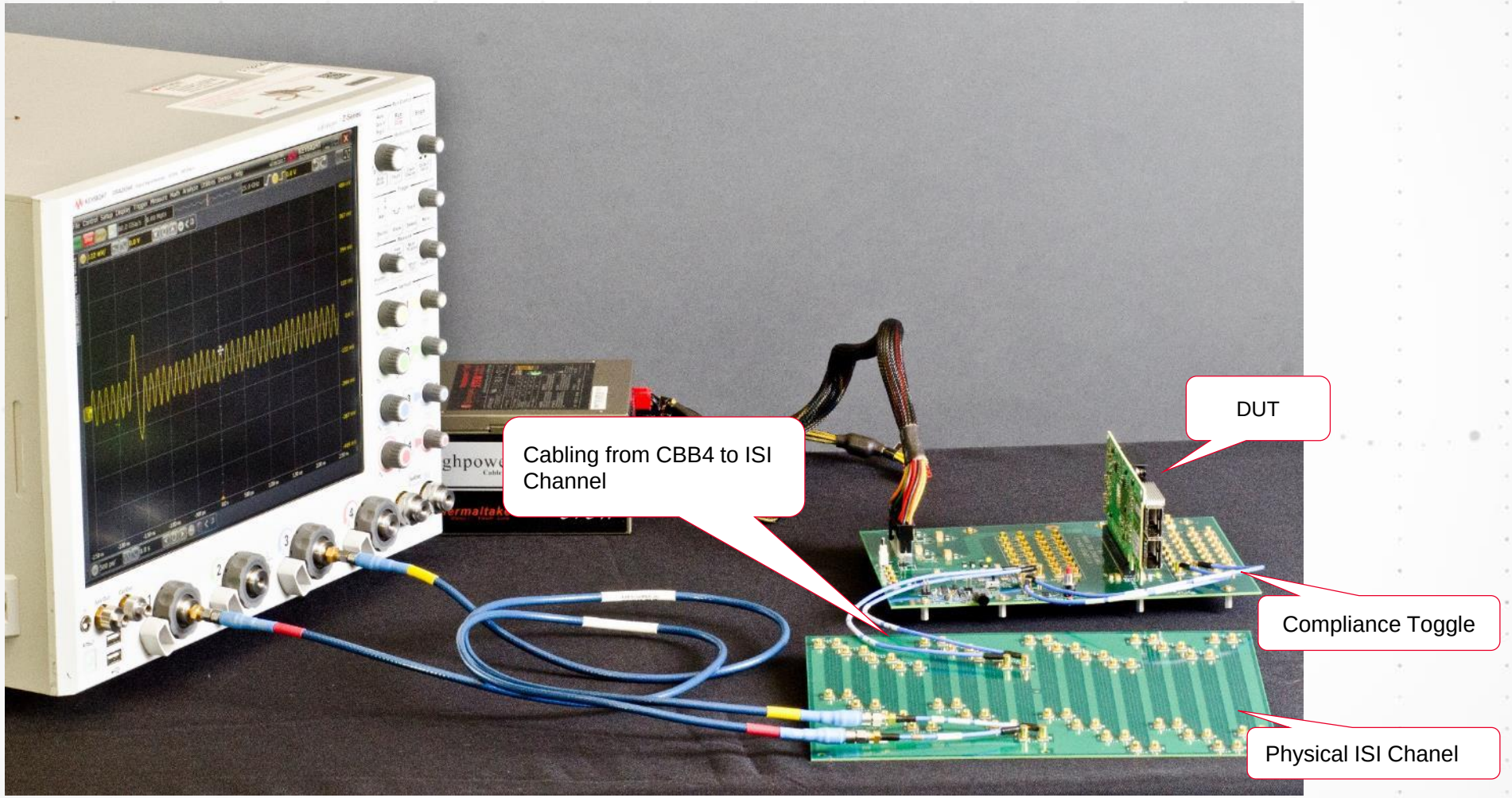
Motherboard TX Test



Note: This TX test proposal utilizes an external variable ISI board to ensure consistent insertion loss of the test setup.

PCIe 4.0 CEM TX Test Setup Example

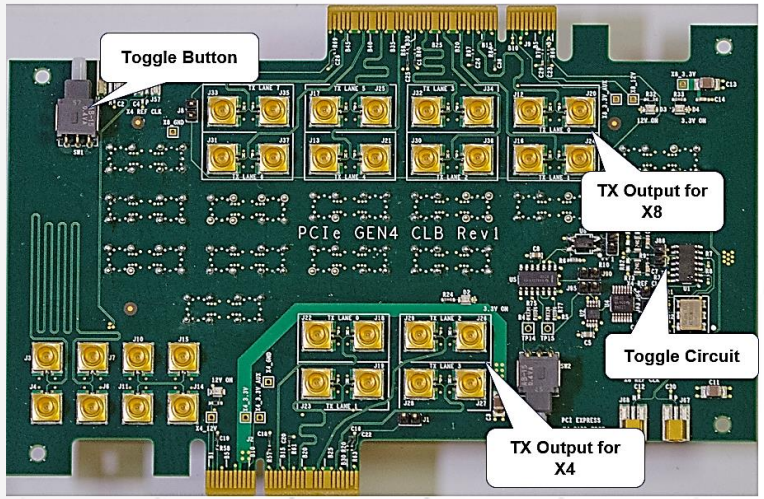
CEM AIC Setup With Scope



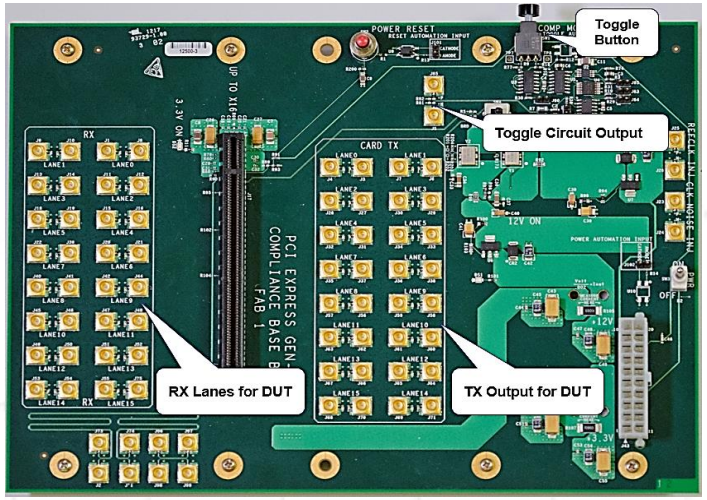
PCIe 4.0 CEM TX Test Fixtures

CEM Test Fixture Set

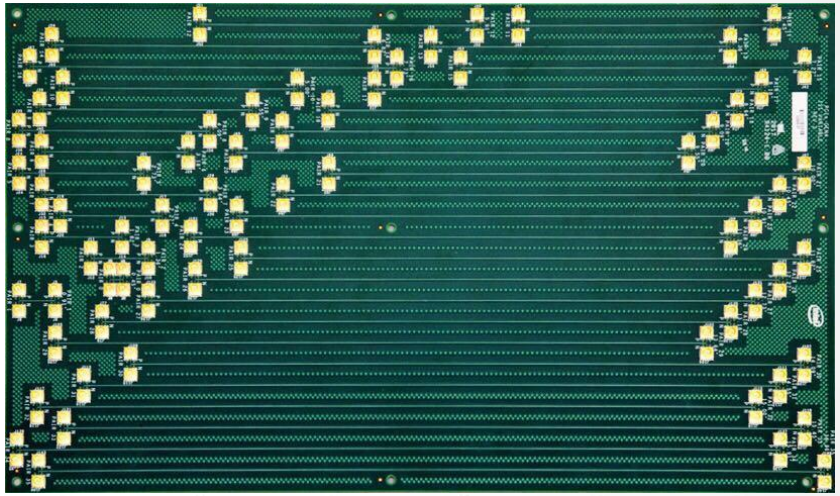
CLB4 x4-x8 Fixture



CBB4 Fixture

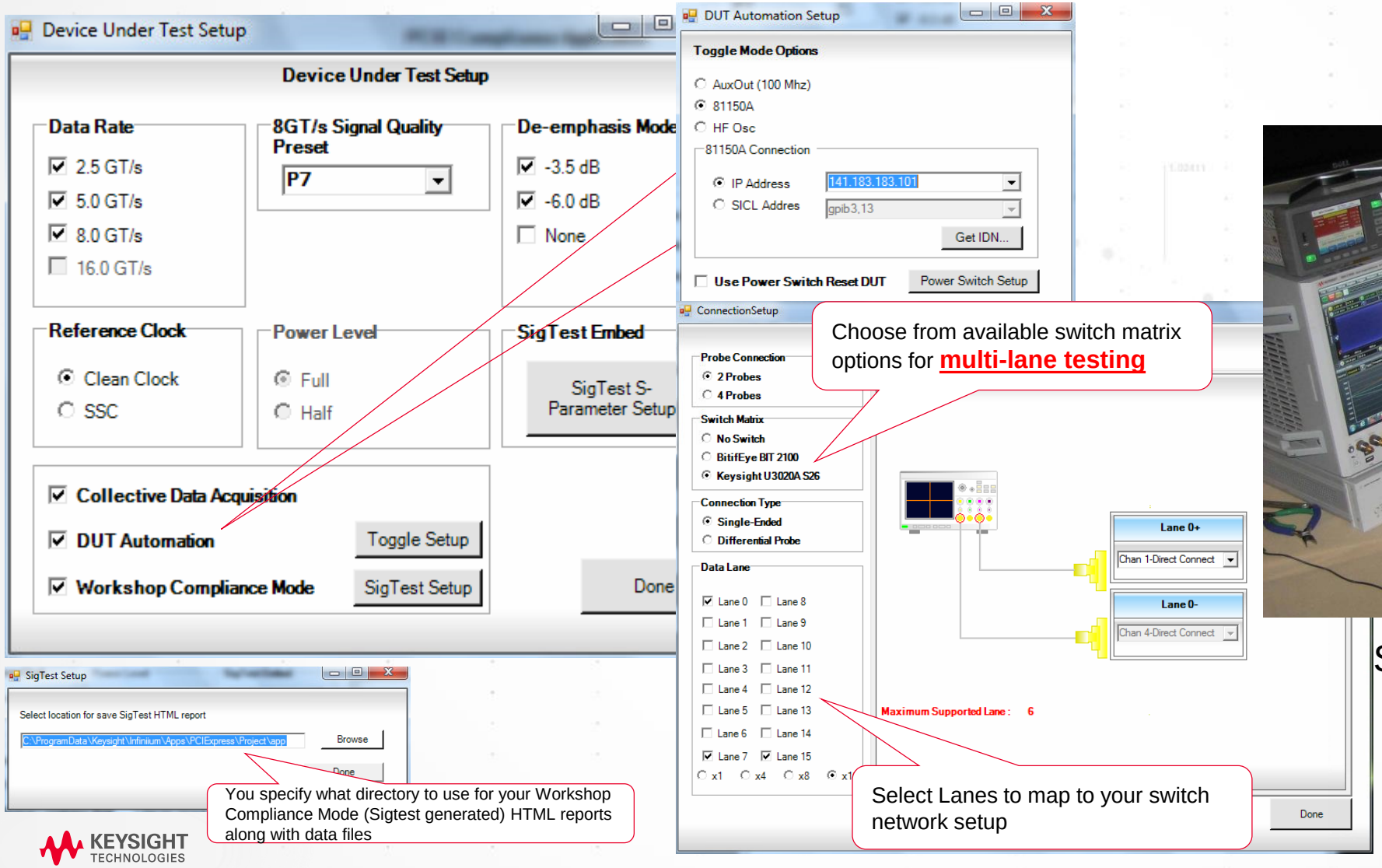


ISI Fixture



Speeding up Testing With N5393F Test Application

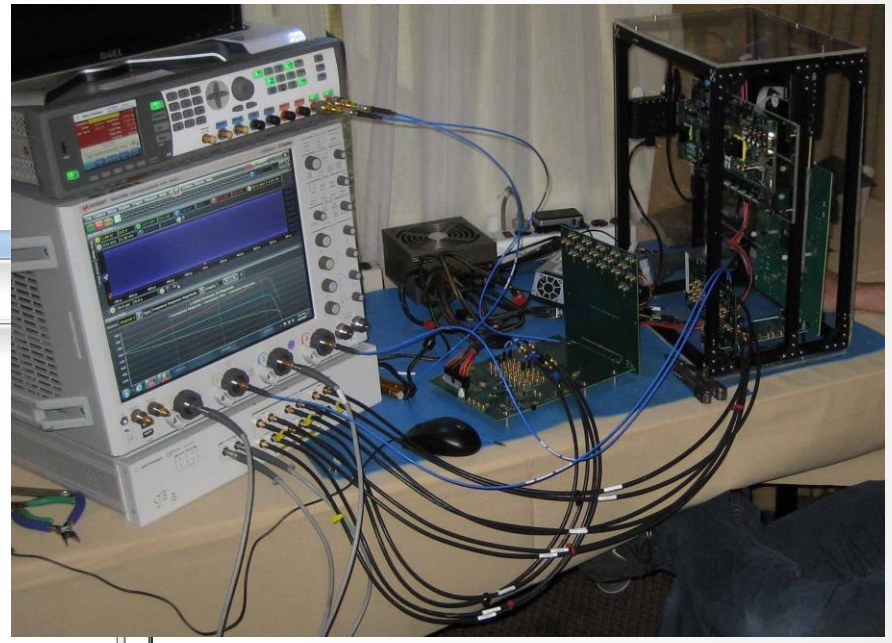
Automated DUT Control, SIGTEST Mode and Enhanced Switch Matrix Lane Mapping



Choose from available switch matrix options for **multi-lane testing**

Select Lanes to map to your switch network setup

You specify what directory to use for your Workshop Compliance Mode (Sigtest generated) HTML reports along with data files



System Automation Test Example

Gen4 Tx testing test spec. and latest SigTEST version

2.7.5 System Board Transmitter Electrical Compliance Test for 16.0 GT/s

1. Connect the Tx lane under test on the CLB to the differential pair of the Variable ISI board which provides a physical channel insertion loss of 5dB at 8 GHz (See Appendix C). Connect the output of the Variable ISI board to a high-speed oscilloscope or equivalent data capture instrument via low loss SMA cables.
2. Connect the Reference Clock (REF CLK) on the CLB to a high-speed oscilloscope or equivalent data capture instrument via low loss SMA cables.
3. If the correct Transmitter Equalization setting is known, push the compliance toggle button on the CLB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the motherboard under test) until the correct Tx EQ is selected, otherwise push the compliance toggle button until the initial 16 GT/s Tx EQ preset is selected.
4. Measure transmitted clock and data waveforms simultaneously with a high-speed oscilloscope or equivalent data capture instrument with the maximum bandwidth set to 25GHz
5. Confirm that the waveform is the correct compliance pattern.
6. Capture 2.0 million unit-intervals of data and clock ($2.0 \times 10^6 \times 62.5ps = 125.0\mu s$) simultaneously.

> **Note:** The Non-Root Complex package model will be embedded into the captured data waveform on the scope or by Sigtest. The s-parameters to be embedded are included with this specification.

7. Measure Extrapolated Eye Height and Minimum Eye Width using SigTest analysis program with the appropriate choice of template file (PCIE_4_0_SYS\ PCIE_4_16GB_CEM_DUAL_PORT.dat).
8. The SigTest analysis program will also indicate if the acquired data pattern matches the expected compliance pattern. (this check is informative)
9. If the SigTest analysis program indicates the system board Minimum Eye Width is greater than or equal to 21.75ps and Extrapolated Eye Height is greater than or equal to 19mV, the, electrical compliance test passes and is complete. If SigTest indicates the system board fails, the next Tx EQ setting should be selected (by pushing the compliance toggle button) and steps 3 through 8 of this test procedure should be repeated until the system board passes or all Tx EQ settings have been tested.

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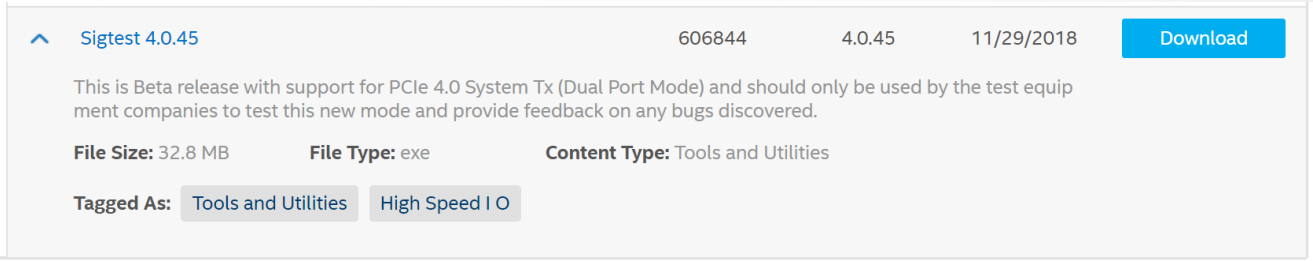


SigTest 4.0.45 test report

SYSTEM BOARD EXAMPLE

Sigtest:

- **Overall Sigtest Result: Pass!**
- **Mean Unit Interval (ps): 62.501194**
- **Min Time Between Crossovers (ps): 51.907773**

- **Data Rate (Gb/s): 15.999694**

- **Max Peak to Peak Jitter: 21.38739 ps**

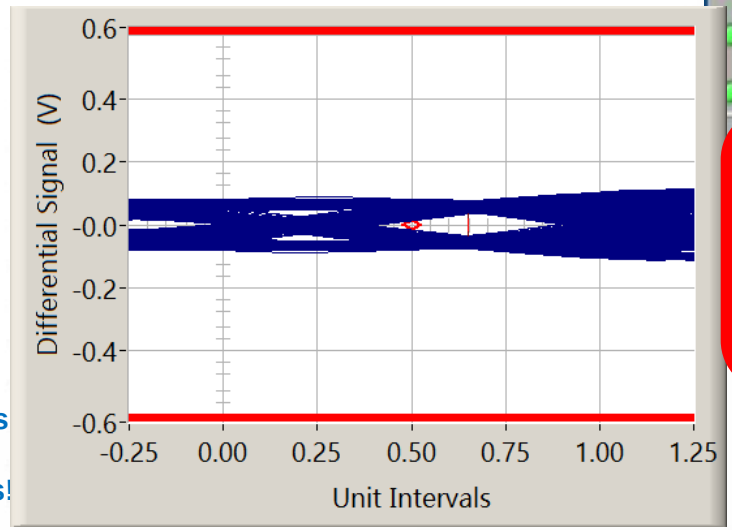
- **Total Jitter at BER of 10E-12: 22.369856 ps**
  Total Jitter at BER of 10E-12 Passes Sigtest Limits!
- **Minimum eye width: 40.130144 ps**

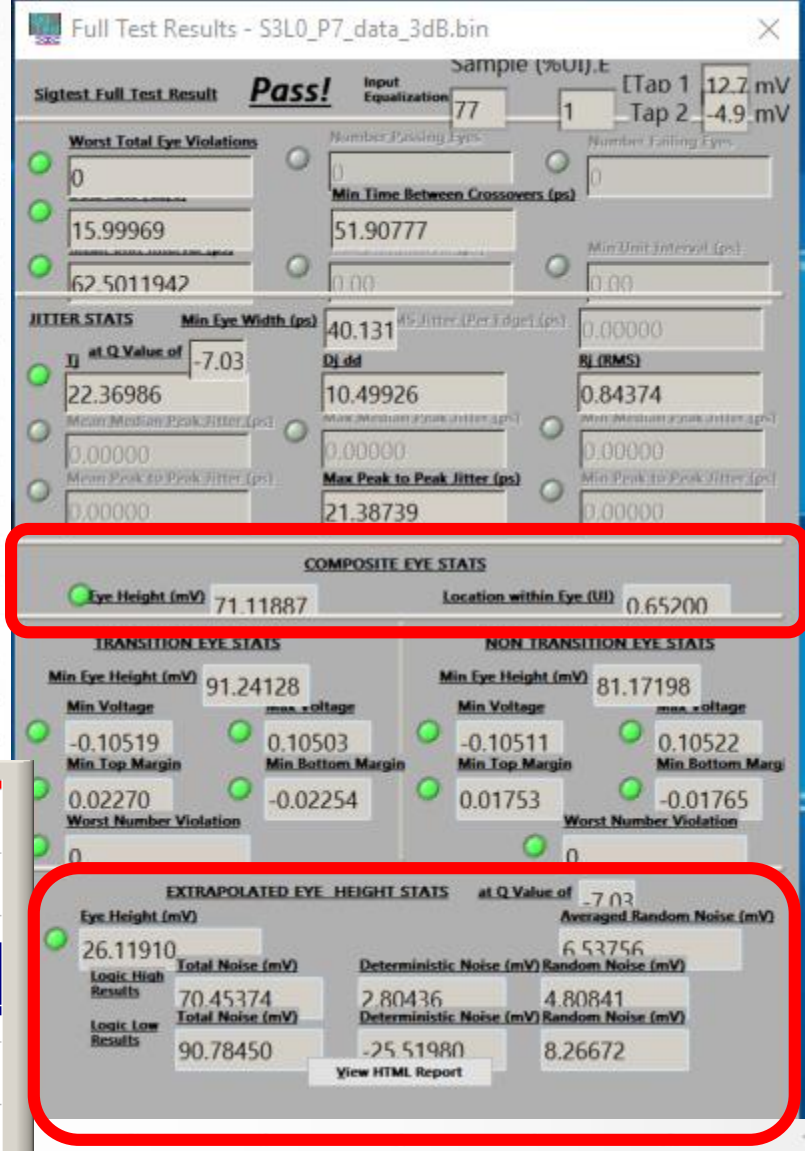
- **Deterministic Jitter Delta-Delta: 10.499261 ps**
  Deterministic Jitter Delta-Delta Passes Sigtest Limits!
- **Random Jitter (RMS): 0.843742 ps**
  Random Jitter (RMS) Passes Sigtest Limits!
- **Minimum Transition Eye Voltage: -0.105189 volts**
  Minimum Transition Eye Voltage Passes Sigtest Limits!
- **Maximum Transition Eye Voltage: 0.105026 volts**
  Maximum Transition Eye Voltage Passes Sigtest Limits!
- **Composite Eye Height: 0.071119**
- **Composite Eye Location: 0.652**
  Composite Eye Height Passes Sigtest Limits!
- **Minimum Transition Eye Voltage Margin Above Eye: 0.022703 volts**
  Minimum Transition Eye Voltage Margin Above Eye Passes Sigtest Limits
- **Minimum Transition Eye Voltage Margin Below Eye: -0.022538 volts**
  Minimum Transition Eye Voltage Margin Below Eye Passes Sigtest Limits!
- **Minimum Transition Eye Height: 0.091241 volts**

TEMPLATE FILE SETTINGS

- **Template File: PCIE_4_0_SYS \ PCIE_4_16GB_CEM_DUAL_PORT**
- **Nominal Data Rate (bits/sec): 15999999999.999998**
- **Target Unit Interval (s): 6.25e-011**
- **Minimum Time Allowed Between Crossovers (s): 4.0e-011**
- **Minimum Data For Testing (UI): 200**
- **Ambiguous UI Resolution Method: EYE_AMBIGUOUS_NONE (0)**
- **Tj@E-12 Peak to Peak Jitter Limit (s): 4.075e-011**
- **CTLE equalization index = 1**
- **DFE equalization: Tap 1 = 12.695312, Tap 2 = -4.882812**

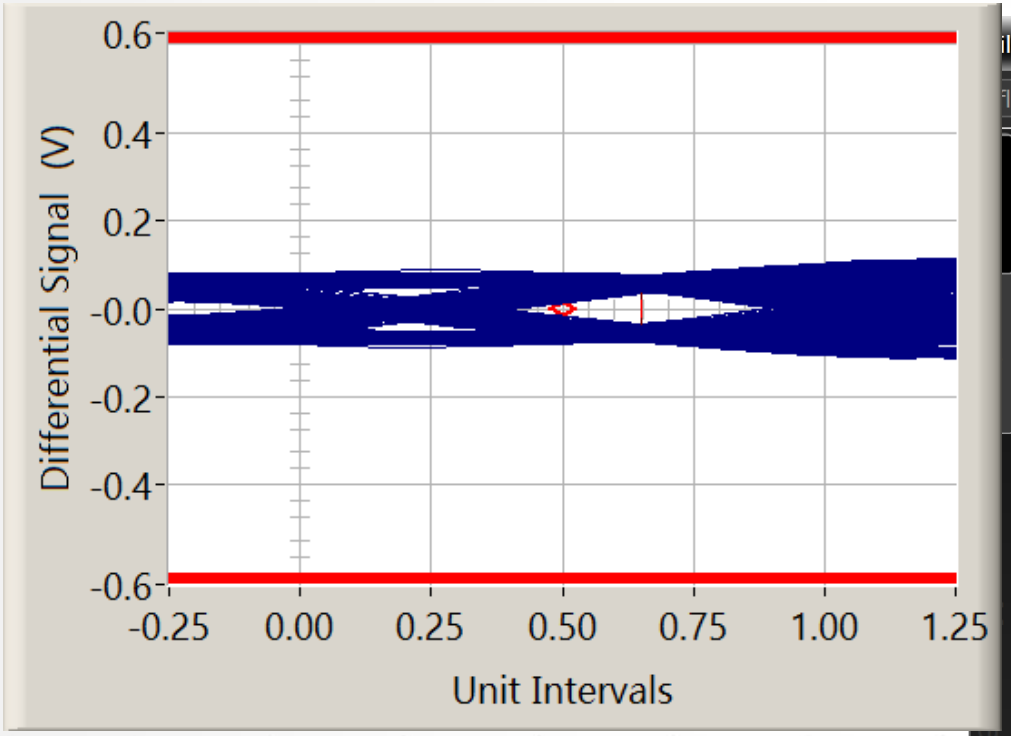
Sigtest Version: 4.0.45





SigTest result vs. Keysight SDA tool

SIGTEST STILL IN BETA VERSION!!!!



Composite Eye Height: 0.071119

Measurements

Measurement	Current	Mean
1 Eye height(eq)	73.0 mV	73.0 mV

KEYSIGHT TECHNOLOGIES

PCIe 4.0 LinkEQ and Receiver Testing at 16Gbps

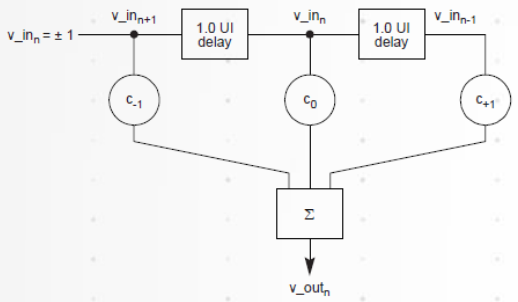
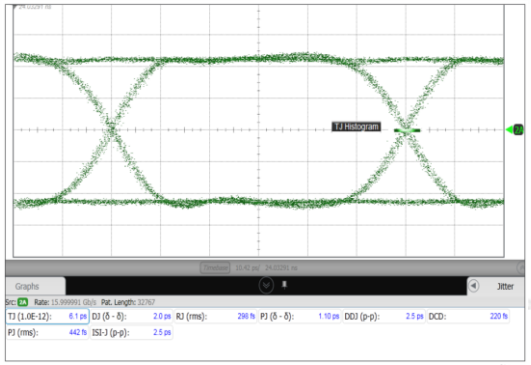


Figure 4-41: Tx Equalization FIR Representation



Jitter and De-emphasis

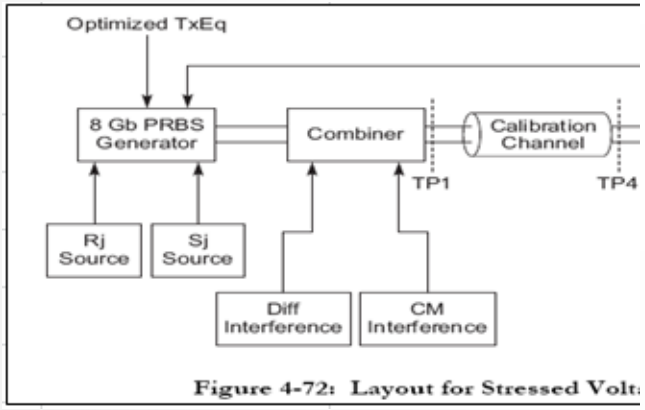
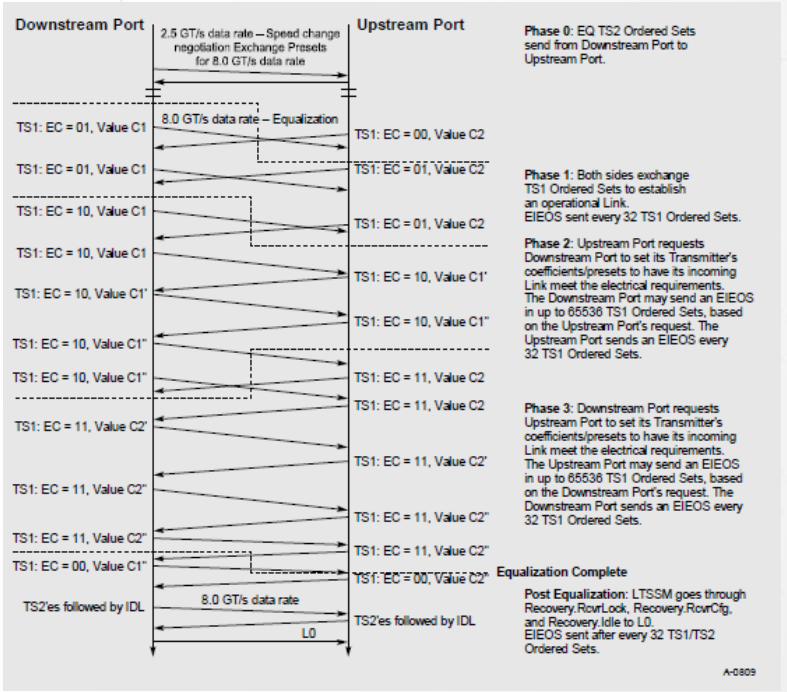


Figure 4-72: Layout for Stressed Volt

Link Equalization



Differences between PCIe Gen3 and PCIe Gen4
Relevant changes with PCIe 4.0 rev 0.5 and 0.7

	PCIe 3.0/3.1	PCIe 4.0 rev 0.5	Outlook PCIe 4.0 rev 0.7
added transfer rate	8 GT/s	16 GT/s	
coding	128B/130B		
block alignment & scrambler reset	EIEOS for block alignment		
EIEOS	10 00FF 00FF 00FF 00FF 00FF 00FF 00FF 00FF ➔ 500 MHz	10 00FF 00FF 00FF 00FF 00FF 00FF 00FF 00FF ➔ 1 GHz	10 0000 FFFF 0000 FFFF 0000 FFFF 0000 FFFF ➔ 500 MHz
scrambling	control: no (partially), data: always PRBS $2^{23}-1$; scrambler reset through EIEOS		
Adaptable TX link equalization	yes	yes, two step process: first 8G link eq followed by 16G link eq if 8G link eq is successful	
RX tests	stressed jitter test and stressed voltage test	one RX stress test	
SSC for common reference clock	no	no	yes
eye opening after reference RX for stress signal cal	0.3 UI, 25 mV, BER of 10^{-12}	0.3 UI, 15 mV (RX eye spec. is actually 14 mV), BER of 10^{-12}	
stress signal adjustment using	RJ, DM-SI and V_{diff}	coarse: ISI fine: DM-SI + SJ or DM-SI + V_{diff}	
CTLE changes: pole 1 frequency ➔ affects RX cal	2 GHz	4 GHz	2 GHz
Channel for RX test	No connector required	PCIe 4.0 CEM connector required as part of RX test channel	

Link EQ gets more important

Different cal procedure

Special cal channel fixture required

There is no Rx Jitter tolerance in Gen 4 test spec.

ONLY TX/RX LINK EQ TEST ITEMS

PCI Express Architecture PHY Test Specification

Revision 4.0, Version 0.7

November 8, 2018

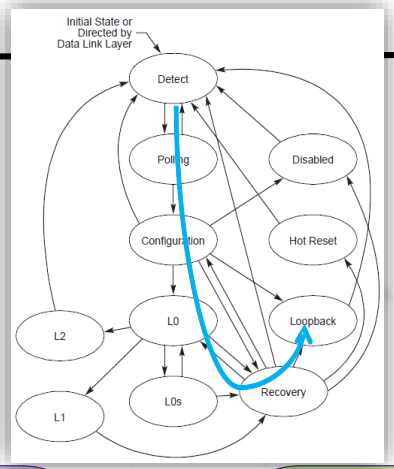
PCIe Tx EQ De-Emphasis and Rx EQ Equalization

Request de-emphasis setting

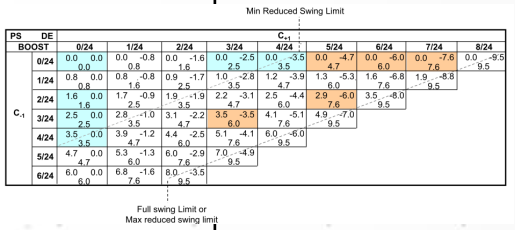
Algorithm for determining equalization and de-emphasis

Means for measuring signal quality

Control



De-Emphasis Controller



CDR

Equalization

Receiver

3-Tap De-Emphasis

Transmitter

2 Tap DFE

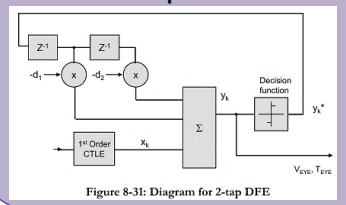


Figure 8-31: Diagram for 2-tap DFE

1 order CTLE

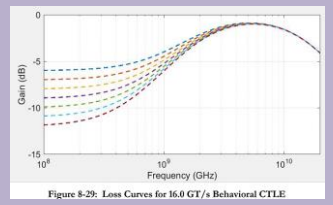
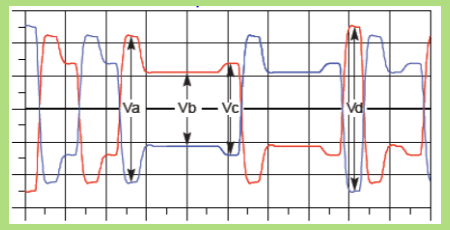


Figure 8-29: Loss Curves for 16.0 GT/s Behavioral CTLE



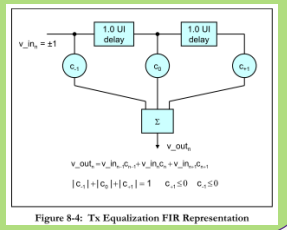


Figure 8-4: Tx Equalization FIR Representation

Reference Tx EQ : 3- Taps FIR, Presets and Cursors

Table 8-1. Tx Preset Ratios and Corresponding Coefficient Values

Preset #	Preshoot (dB)	De-emphasis (dB)	c-1	c+1	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5 dB	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1 dB	0.0	-0.166	0.000	0.668	0.668	1.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5 dB	0.000	-0.200	1.000	0.600	0.600
P10	0.0	Note 2.	0.000	Note 2.	1.000	Note 2.	Note 2.

Min Reduced Swing Limit

PS DE		C_{+1}								
BOOST		0/24	1/24	2/24	3/24	4/24	5/24	6/24	7/24	8/24
C_{-1}	0/24	0.0 0.0 0.0	0.0 -0.8 0.8	0.0 -1.6 1.6	0.0 -2.5 2.5	0.0 -3.5 3.5	0.0 -4.7 4.7	0.0 -6.0 6.0	0.0 -7.6 7.6	0.0 -9.5 9.5
	1/24	0.8 0.0 0.8	0.8 -0.8 1.6	0.9 -1.7 2.5	1.0 -2.8 3.5	1.2 -3.9 4.7	1.3 -5.3 6.0	1.6 -6.8 7.6	1.9 -8.8 9.5	
	2/24	1.6 0.0 1.6	1.7 -0.9 2.5	1.9 -1.9 3.5	2.2 -3.1 4.7	2.5 -4.4 6.0	2.9 -6.0 7.6	3.5 -8.0 9.5		
	3/24	2.5 0.0 2.5	2.8 -1.0 3.5	3.1 -2.2 4.7	3.5 -3.5 6.0	4.1 -5.1 7.6	4.9 -7.0 9.5			
	4/24	3.5 0.0 3.5	3.9 -1.2 4.7	4.4 -2.5 6.0	5.1 -4.1 7.6	6.0 -6.0 9.5				
	5/24	4.7 0.0 4.7	5.3 -1.3 6.0	6.0 -2.9 7.6	7.0 -4.9 9.5					
	6/24	6.0 0.0 6.0	6.8 -1.6 7.6	8.0 -3.5 9.5						

Full swing Limit or
Max reduced swing limit

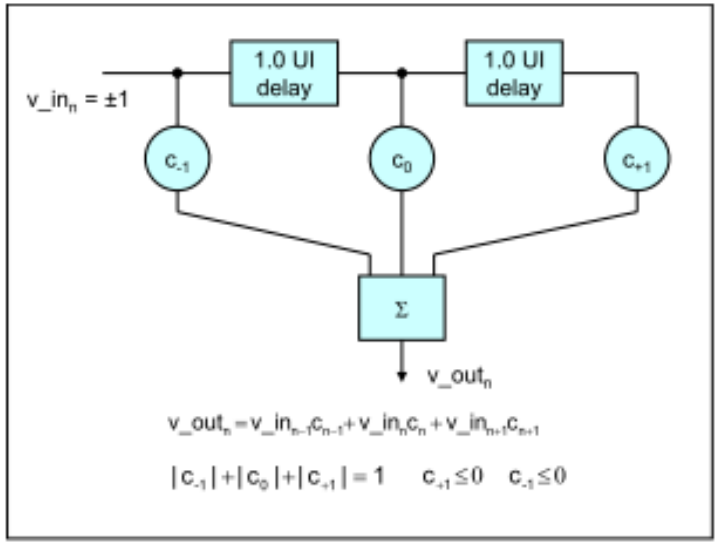
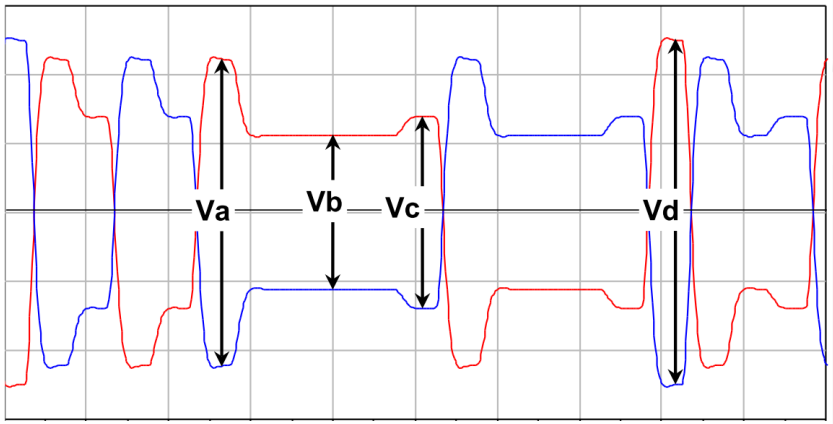


Figure 8-4: Tx Equalization FIR Representation



Reference Rx EQ : CTLE + DFE

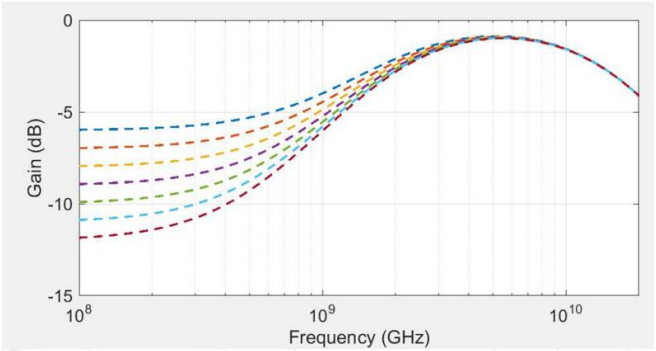
CTLE Should Be Static Setup or Adaptive ?

1st order CTLE with seven different “DC-attenuation“ settings peaking at 8 GHz

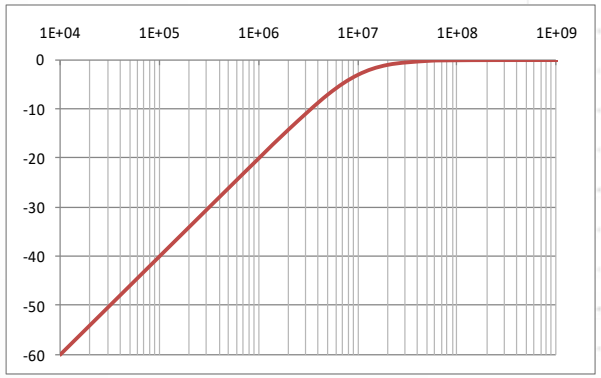
2 tap DFE with a limit for d1 of +/- 20mV

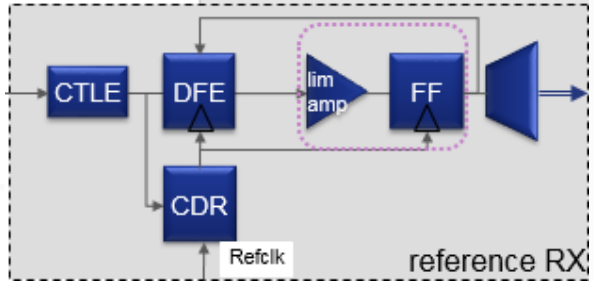
$$H(s) = \omega_{P2} \frac{s + \omega_{P1} * A_{DC}}{(s + \omega_{P1}) * (s + \omega_{P2})}$$

1



2





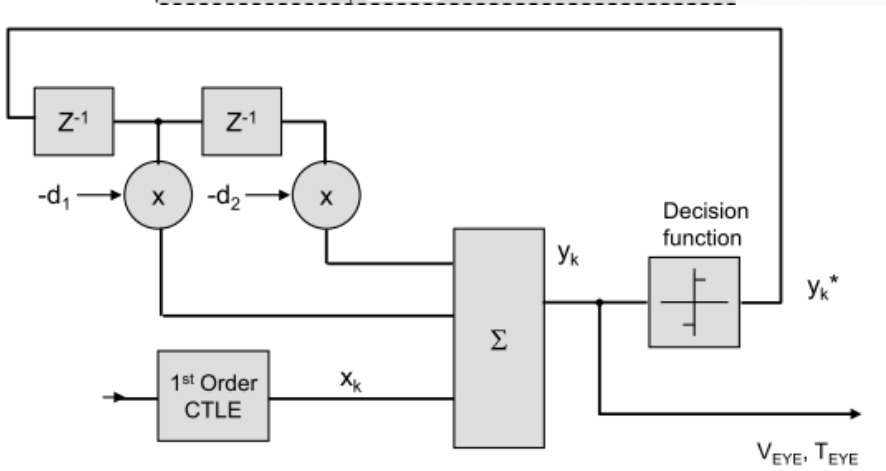
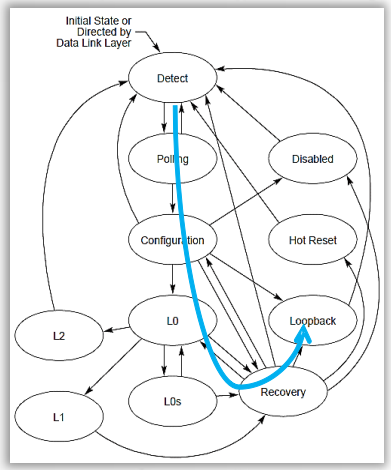
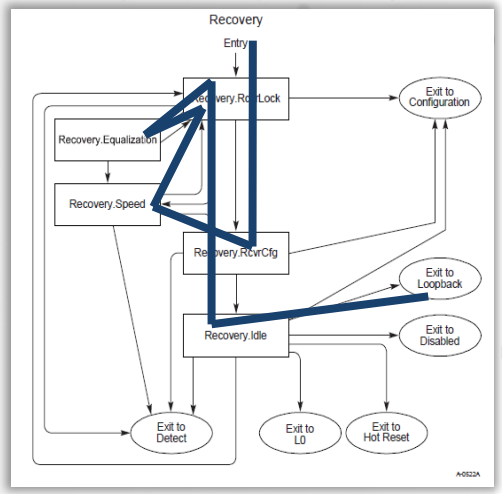


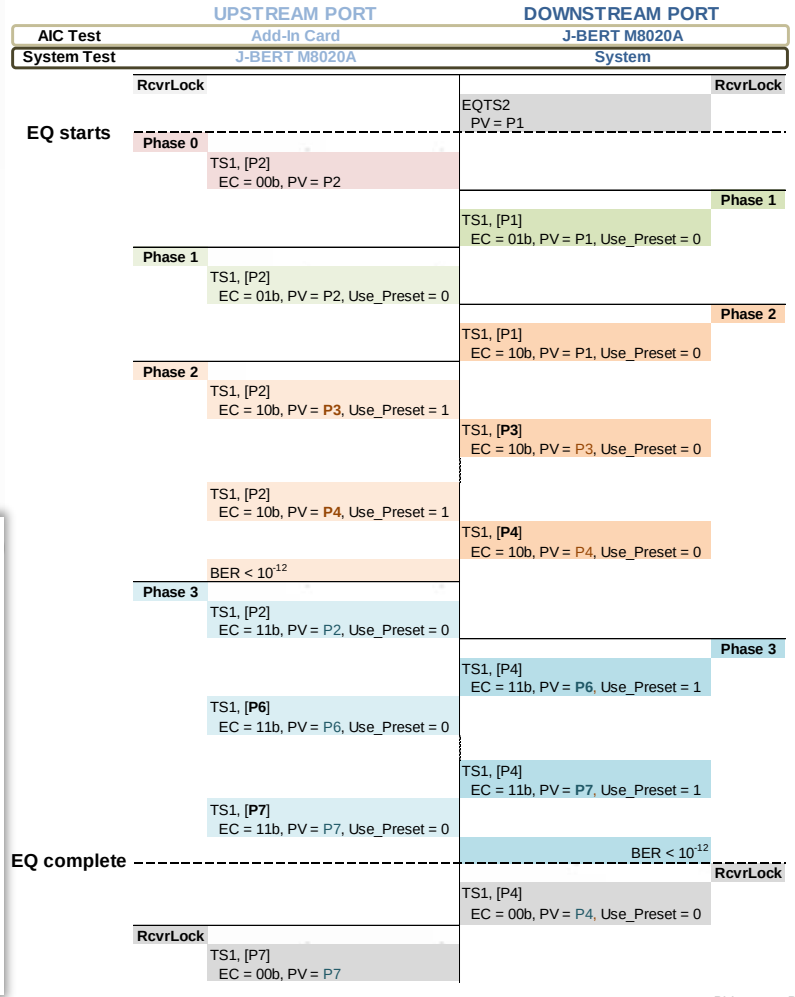
Figure 8-31: Diagram for 2-tap DFE

Dynamic Link Equalization Handshake 16G

The Four Phases Of The Link Equalization Protocol







Phase 0:
- 2.5 Gb/s
- Downstream port tells upstream port which initial preset to use after the speed change will have been done.

Phase 1:
- 8 Gb/s
- Link partners settle on 8 GT/s speed.
- Exchange FS/LF values.

Phase 2:
- 8 Gb/s
- Add-in Card sets up the de-emphasis of the System Board's transmitter.

Phase 3:
- 8 Gb/s
- System Board sets up the de-emphasis of the Add-in Card's transmitter.

IF SUCCESSFUL

Phase 0:
- 8 Gb/s
- Downstream port tells upstream port which initial preset to use after the speed change will have been done.

Phase 1:
- 16 Gb/s
- Link partners settle on 16 GT/s speed.
- Exchange FS/LF values.

Phase 2:
- 16 Gb/s
- Add-in Card sets up the de-emphasis of the System Board's transmitter.

Phase 3:
- 16 Gb/s
- System Board sets up the de-emphasis of the Add-in Card's transmitter.

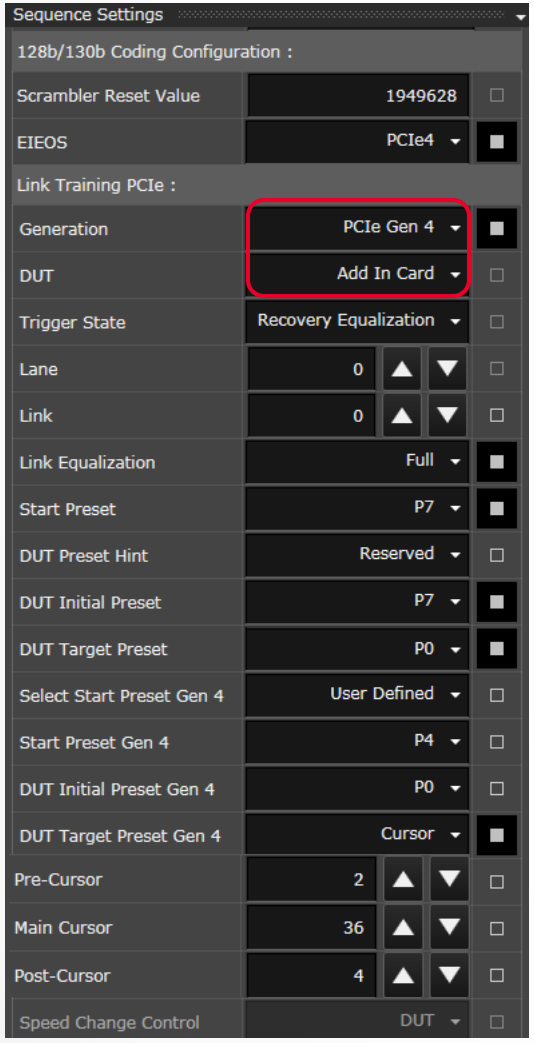
PV Preset Value

EC Equalization Control

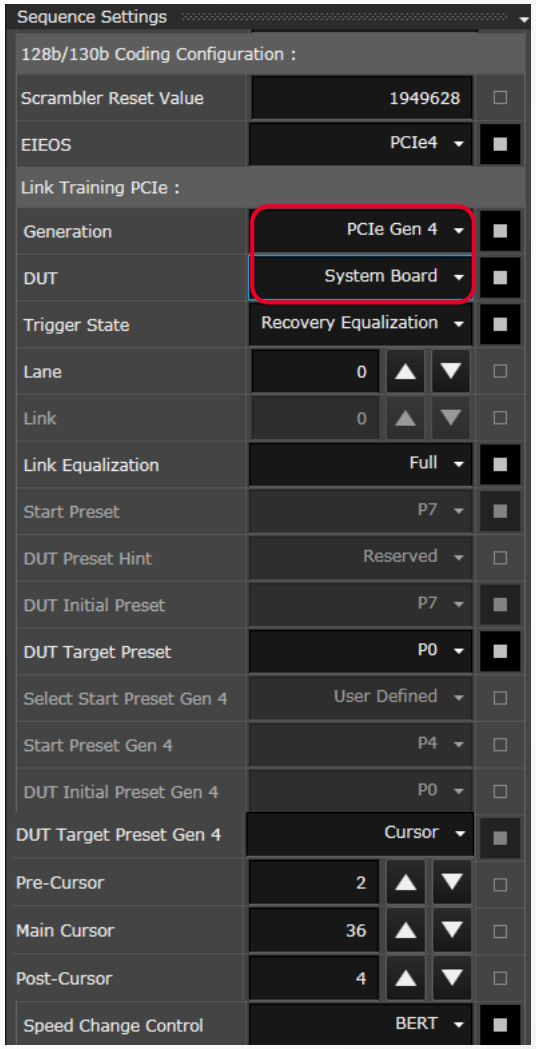
Tx/Rx Link Equalization Testing

LTSSM SETUP – PCIE 16GT/S

M8020A J-BERT



- EIEOS needs to be set to PCIe3 for PCI Express Base Specification 4.0 rev 0.5. But for PCIe Base Specification 4.0 rev 0.7 and higher it needs to be set PCIe4!
- Generation needs to be set to PCIe Gen 4
- Select DUT type:
  - Any endpoint device ➔ Add In Card
  - Any root complex device ➔ System Board
- Two sets of phase 0 through phase 3 parameters
  - 2.5GT/s to 8GT/s
    - DUT Target Preset can be presets only
  - 8GT/s to 16GT/s
    - DUT Target Preset 4 can be presets or coefficients
- Speed Change Control:
  - While the root complex usually is responsible for initiating the speed change, most root complex today need the RX test equipment to take control of the speed change.



J-BERT M8020A Setup – PCIe 4.0

LTSSM Log – CPU example

Link Training Logging for M1.DataOut1 at 12/05/2018 11:55:20

State	Execution Time	Transfer Rate
Detect.Active	1.04864 ms	2.5 GT/s
Polling.Active	2.25792 ms	2.5 GT/s
Polling.Configuration	22.94616 ms	2.5 GT/s
Configuration.Linkwidth.Start	528 ns	2.5 GT/s
Configuration.Linkwidth.Accept	22.96 us	2.5 GT/s
Configuration.Lanenum.Wait	2.16 us	2.5 GT/s
Configuration.Lanenum.Accept	496 ns	2.5 GT/s
Configuration.Complete	1.36 us	2.5 GT/s
Configuration.Idle	1.856 us	2.5 GT/s
L0	336 ns	2.5 GT/s
Recovery.RcvrLock	4.848 us	2.5 GT/s
Recovery.RcvrCfg	2.496 us	2.5 GT/s
Recovery.Speed	7.616 us	2.5 GT/s
Recovery.RcvrLock	448 ns	8.0 GT/s
Recovery.Equalization.Phase0	1.074304 ms	8.0 GT/s
Recovery.Equalization.Phase1	906.832 us	8.0 GT/s
Recovery.Equalization.Phase2	1.728 us	8.0 GT/s
Recovery.Equalization.Phase3	10.050416 ms	8.0 GT/s
Recovery.RcvrLock	432 ns	8.0 GT/s
Recovery.RcvrCfg	1.568 us	8.0 GT/s
Recovery.Idle	432 ns	8.0 GT/s
L0	336 ns	8.0 GT/s
Recovery.RcvrLock	3.328 us	8.0 GT/s
Recovery.RcvrCfg	816 ns	8.0 GT/s
Recovery.Speed	8.96 us	8.0 GT/s
Recovery.RcvrLock	448 ns	16.0 GT/s
Recovery.Equalization.Phase0	141.6 us	16.0 GT/s
Recovery.Equalization.Phase1	629.856 us	16.0 GT/s
Recovery.Equalization.Phase2	1.456 us	16.0 GT/s
Recovery.Equalization.Phase3	6.97888 ms	16.0 GT/s
Recovery.RcvrLock	304 ns	16.0 GT/s
Recovery.RcvrCfg	1.424 us	16.0 GT/s
Recovery.Idle	112 ns	16.0 GT/s
Loopback.Entry	2.16 us	16.0 GT/s
Loopback.Active	-	16.0 GT/s

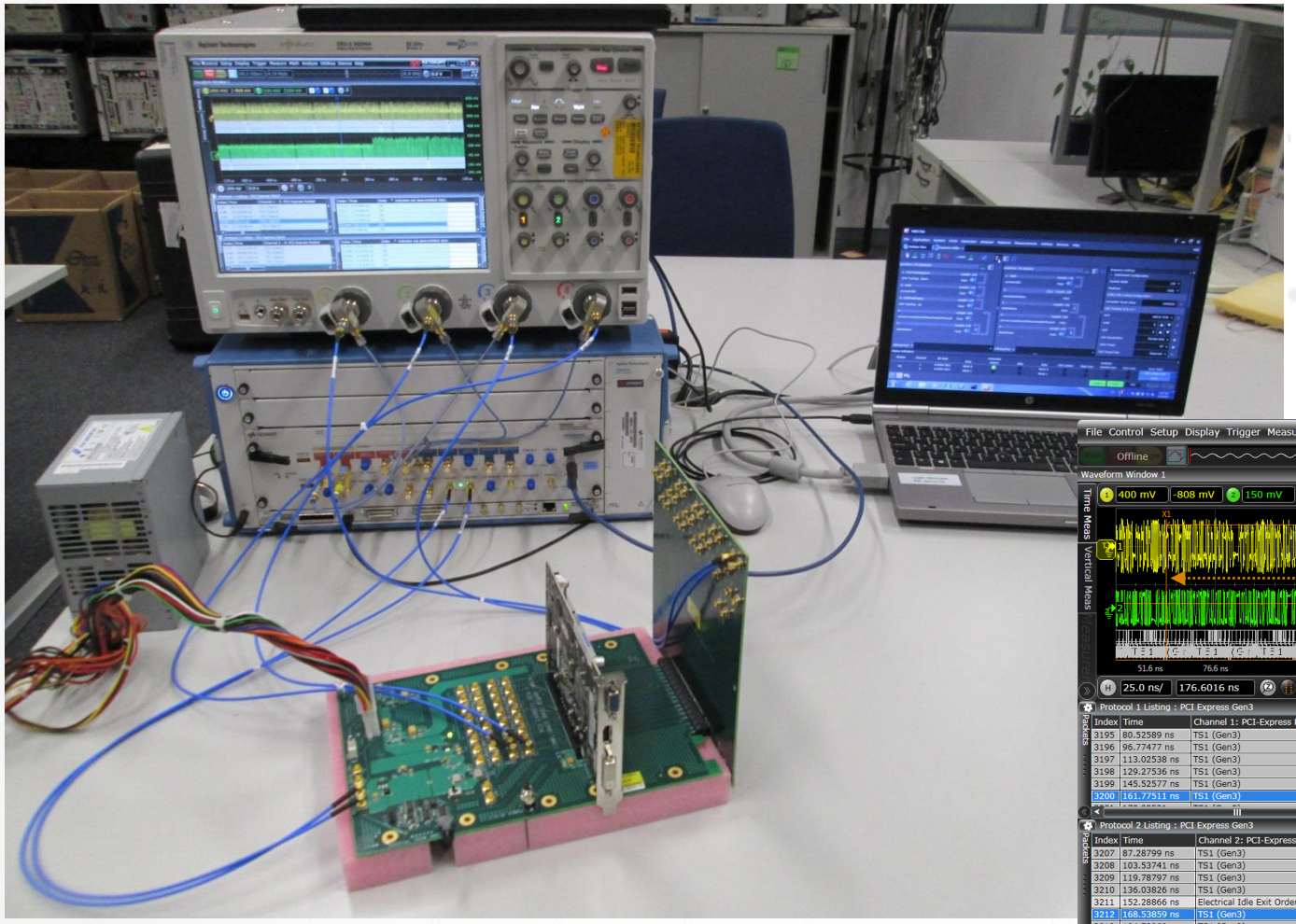
Change Requests to BERT

BERT Tx Equalization

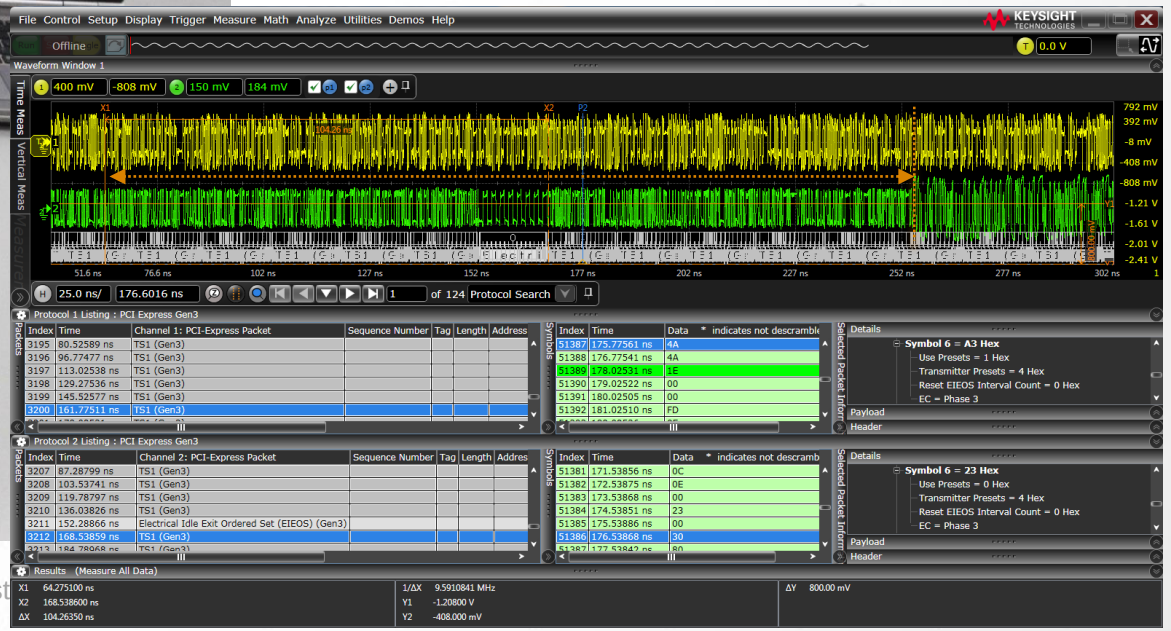
Accept LowFrequency	Speed	Preset	PreCursor	MainCursor	PostCursor	FullSwing	
True	Gen3	P7	-	-	-	24	8
True	Gen3	P0	-	-	-	24	8
True	Gen3	P1	-	-	-	24	8
True	Gen3	P2	-	-	-	24	8
True	Gen3	P3	-	-	-	24	8
True	Gen3	P4	-	-	-	24	8
True	Gen3	P5	-	-	-	24	8
True	Gen3	P6	-	-	-	24	8
True	Gen3	P7	-	-	-	24	8
True	Gen3	P8	-	-	-	24	8
True	Gen3	P9	-	-	-	24	8
True	Gen3	P6	-	-	-	24	8
True	Gen3	P7	-	-	-	24	8
True	Gen4	P0	-	-	-	24	8
True	Gen4	P1	-	-	-	24	8
True	Gen4	P2	-	-	-	24	8
True	Gen4	P3	-	-	-	24	8
True	Gen4	P4	-	-	-	24	8
True	Gen4	P5	-	-	-	24	8
True	Gen4	P6	-	-	-	24	8
True	Gen4	P7	-	-	-	24	8
True	Gen4	P8	-	-	-	24	8
True	Gen4	P9	-	-	-	24	8
True	Gen4	P7	-	-	-	24	8

Tx Link Equalization Testing for PCIe 3.0/4.0

Tests 2.3 and 2.4 – Add-in Card Transmitter Initial TX EQ test and Link Equalization Response Test Test Setup



- J-BERT M8020A is used to train the device and issue a trigger to the scope allowing to capture phase 3
- J-BERT TX signal as well as DUT TX signals are split and captured by the scope
- The common timing reference allows for timing measurements on the captured and decoded waveforms

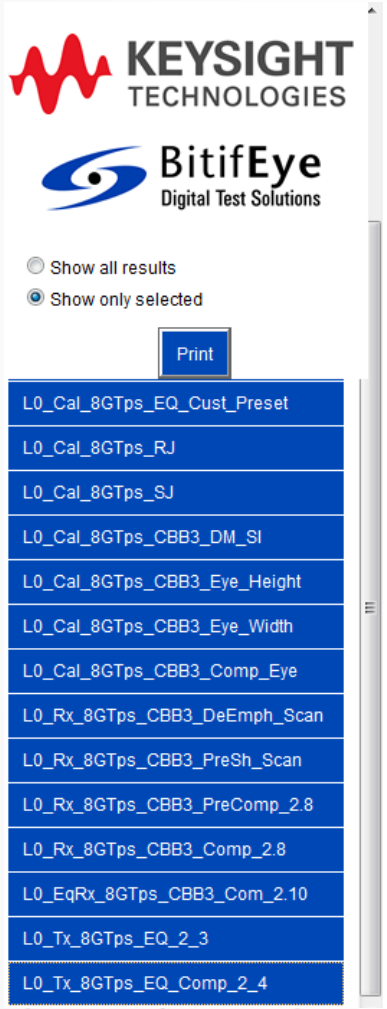


PCIe 4.0
16 GT/s RX Test

KEYSIGHT TECHNOLOGIES

Tx Link Equalization Testing for PCIe 3.0

Test 2.4 – Example Test Result Report

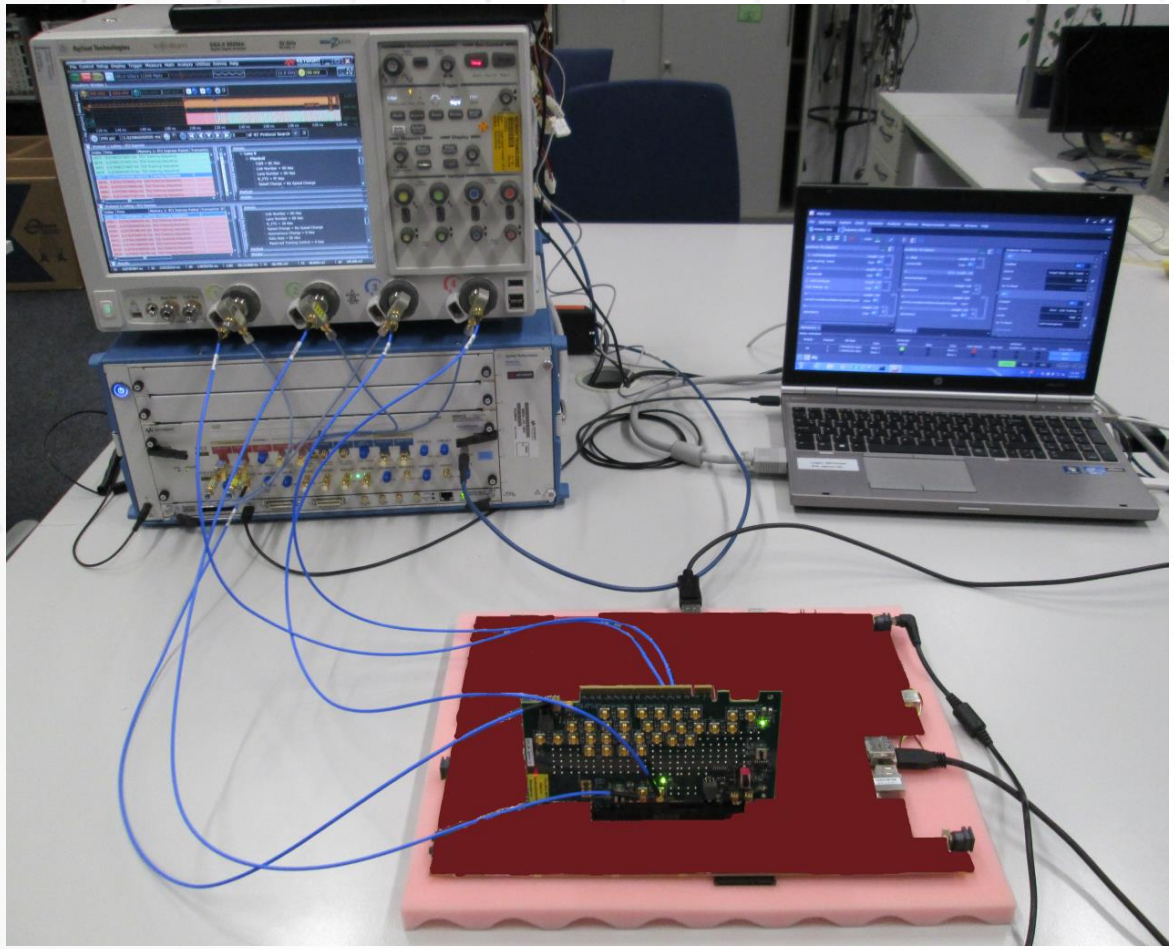


Use Power Switch Automation	True
Power Switch Channel Number	2
Power Cycle Off On Duration	7 s
Power Cycle Settling Time	8 s
Power Cycle max. Retries for LB Training	3

Result	DUT Target Preset	Electrical response time [ns]	Protocol response time [ns]	Pre-Shoot [dB]	Min Spec PS [dB]	Max Spec PS [dB]	De-Emphasis [dB]	Min Spec DE [dB]	Max Spec DE [dB]	Comment
pass	P0	129.87	125.25	0.00	0.00	0.00	-6.03	-7.50	-4.50	DUT reported cursors: (0,45,15)
pass	P1	125.12	136.12	0.00	0.00	0.00	-3.54	-4.50	-2.50	DUT reported cursors: (0,50,10)
pass	P2	126.25	125.87	0.00	0.00	0.00	-4.45	-5.90	-2.90	DUT reported cursors: (0,48,12)
pass	P3	131.87	124.62	0.00	0.00	0.00	-2.71	-3.50	-1.50	DUT reported cursors: (0,52,8)
pass	P4	132.25	121.62	0.00	0.00	0.00	0.00	0.00	0.00	DUT reported cursors: (0,60,0)
pass	P5	126.37	130.37	1.93	0.90	2.90	0.00	0.00	0.00	DUT reported cursors: (6,54,0)
pass	P6	128.50	132.00	2.69	1.50	3.50	0.00	0.00	0.00	DUT reported cursors: (8,52,0)
pass	P7	134.50	132.37	3.51	2.50	4.50	-6.03	-7.50	-4.50	DUT reported cursors: (6,42,12)
pass	P8	131.12	121.62	3.91	2.50	4.50	-3.92	-4.50	-2.50	DUT reported cursors: (8,44,8)
pass	P9	130.75	128.12	3.50	2.50	4.50	0.00	0.00	0.00	DUT reported cursors: (10,50,0)
pass	P0' (0,45,15)	127.12	128.25	0.00	0.00	0.00	-6.03	-7.50	-4.50	
pass	P1' (0,50,10)	127.12	127.75	0.00	0.00	0.00	-3.54	-4.50	-2.50	
pass	P2' (0,48,12)	126.00	124.12	0.00	0.00	0.00	-4.46	-5.90	-2.90	
pass	P3' (0,52,8)	142.12	120.12	0.00	0.00	0.00	-2.70	-3.50	-1.50	
pass	P4' (0,60,0)	127.00	126.87	0.00	0.00	0.00	0.00	0.00	0.00	
pass	P5' (6,54,0)	130.50	121.37	1.93	0.90	2.90	0.00	0.00	0.00	
pass	P6' (8,52,0)	127.25	121.37	2.68	1.50	3.50	0.00	0.00	0.00	
pass	P7' (6,42,12)	125.37	128.12	3.50	2.50	4.50	-6.03	-7.50	-4.50	
pass	P8' (8,44,8)	123.75	123.37	3.91	2.50	4.50	-3.93	-4.50	-2.50	
pass	P9' (10,50,0)	133.75	119.87	3.52	2.50	4.50	0.00	0.00	0.00	

Tx Link Equalization Testing for PCIe 3.0

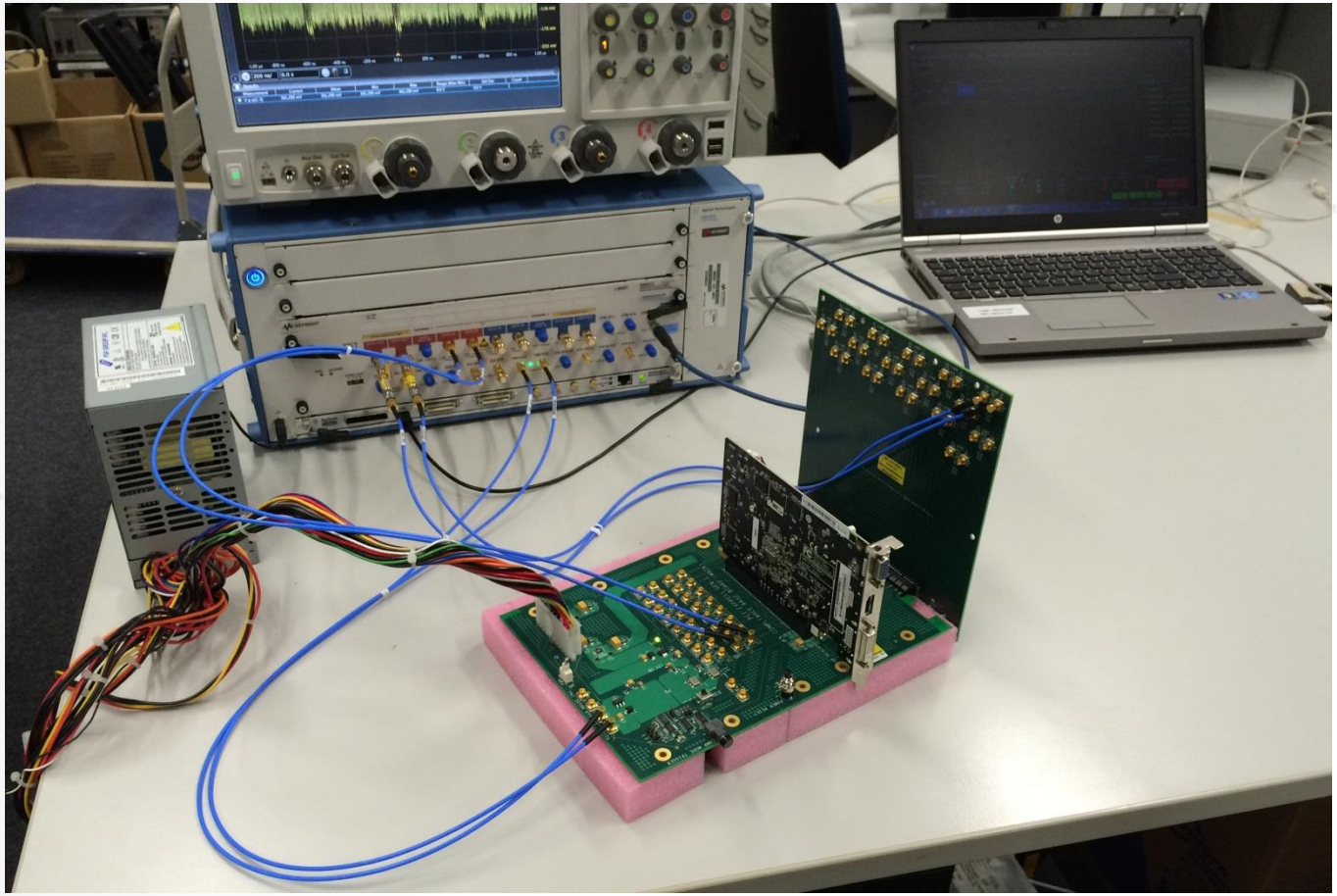
Tests 2.7 System Board Transmitter Link Equalization Response Test – Test Setup



- J-BERT M8020A is used to train the device and issue a trigger to the scope allowing to capture phase 2
- J-BERT TX signal as well as DUT TX signals are split and captured by the scope
- J-BERT M8020A is synchronized to the system by the system's 100MHz clock
- It is not necessary to turn off SSC on the system side

Rx Link Equalization Testing for PCIe 3.0

Tests 2.10 – Add-in Card Receiver Link Equalization Test - Test Setup



J-BERT M8020A is used to train the device through L0 and recovery into loopback

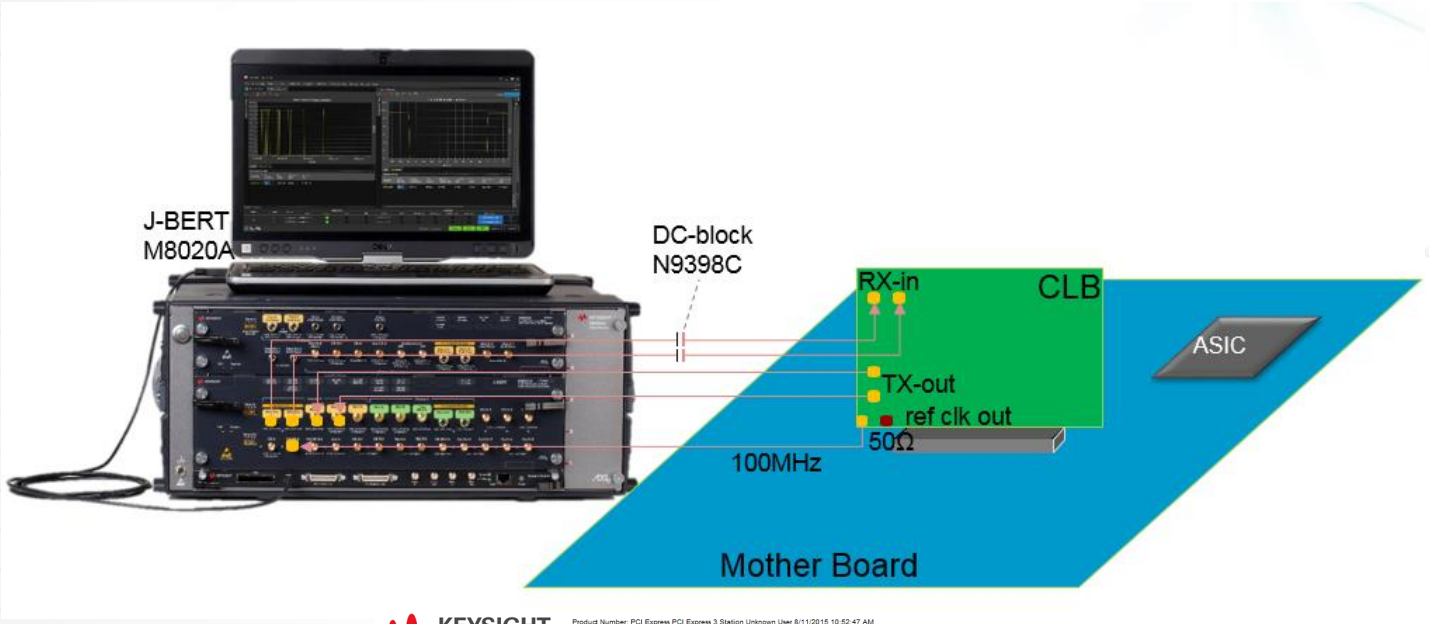
Phase 2 and 3 are performed and the AIC optimizes J-BERT TX to the actual stress signal

J-BERT checks the looped signal for the BER

Very clean setup since no additional instruments or repeaters are required

Rx Link Equalization Testing for PCIe 3.0

Tests 2.11 System Receiver Link Equalization Test – Test Setup



KEYSIGHT TECHNOLOGIES

BitifEye Digital Test Solutions

Show all results
Show only selected

Print

Summary
Instruments
L0_Cal_8GTps_PreShoot
L0_Cal_8GTps_DeEmphasis
L0_Cal_8GTps_EQ_Preset
L0_Cal_8GTps_EQ_Cust_Preset
L0_Cal_8GTps_RJ
L0_Cal_8GTps_SJ
L0_Cal_8GTps_CBB3_DM_SI
L0_Cal_8GTps_CLB3_Eye_Height
L0_Cal_8GTps_CLB3_Eye_Width
L0_Cal_8GTps_CLB3_Comp_Eye
L0_Rx_8GTps_CLB3_DeEmph_Scan
L0_Rx_8GTps_CLB3_PreSh_Scan
L0_Rx_8GTps_CLB3_Comp_2.9
L0_EqRx_8GTps_CLB3_Com_2.11
L0_Tx_8GTps_EQ_Comp_2_7

Product Number: PCI Express PCI Express 3 Station Unknown User 8/11/2015 10:52:47 AM

L0_EqRx_8GTps_CLB3_Com_2.11

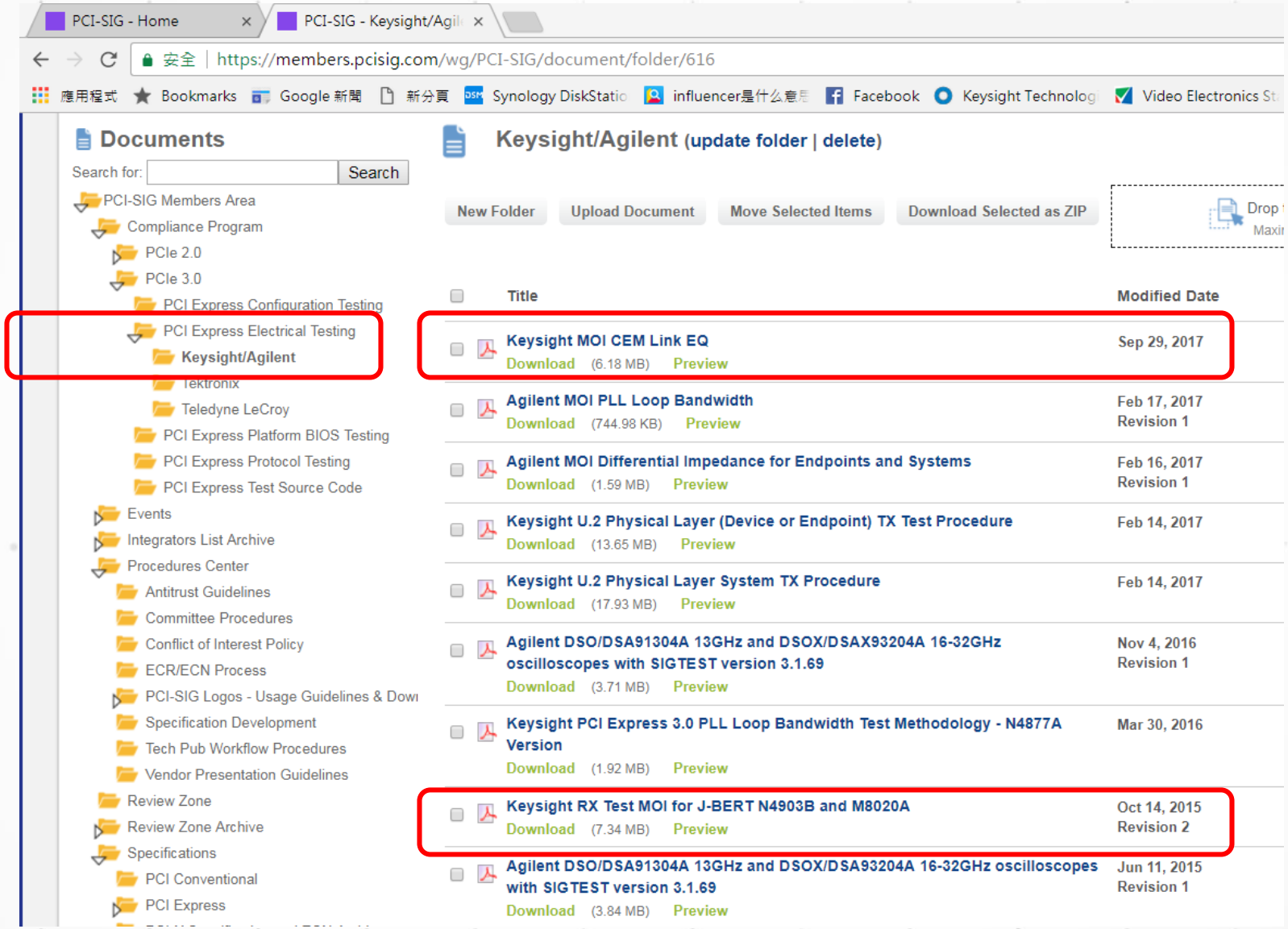
for PCI Express 3.0 System

Differential Mode Sinusoidal Interference	26.96 mV
Random Jitter	2.735 ps
Sinusoidal Jitter	12.5 ps
Offline	False
Enable Impairments for Link Training	True
Eye-Height	49 mV
Eye-Width	44.5 ps
Sinusoidal Jitter Frequency	100 MHz
BER Mode	FixedTime
BER Measurement Duration	125 s
Allowed Bit Error	1
DUT Tx Preset	P4
DUT Target Preset	P7
Interactive Training Script File	C:\Documents and Settings\All Users\Application Data\Bitifeye\Valiframe\Settings\PCIExpress3\Pcie3_8G_M8020A_IIT_Loopback.txt
Suppress Loopback Training Messages	False
CDR Loop Bandwidth	12 MHz
Peaking	1 dB
Analyzer Equalization	6dB
Capture and Compare Mode	False
Relax Time	1 s
Use Power Switch Automation	False

Result	Initial Generator Preset	Final Generator Preset	Final Generator Pre-shoot [dB]	Final Generator De-emphasis [dB]	Allowed Bit Errors []	Measured Bit Errors []
pass	P7	P6	2.50	0.00	1	0

- J-BERT is running on the system's 100MHz reference clock
- J-BERT M8020A is used to train the system through L0 and recovery into loopback
- Phase 3 are performed and the System optimizes J-BERT TX to the actual stress signal
- J-BERT checks the looped signal for the BER
- Very clean setup since no additional instruments or repeaters are required

PCIe3.0 Rx and CEM LinkEQ Test Gold Suites approval by PCISIG



PCIe 4.0 Base Receiver Tests

16GT/s Base Specification – RX Calibration Channel

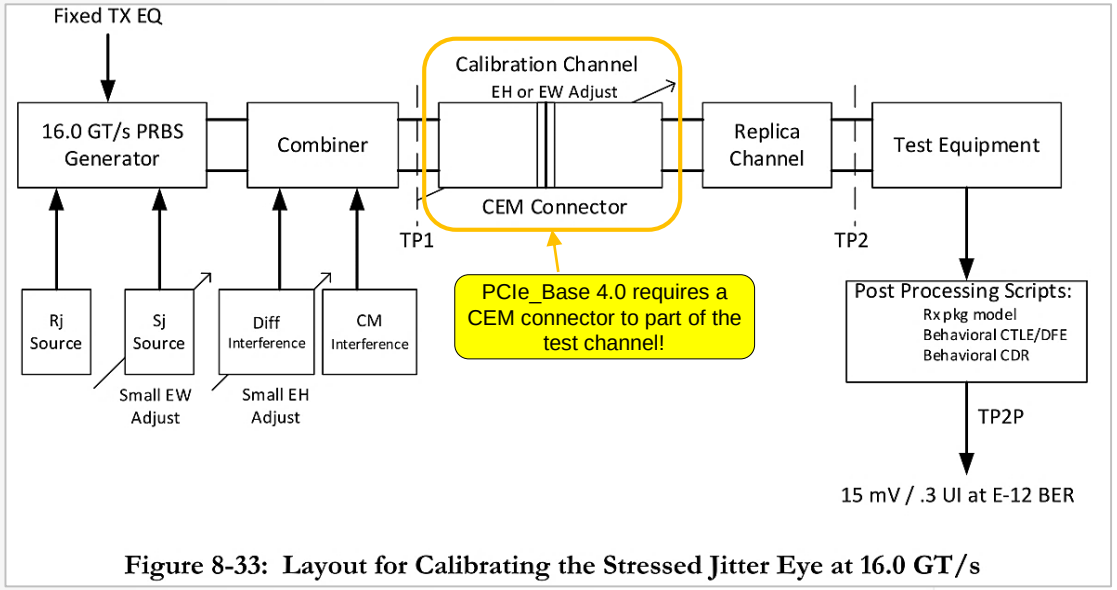
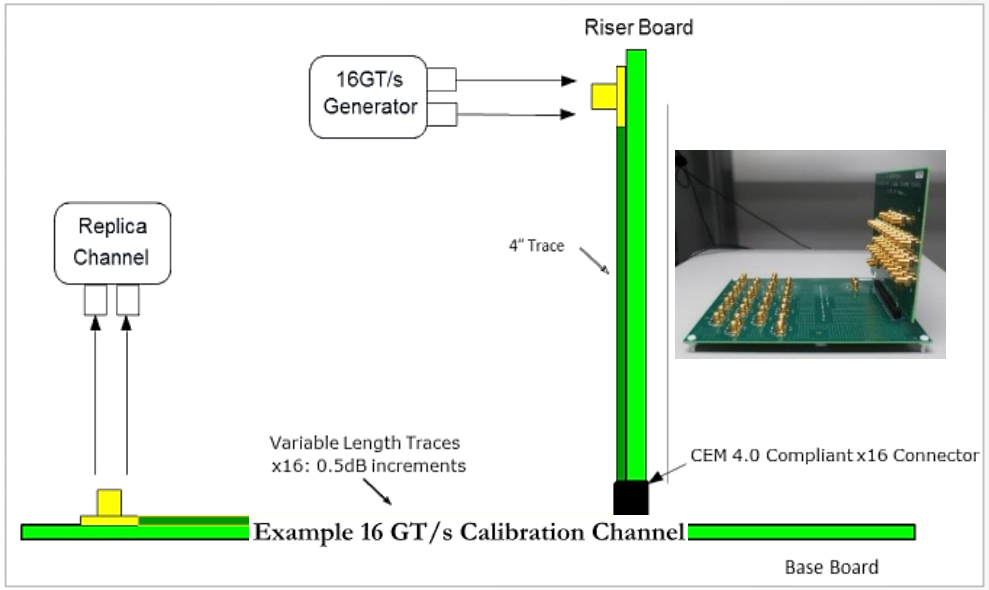
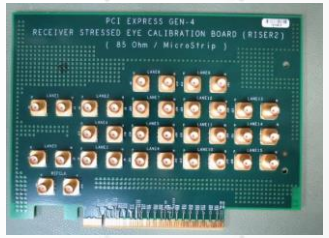
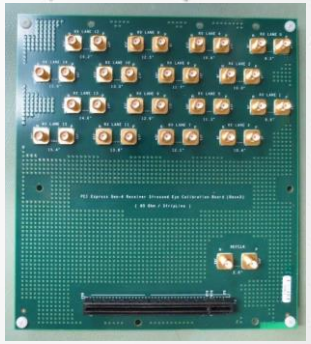


Figure 8-33: Layout for Calibrating the Stressed Jitter Eye at 16.0 GT/s



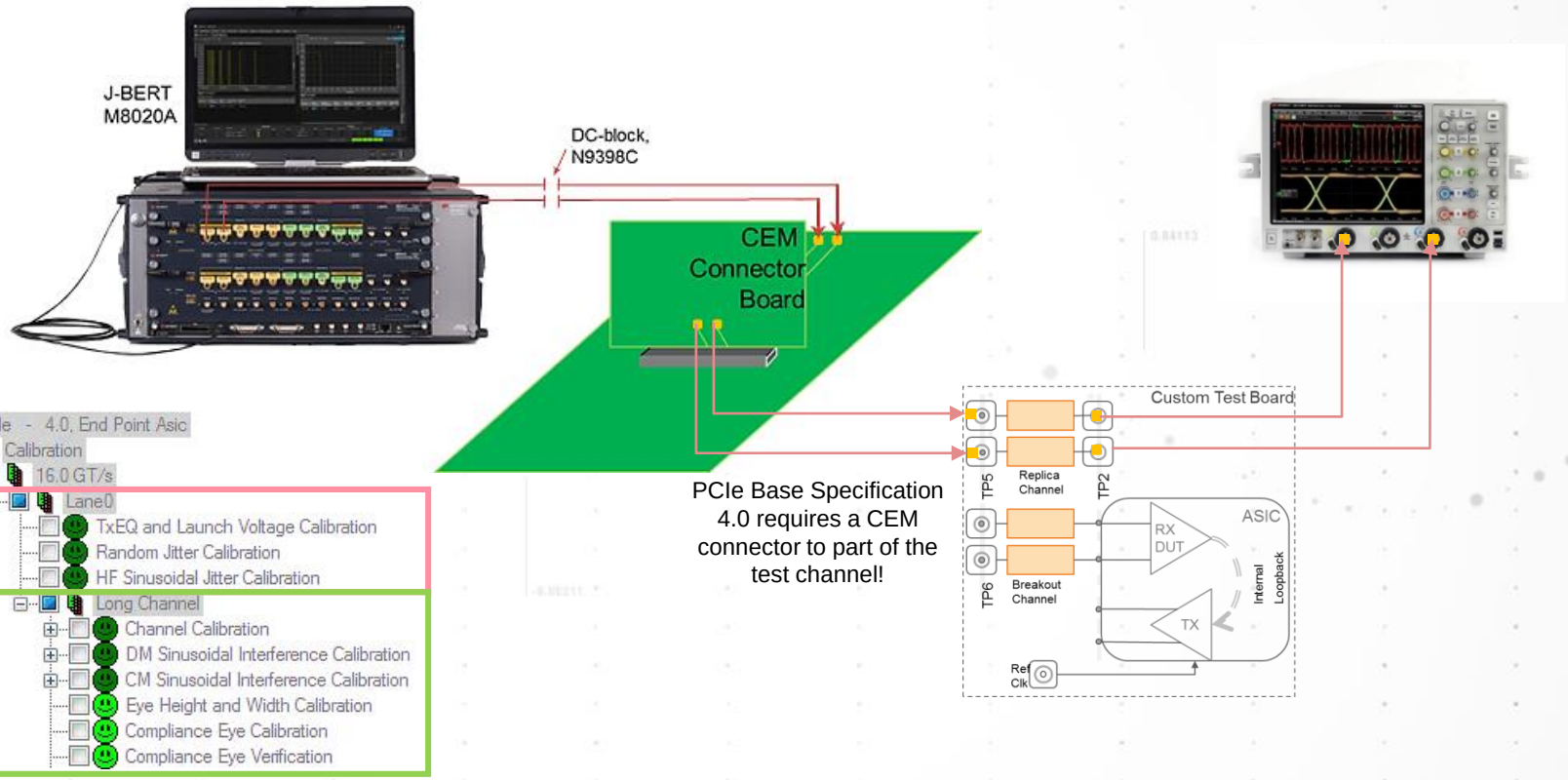
- The test channel is the long Rx calibration channel with a total loss of **28.0dB at** (Physical channel loss 23dB for RC)
- PCIe 4.0 Base Spec **requires a CEM connector to be part of the test channel 8GHz.**
- Stress jitter eye height **≤15mV**, Eye width **≤0.3UI**, same with CEM spec.
- Channel calibration with preset selection to get as close to target eye height and eye width as possible.
- Compliance eye calibration is done by adjusting **DM-SI, SJ or $V_{diff.}$**
- DM-SI and CM-SI are calibrated through the channel.





PCIe 4.0 Base Receiver Tests - Calibration

16GT/s Base Specification – RX Stress Signal Calibration Setup



N5990A Test Automation SW

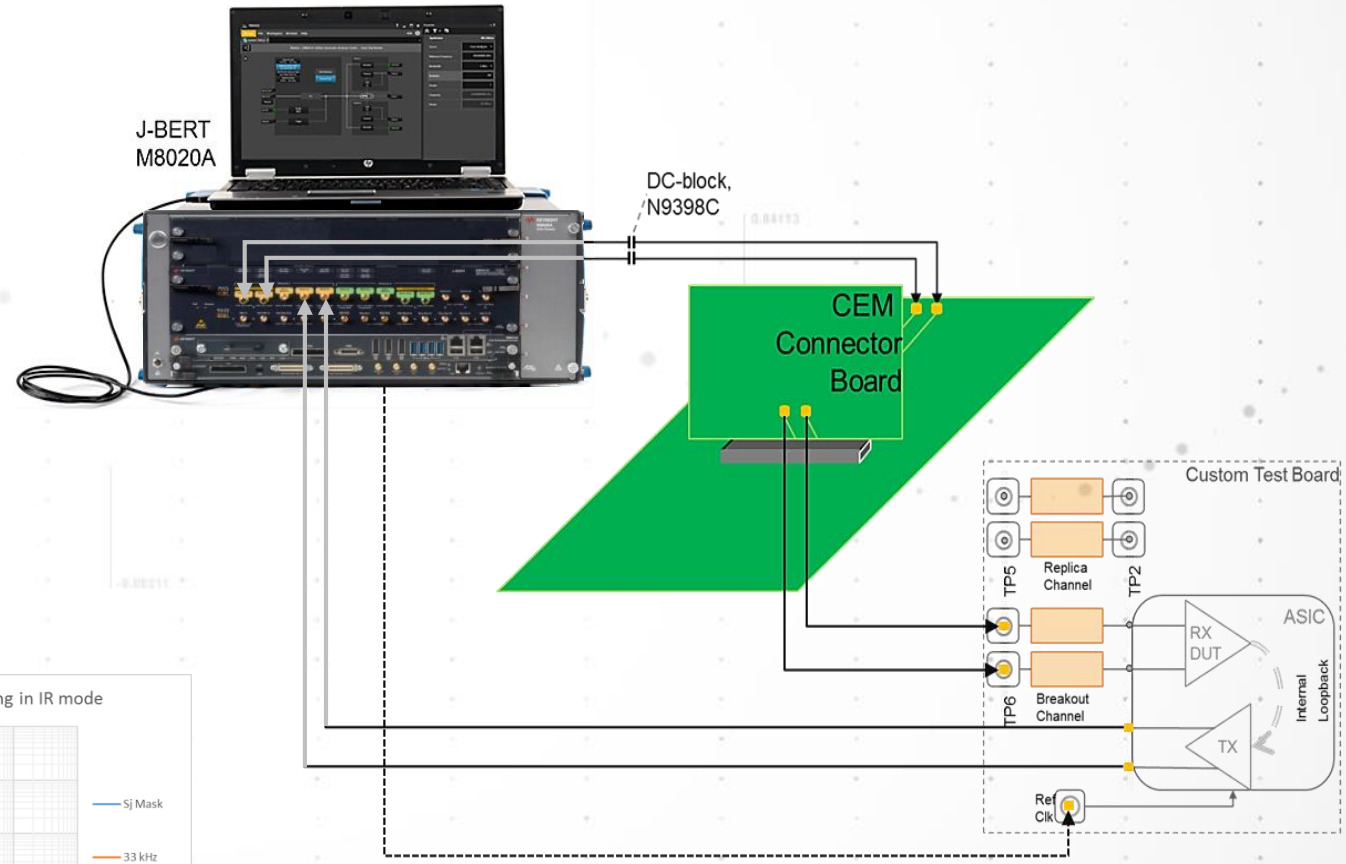
PCIe Base Specification 4.0 requires a CEM connector to part of the test channel!

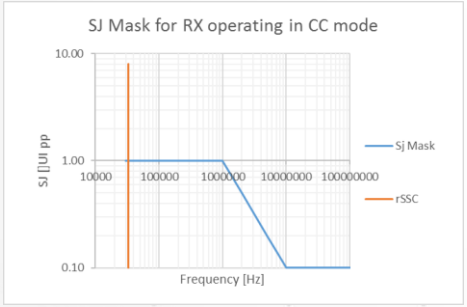
- **J-BERT M8020A's internal ISI can be used to calibrate channel**.
- All other impairments are provided by J-BERT M8020A (**RJ, SJ, DMSI, ISI, SSC**).
- A built-in reference clock multiplier enables J-BERT M8020A to operate on a DUT's reference clock if required.

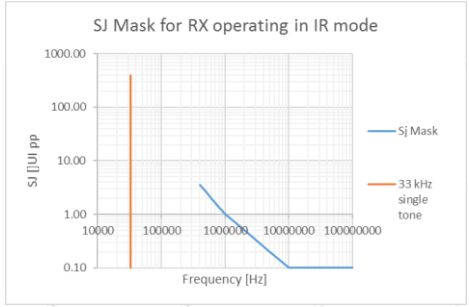
PCIe 4.0 Base Receiver Tests

16GT/s Base Specification – RX Test Setup

- PCIe 4.0 Base Spec requires a CEM connector to be part of the test channel!
- All other impairments are provided by J-BERT M8020A
- A built-in reference clock multiplier enables J-BERT M8020A to operate on a DUT's reference clock if required
- No ref clock connection in case of IR / SRIS

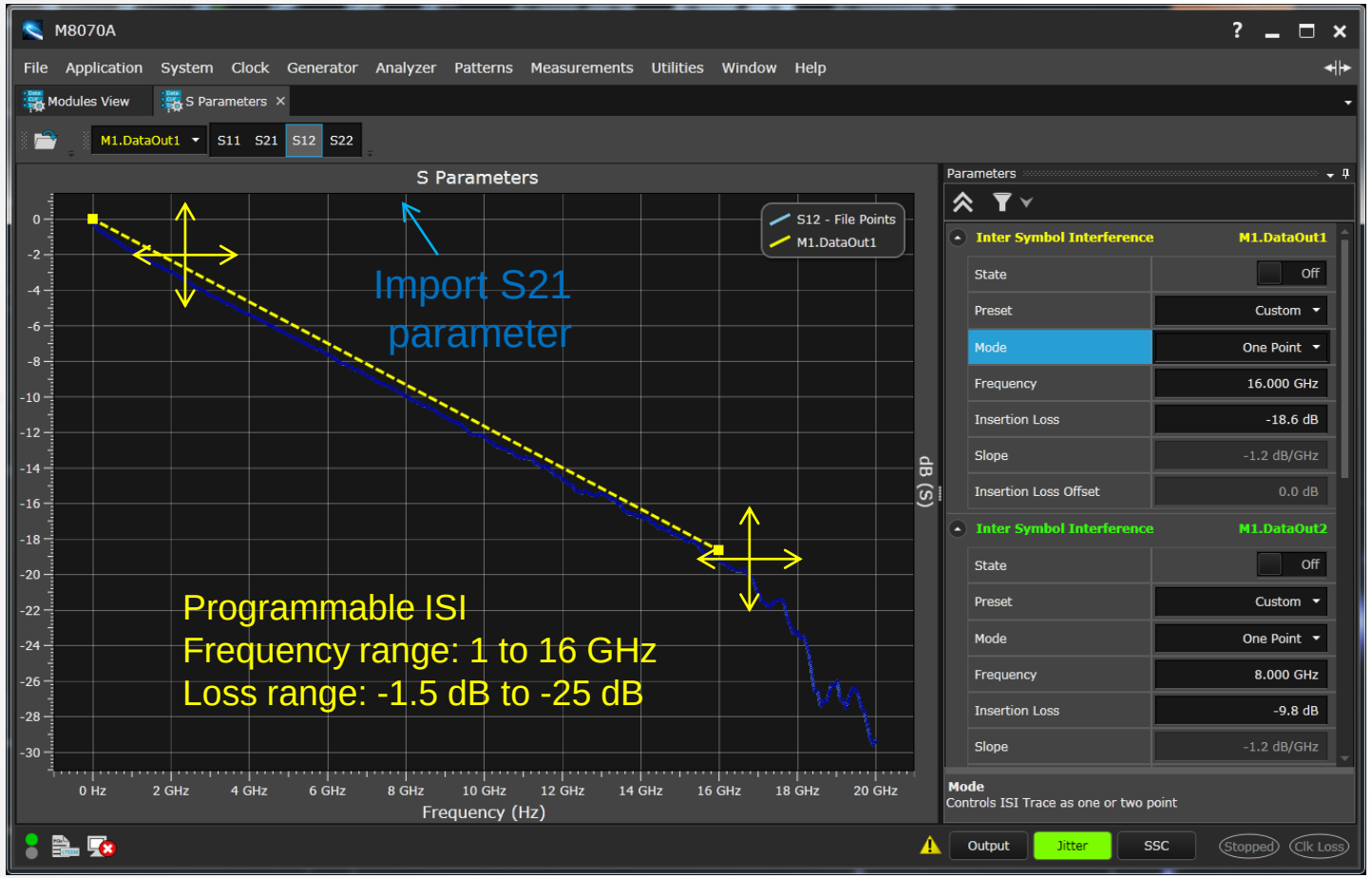






Emulating Loss with J-BERT M8020A

DATA OUTPUT – Internally Generated ISI



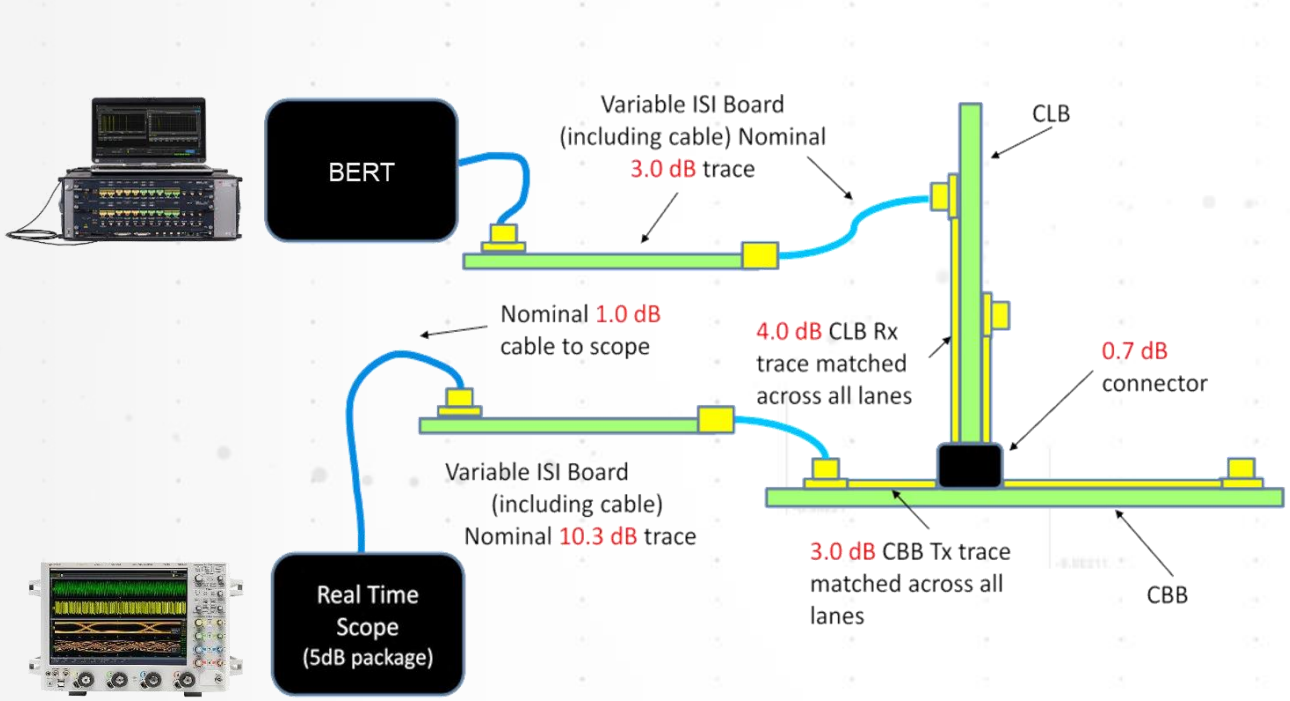
M8020A J-BERT

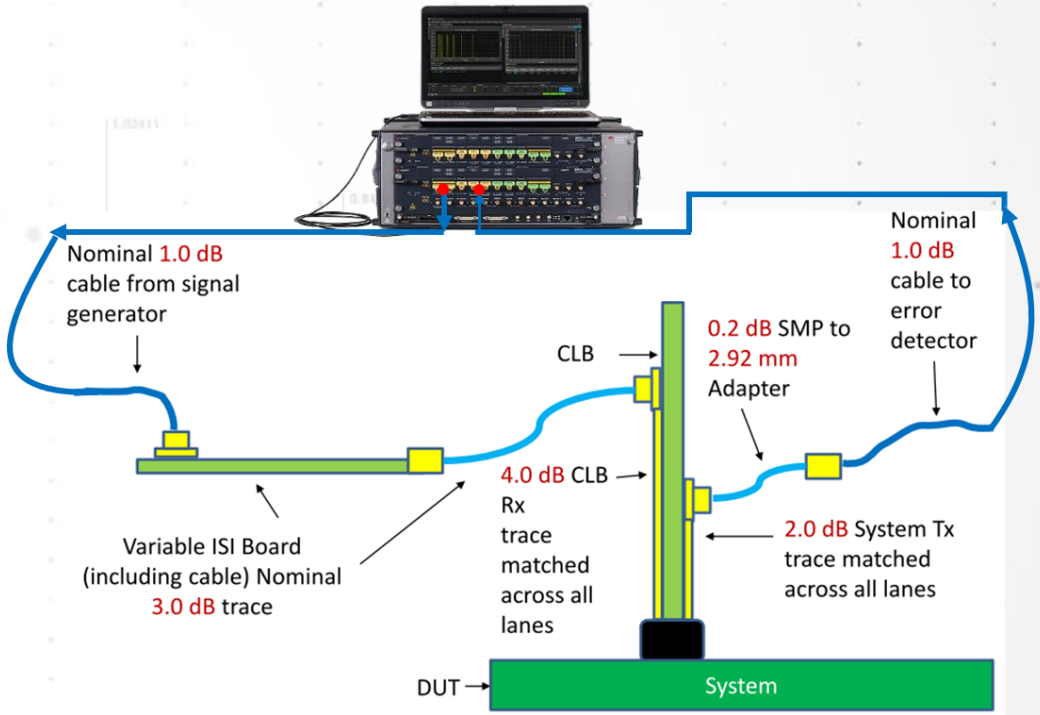
Integrated ISI for streamlined RX Test Setups and accurate Results:

- Adjustable loss and frequency up to **25dB @16GHz**
- Import of S-parameters
- Multiple channels
- Programmable
- Upgradeable option

PCIe 4.0 CEM Receiver Tests

16GT/s CEM Specification – System RX Calibration and Test

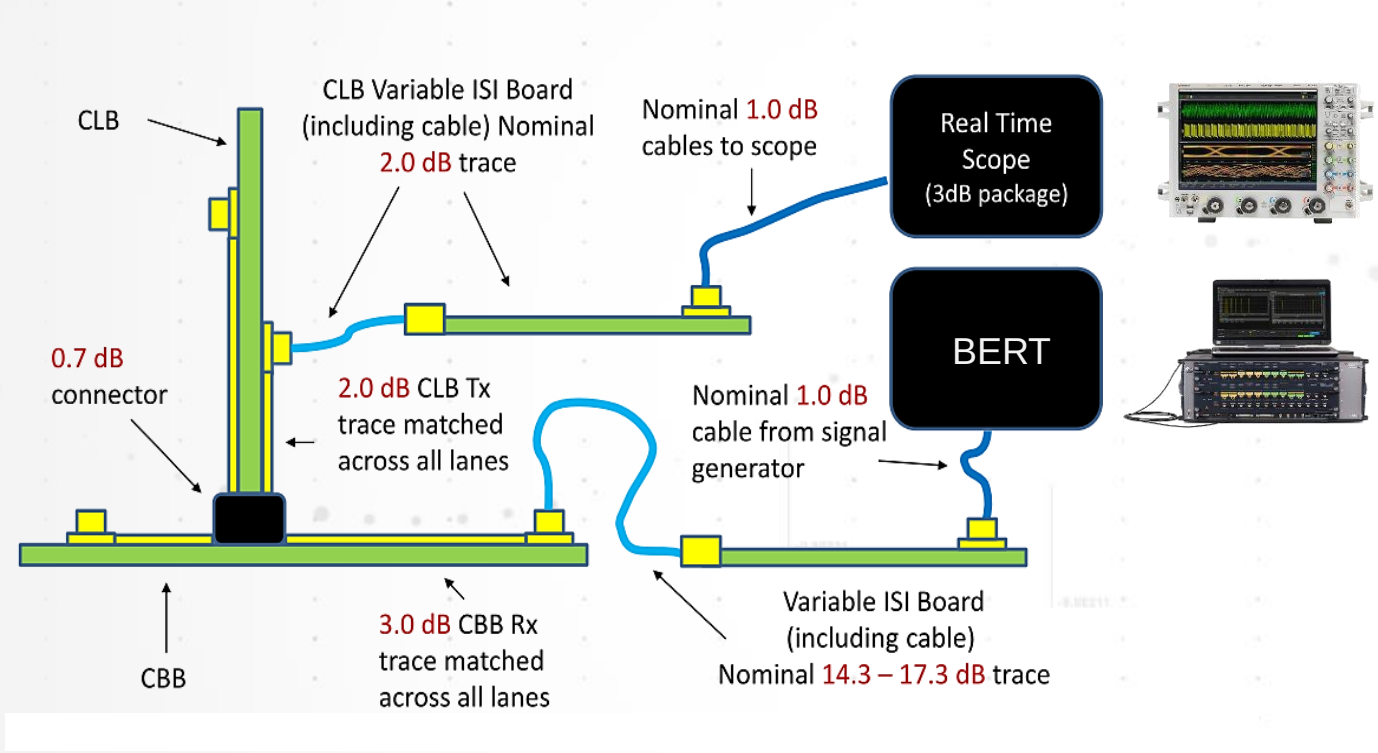


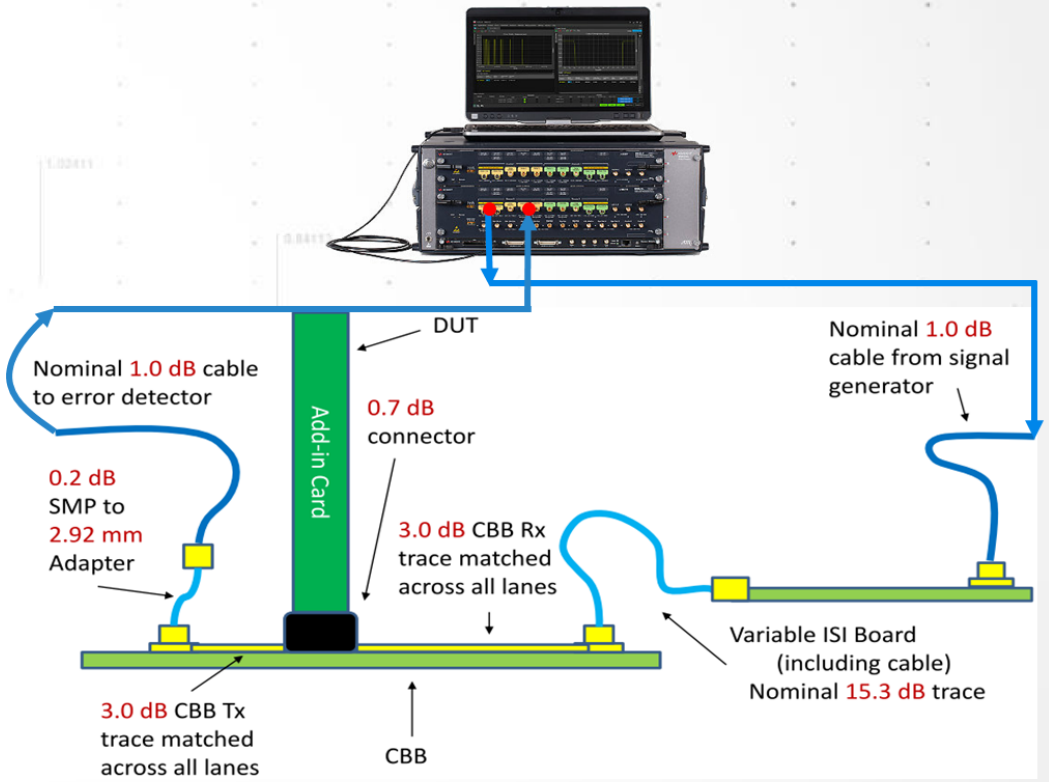


Note: This RX test proposal utilizes an external variable ISI board to ensure consistent insertion loss of the test setup.

PCIe 4.0 CEM Receiver Tests

16GT/s CEM Specification – AIC RX Calibration and Test

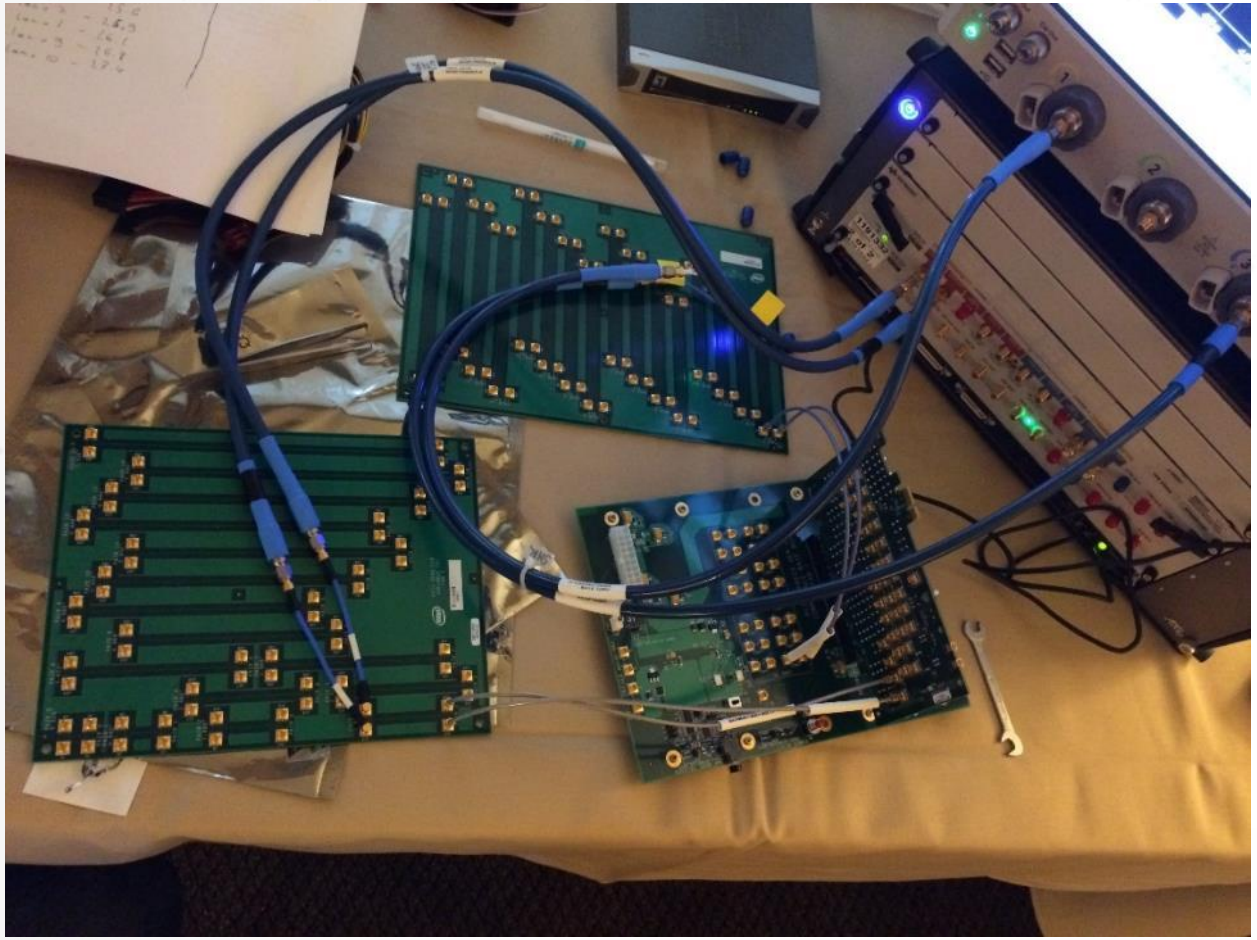




Note: This RX test proposal utilizes an external variable ISI board to ensure consistent insertion loss of the test setup.

PCIe 4.0 CEM Test Setup

Calibration Setup Example For 16GT/s RX

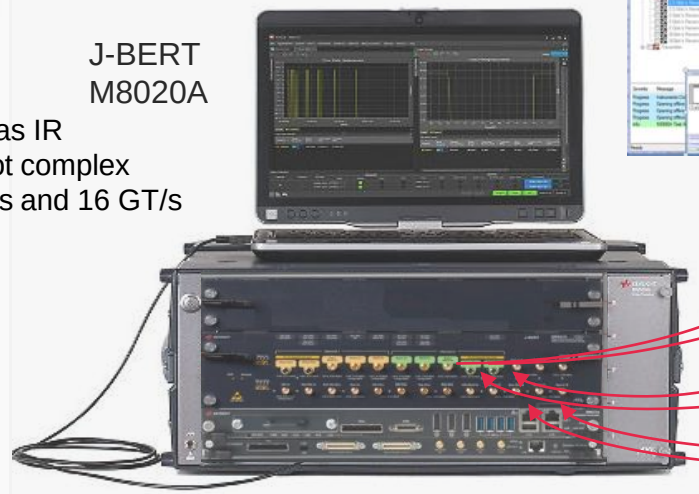


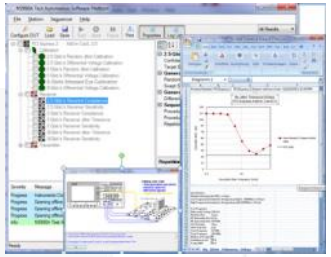
- CBB 4.0 as well as CLB 4.0 need to be combined with ISI trace boards
- CEM calibration procedure is very similar to base spec calibration but SIGTEST instead of SEASIM is mandatory
- J-BERT M8020A successfully tested most of the 16 GT/s AICs and systems at PCIe WS 101
- Many AICs and systems could be trained to loopback using the new LTSSM

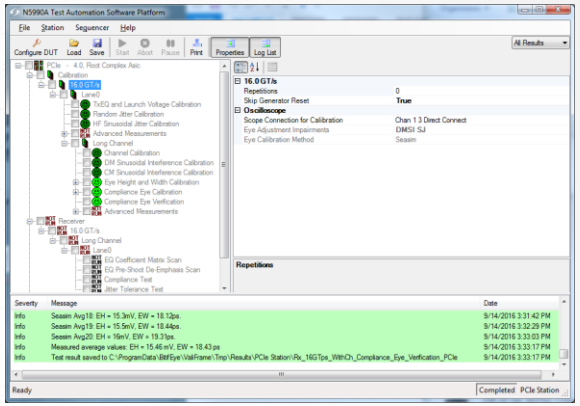
PCIe 3.0/4.0 RX Test Solution - now

Latest Generation

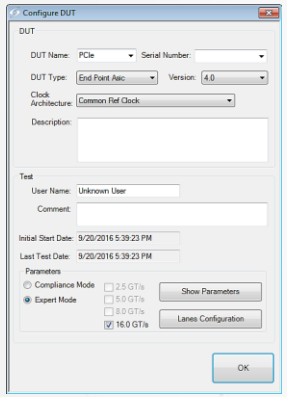
J-BERT
M8020A

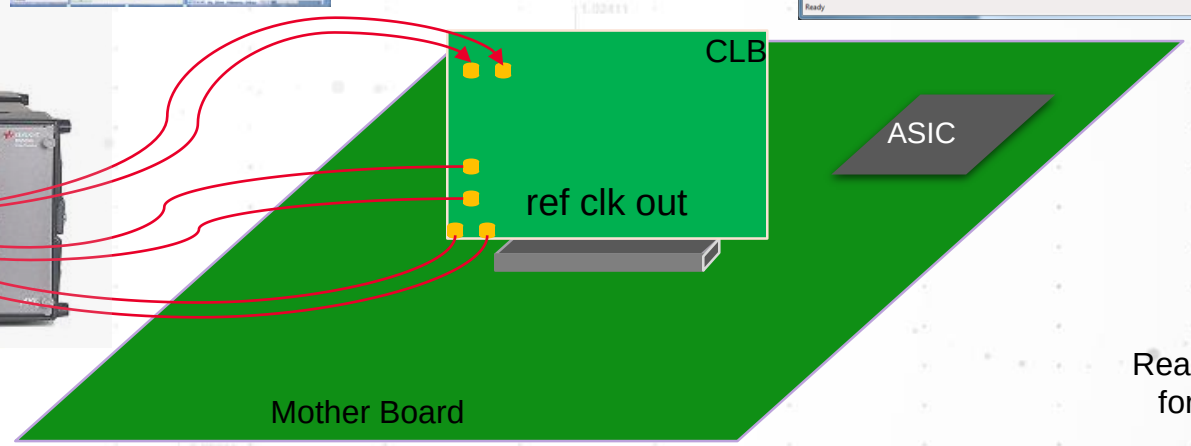






Support for CC as well as IR
End point as well as root complex
2.5 GT/s, 5 GT/s, 8 GT/s and 16 GT/s

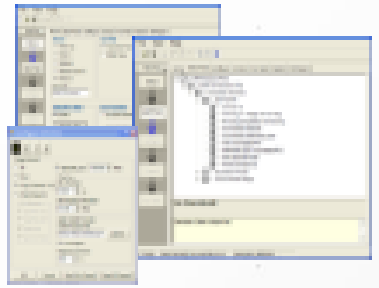




Real Time Scope
for calibration

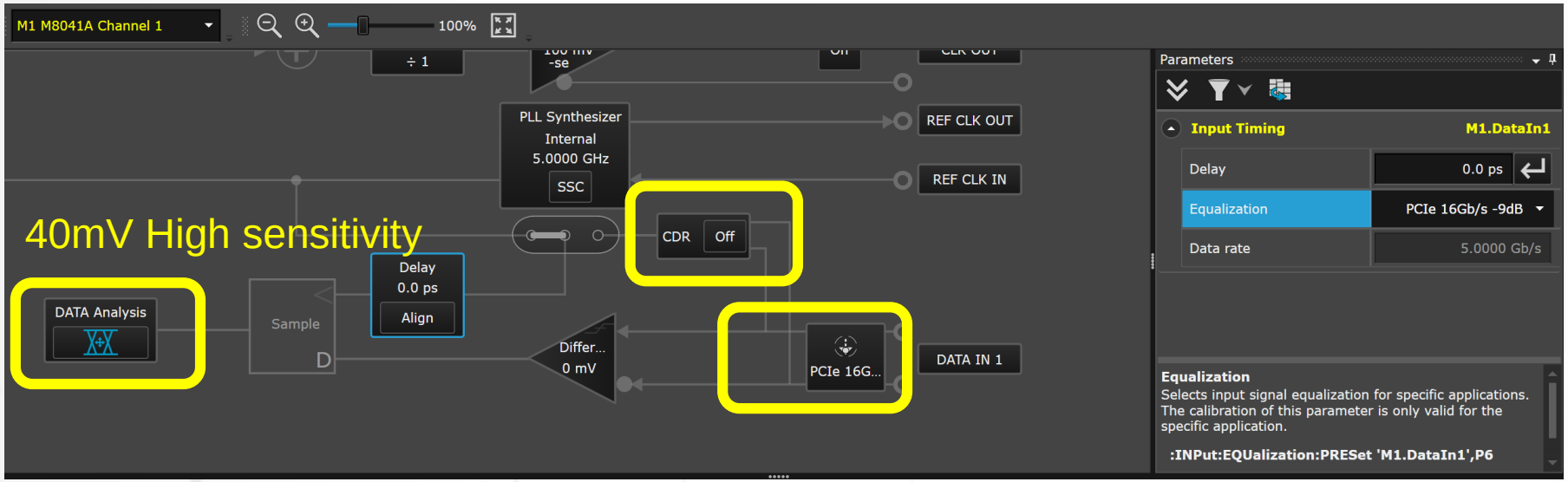
J-BERT M8020A (8-32 Gb/s)

- **Interactive Training Function**
- **Build in Jitter Sources /DMI + CMI source**
- **Build in CDR and analyzer equalization**
- **Build in 8 Tap De-emphasis**
- **Build Adjustable ISI**
- **Support fully programmable**



Key of Successful PCIe Gen4 Rx testing: CTLE & CDR

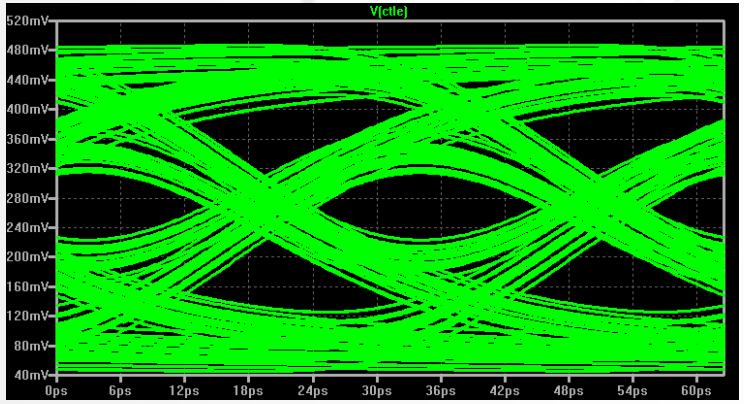
BERT ED GET CHALLENGE WITH LONG TRACE

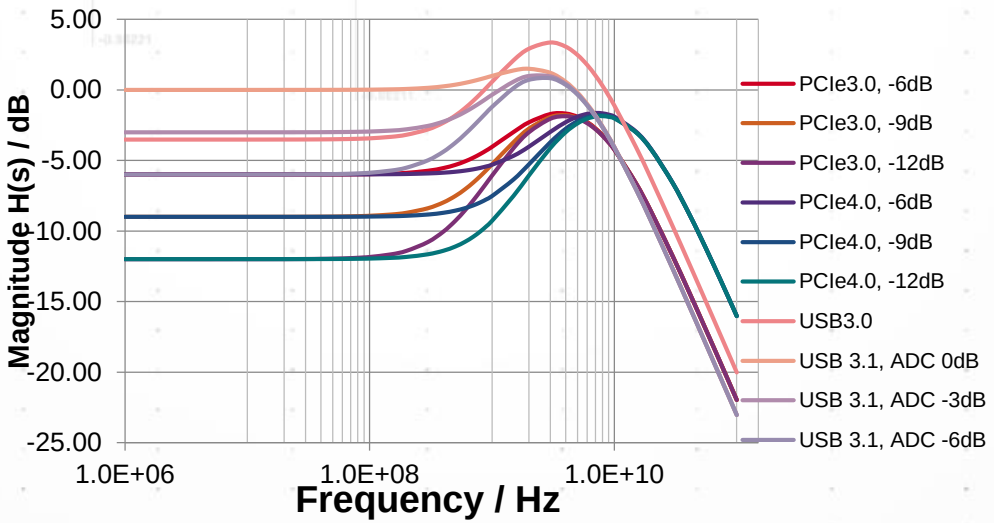


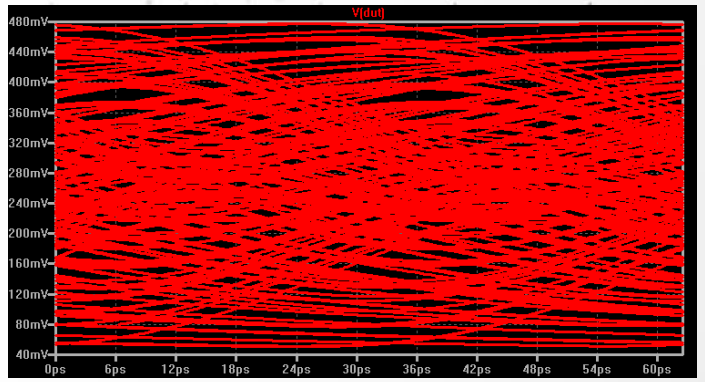
The Key with Error Free:

- No additional loss with integrated CDR

Tx signal after > 10 inches







Example: System board Gen4 Rx Test Report

BEAUTIFUL TEST REPORT WITH DETAIL INFORMATION

KEYSIGHT TECHNOLOGIES

BitifEye Digital Test Solutions

○ Show all results
◉ Show only selected

Print

- L0_Cal_16GTps_IniPres_EH
- L0_Cal_16GTps_IniPres_EW
- L0_Cal_16GTps_Chan_EH
- L0_Cal_16GTps_Chan_EW
- L0_Cal_16GTps_FinPres_EH
- L0_Cal_16GTps_FinPres_EW
- L0_Cal_16GTps_PreComp
- L0_Cal_16GTps_CompEye
- L0_Rx_16GTps_Comp
- L0_EqRx_16GTps_Comp_2.12.2

Product Number: PCIe PCIe Station Unknown User 05/12/2018 12:00:40

L0_EqRx_16GTps_Comp_2.12.2

for PCIe 4.0 System

Random Jitter	1 ps
Sinusoidal Jitter	10 ps
Differential Mode Sinusoidal Interference	17 mV
Generator Launch Voltage	800 mV
Offline	False
CLB var. ISI pair	2
Total Channel Loss	-29.9 dB
Sinusoidal Jitter Frequency	100 MHz
Common Mode Sinusoidal Interference	150 mV
Enable Impairments for Loopback Training	True
BER Mode	FixedTime
BER Measurement Duration	62.5 s
Allowed Bit Error	1
Interactive Training Script File	C:\ProgramData\BitifEye\ValiFrame`
Default Link Training Lane Number for every Lane	Auto
Suppress Loopback Training Messages	False
Use Gen3 EIEOS	False
DUT Target Preset	P5
DUT Target Preset Gen4	P5
Speed Change Control	DUT
Drop Link Method	LTSSM

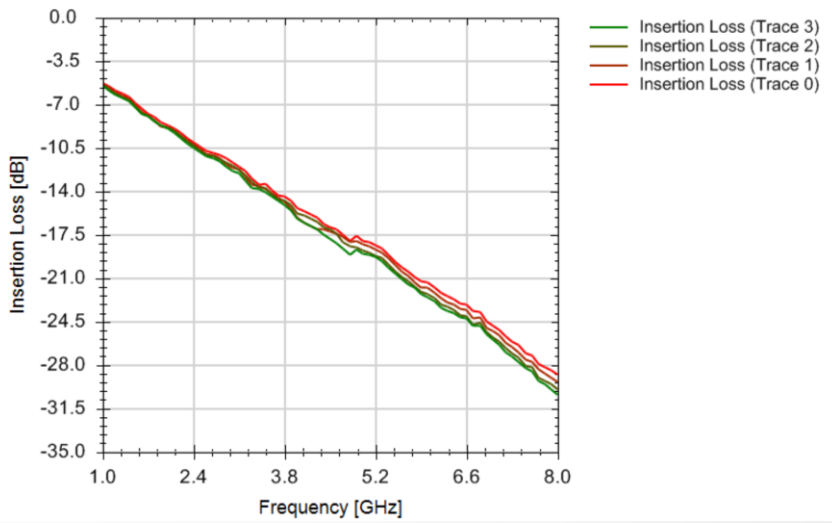
Drop Link Method	LTSSM
Use CDR	True
CDR Loop Bandwidth	20 MHz
Peaking	1 dB
Analyzer Equalization	-9 dB
Sensitivity	High
Polarity	Normal
Capture and Compare Mode	False
Pause before Auto-Align	False
Relax Time	3 s

Result	Final Generator Preset	Final Generator Pre-shoot [dB]	Final Generator De-emphasis [dB]	Allowed Bit Errors []	Measured Bit Errors []
pass	P5	1.90	0.00	1	0

Product Number: PCIe PCIe Station Unknown User 04/12/2018 21:00:57

L0_Cal_16GTps_IL

for PCIe 4.0 System



Agenda

- PCI Express 4.0 Simulation and Case Study
- PCI Express 4.0 Timeline and 5.0 Roadmap
- PCI Express 4.0 TX / LTSSM Link EQ / RX Testing
- **PCI Express 5.0 Preview**

PCIe Gen5 Preliminary Goals

PCIE Base Spec Ver:0.5

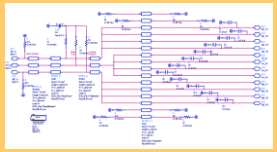
PCI Express® Base Specification Revision 5.0 Version 0.9

PCI-SIG 18 October 2018

- Signaling rate: 32GT/s NRZ (no PAM4)
- Channel loss target is: -36dB @ 16GHz (Nyquist), Package Loss RC -9dB, EP -4dB
- PCIe 5.0 base specification compliant PHYs must support both common clock and SRIS clocking architectures
- Reference Clock is reduced from 300 ppm to 100 ppm, Phase Jitter: ≤ 250fs RMS
- BER target is 1e-12
- 2nd order CTLE and 3-tap DFE for 32GT/s
- TX Presets P0-P10 to remain the same
- Backward compatibility with previous PCIe Gen1/2/3/4
- Same TX Voltage parameters as Gen4
- Same approach for TX and RX testing used for Gen4
  - Similar method for TX testing via de-embedding of breakout board traces
  - Similar method for calibrating the eye width and eye height as used with PCIe 4.0 (ISI based, fixed RJ)

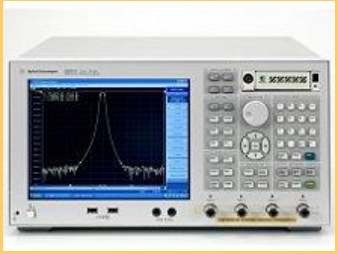
PCI Express® 4.0 – Keysight Total Solution

Physical layer – interconnect design



ADS design software

DCAX 86100D N1055A TDR

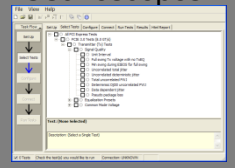


PNA PLTS / E5071C ENA option TDR

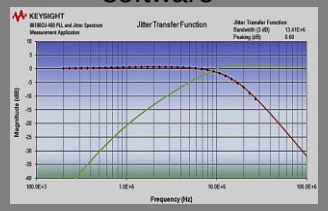
Verify PCIe 4.0 Compliant Channels
Verify Return Loss Compliance

Physical layer-transmitter test

V-Series, Z-Series Real-Time Oscilloscopes



N5393F PCI Express 4.0 TX Electrical compliance software



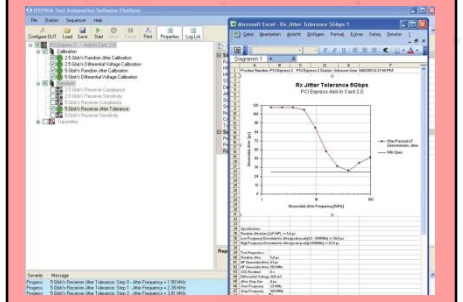
86100DU-400 PLL and Jitter Spectrum Measurement SW

DSA V-series & Z-Series Real-Time Oscilloscopes

Physical layer-receiver test

M8020/40A J-BERT High Perfformance, Protocol Aware BERT

N5990A automated compliance and device characterization test software



Automated RX Test software
- Accurate, Efficient
- Comprehensive RX Testing