400G/CEI 4.0 Characterization and Compliance Testing

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Keysight Technologies, Inc.	

Agenda

- Introduction – What is happening with the data center networking standards?
- Output (Transmitter) Testing Updates – Rob Sleigh
  - Optical
  - Electrical
- Input (Receiver) Testing Updates – Steve Sekel
  - Deep dive on 802.3 Annex 120E C2M
- Summary & Wrap-up

State of the '400G Class' Standards (Current Generation - 50 G lane rate)

✓ • IEEE 802.3~~bs~~ 200/400GBaseE Medium reach SMF + C2C,C2M PAM4 @ 53.1 & 26.6 Gbaud	Released, Clauses 121 – 124, Annex 120D/120E
✓ • OIF CEI-56G 5 reaches PAM4 up to 29 Gbaud, NRZ up to 58 Gb/s	Released and published in CEI_4.0
• 802.3cd: 50/100/200GBaseE Short reach MMF. + C2C,C2M, backplanes & cables PAM4 @ 26.6 Gbaud	Nearing completion (Resolving TDECQ measurement issues)
✓ • 64G Fibre Channel Short & medium reach in MMF & SMF PAM4 @ 28.9 Gbaud	Nearing completion (Waiting for 802.3 to resolve TDECQ measurement issues)
• 802.3cm 400G in MMF	Project start in September
• 802.3cn 50/100/200/400G >10 km SMF	Project start in September
• COBO version 1.0	Released (Optical PHY from 802.3bs, Elec. From OIF-CEI-56G-VSR)

Important note on preleased standards

- Very dynamic (even in the late ballot stages)
- Check for latest draft before running ‘pre-compliance’ testing
- Verify which draft version any built-in measurements are based on

Transmitter Characterization

- Optical TX Test
- Electrical TX Test

Patterns

TEST PATTERNS FOR PAM4 ENCODED SIGNALS DEFINED IN IEEE 802.3BS/CD

- **JP03A** - The JP03A test pattern is a repeating {0,3} sequence (clock)
  – No longer used in 802.3bs/cd.

- **JP03B** - The JP03B test pattern is a repeating sequence of {0,3} repeated 15 times followed by {3,0} repeated 16 times (clock with a phase shift)
  - No longer used in 802.3bs/cd

PAM4 Test Patterns		
Pattern	**Pattern Description**	**Defined in Clause**
Square Wave	Square wave (8 threes, 8 zeros)	120.5.11.2.4
3	PRBS31Q	120.5.11.2.2
4	PRBS13Q	120.5.11.2.1
5	Scrambled Idle	119.2.4.9
6	SSPRQ	120.5.11.2.3

- **PRBS13Q** - The PRBS13Q test pattern is a repeating 8191-symbol sequence formed by Gray coding pairs of bits from two repetitions of the PRBS13 pattern into PAM4 symbols as described in 120.5.7. (Note: PRBS13Q is different from QPRBS13 defined in IEEE 802.3-2015 (bj) Clause 94). Used for victim channel in TX tests.

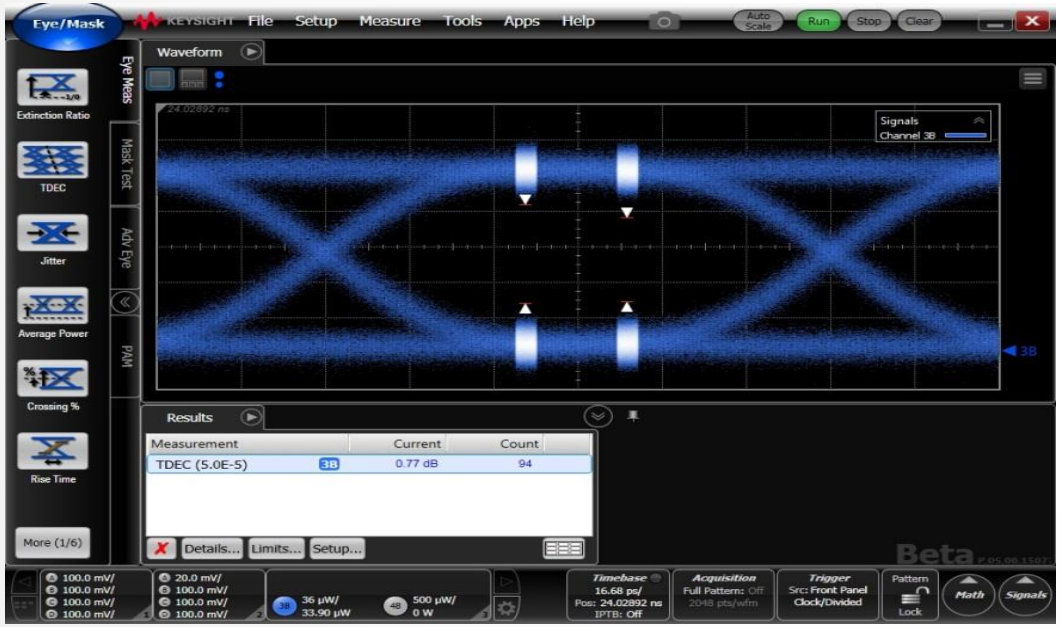
- **PRBS31Q** - The PRBS31Q test pattern is a repeating 2^31-1 symbol sequence formed by Gray coding pairs of bits from two repetitions of the PRBS31 pattern defined in 49.2.8 into PAM4 symbols as described in 120.5.7. Used for victim channel in RX tests and aggressor lanes in TX/RX tests.

- **SSPRQ** – Short Stress Pattern Random Quaternary.
  The SSPRQ pattern is a repeating 2^16–1 PAM4 symbol sequence. Comprised of 4 sequences, each based key “stressors” from PRBS31. Stressful pattern, but short enough to use advanced analysis tools available on today’s T&M tools (e.g. Equalization, Jitter/Noise analysis, etc.). Used for Optical TX test.

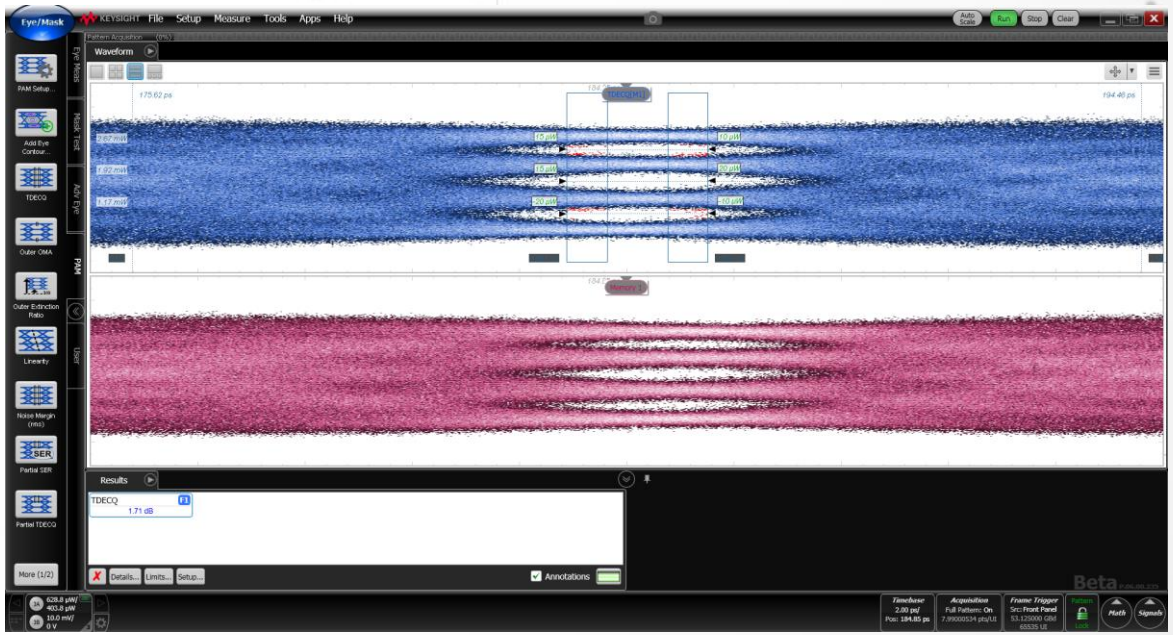
Optical Measurement Differences: NRZ vs PAM4

USE OF FORWARD ERROR CORRECTION (FEC) RESULTS IN MAJOR CHANGES TO TX TEST

- **Primary NRZ transmitter tests:**
  - OMA (optical modulation amplitude)
  - Extinction Ratio (ER)
  - Eye-mask
  - NEW!: Transmitter Dispersion and Eye Closure (TDEC) replaces Transmitter Dispersion Penalty (TDP) for new 25G and 50G TX



- **Primary PAM4 transmitter tests:**
  - Outer OMA
  - Outer Extinction Ratio
  - NEW!: **No** eye-mask
  - NEW!: TDECQ replaces TDP
  - NEW! Transition Time (IEEE 802.3cd)

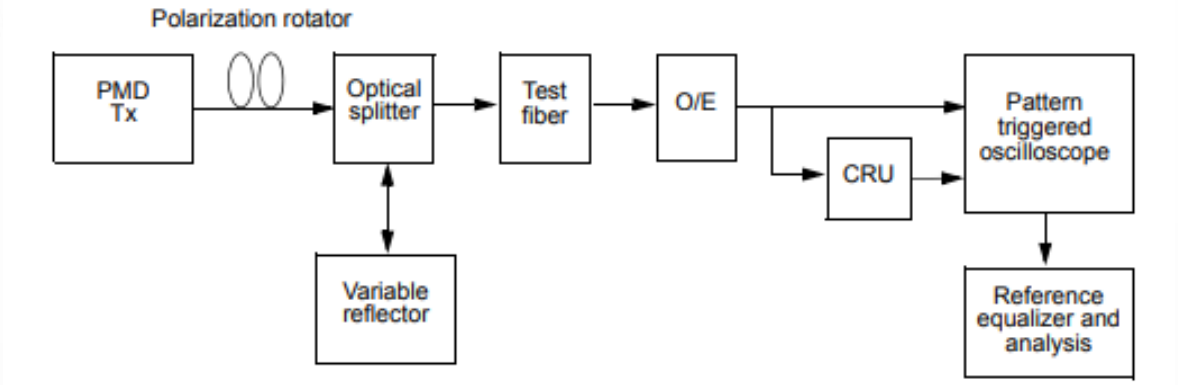


TDECQ

TRANSMITTER DISPERSION AND EYE CLOSURE QUATERNARY

- Tells you the performance of your transmitter relative to an ideal transmitter
- For NRZ TDP, we literally used a BERT to measure the BER performance of the transmitter compared to an actual (real) golden transmitter
  - Determine how much extra power was required at the receiver to compensate for non-ideal performance

- For TDECQ we indirectly measure SER (symbol error rate) using a scope, no BERT required.



Reference: IEEE P802.3bs™/D3.5, 10th October 2017, Figure 121-4, page 222.

TDECQ measurement process (from IEEE 802.3bs)

- SSPRQ test pattern (~2^16 length) (Short Stress Pattern Repetitive Quartenary)
- Includes test fiber dispersion
- Oscilloscope noise measured and mathematically ‘backed out’
- Virtual 5 tap, T spaced FFE reference equalizer optimizes eye openings (to minimize TDECQ penalty).
- Histograms constructed to assess eye closure relative to OMA and **compute an effective power penalty in dB. This is the TDECQ result**

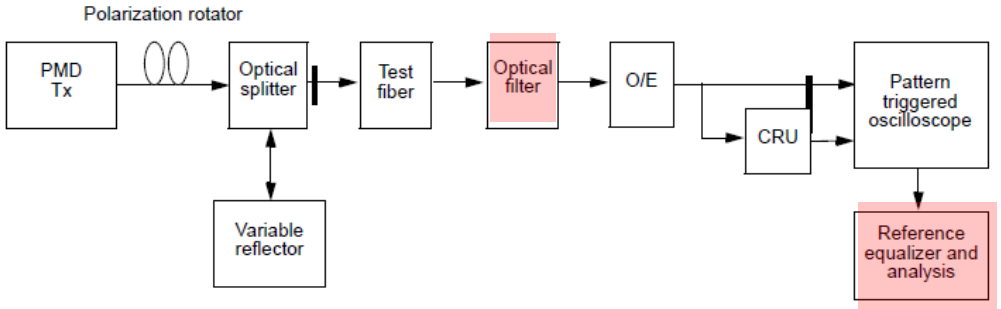


Figure 122–4—TDECQ conformance test block diagram

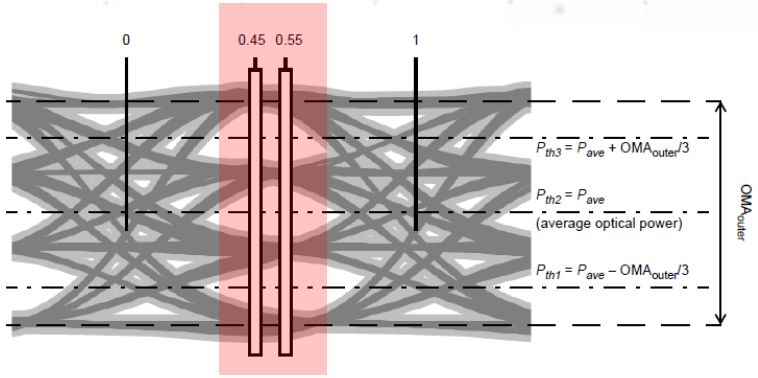


Figure 121–5—Illustration of the TDECQ measurement

Reference: IEEE P802.3bs™/D3.5, 10th October 2017, Figure 121-5, page 222, 224.

TDECQ has evolved during the development of IEEE 802.3bs (400G Ethernet) and 802.3cd (50/100G)

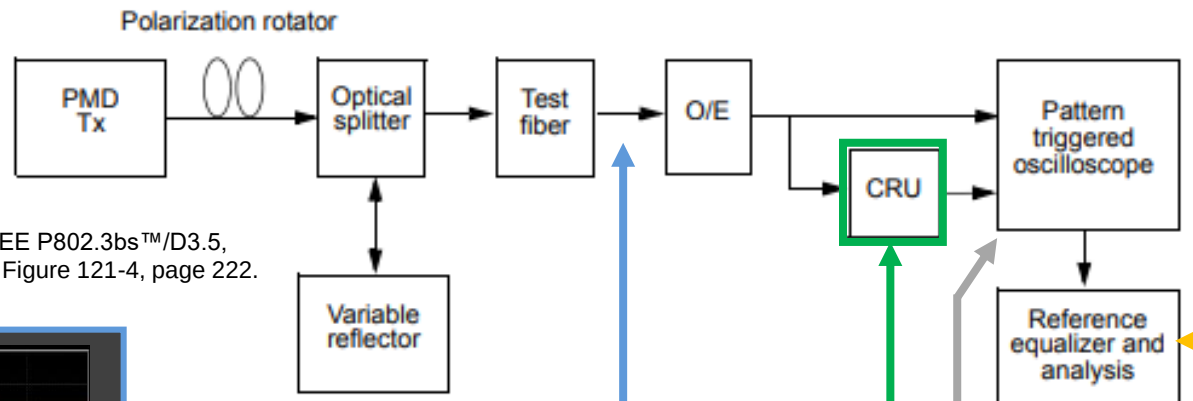
- **Early versions**
  - Optimized virtual equalizer to minimize the spread of the eye levels (e.g. open up the eye)
  - T/2 spaced virtual equalizer
  - Oscilloscope bandwidth a classic Bessel-Thomson response (BW = 75% of baud rate)
  - Measurement made at two time slices located on each side of the eye center
  - Measurement uses ideal decision thresholds based on OMA

In each case, the changes were made to better represent the typical system that the transmitter would operate in. In most cases this is representative of how real system receivers are expected to operate.

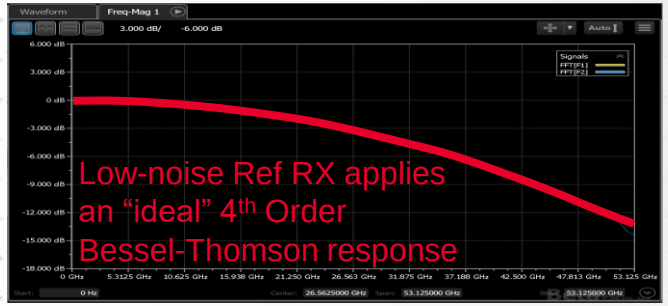
- **Final version**
  - Optimized to minimize the TDECQ penalty
  - T-spaced virtual equalizer
  - Nyquist scope bandwidth (50% of baud rate) with Bessel-Thomson response
    - 26.56 Gbd: 13.28 GHz (802.3bs), 11.2 GHz (802.3cd)
    - 53.13 Gbd: 26.56 GHz
  - Measurement time position allowed to be optimized for minimum TDECQ penalty
  - Decision thresholds allowed to vary from ideal (variation up to 1% of OMA, 802.3cd, likely inclusion in 802.3bs through a revision project)
  - Constraints being considered for preventing transmitters that are equalizable but likely not able to operate with typical receivers (should be finalized in the coming months)

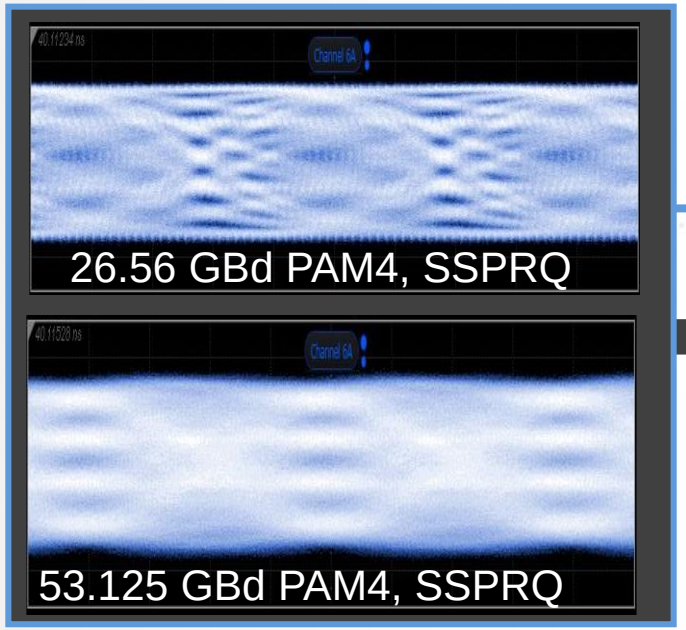
TDECQ Measurement Setup

REQUIRES ACCURATE OPTICAL REF RX AND ROBUST CLOCK RECOVERY DESIGN



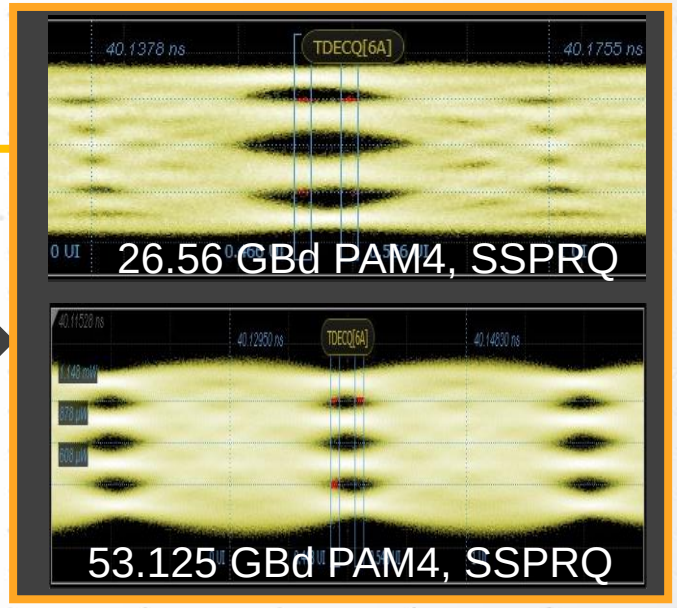
Reference: IEEE P802.3bs™/D3.5, 10th Oct 2017, Figure 121-4, page 222.

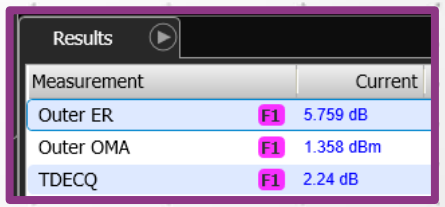




CRU (N1078A)

Reference RX (N1092A DCA-M)



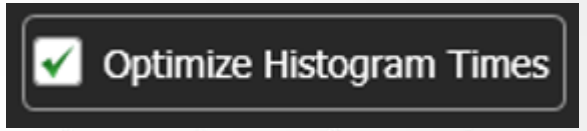


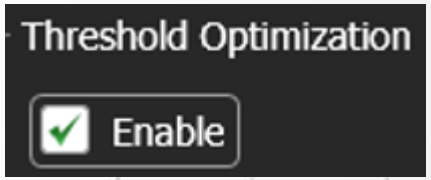
Screen captures of actual degraded signals used in the N1078A production test process.

TDECQ: Measurement Tips

CHOOSE A MEASUREMENT SOLUTION THAT IS FAST, FLEXIBLE, AND ACCURATE

- **Compliant TDECQ measurements require:**
  - **Histogram optimization** (adjust left and right)
    (IEEE 802.3bs D3.5, IEEE802.3cd D3.2)
  - **Threshold optimization** (adjust up and down)
    (IEEE 802.3cd D3.4, likely will be added to 802.3bs in a maintenance release)
  - **Recommendation:** keep these **enabled at all times** (they have a minimal impact on throughput, but can have a large impact on result).





- **Recommendations for throughput optimization:**
  - Iterative "tap" optimization – typically results in a 0.1dB to 0.2dB difference in TDECQ (signal dependent). Consider disabling this feature to increase throughput (e.g. in production test).
  - "Seed" equalizer tap values for faster tap optimization
  - Consider using a more powerful CPU to perform your TDECQ measurements, especially for parallel TDECQ testing (4 channels)

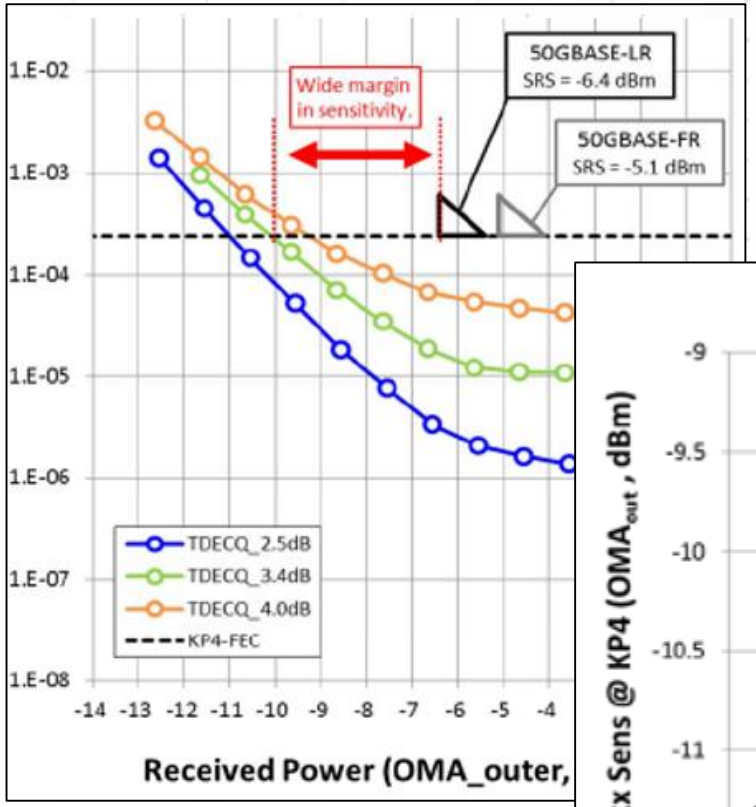
TDECQ: Does it work as designed?

POWER PENALTY VALUES PROVIDED BY THE FINAL IMPLEMENTATION OF TDECQ CORRELATE DIRECTLY TO OBSERVED RECEIVER SENSITIVITY

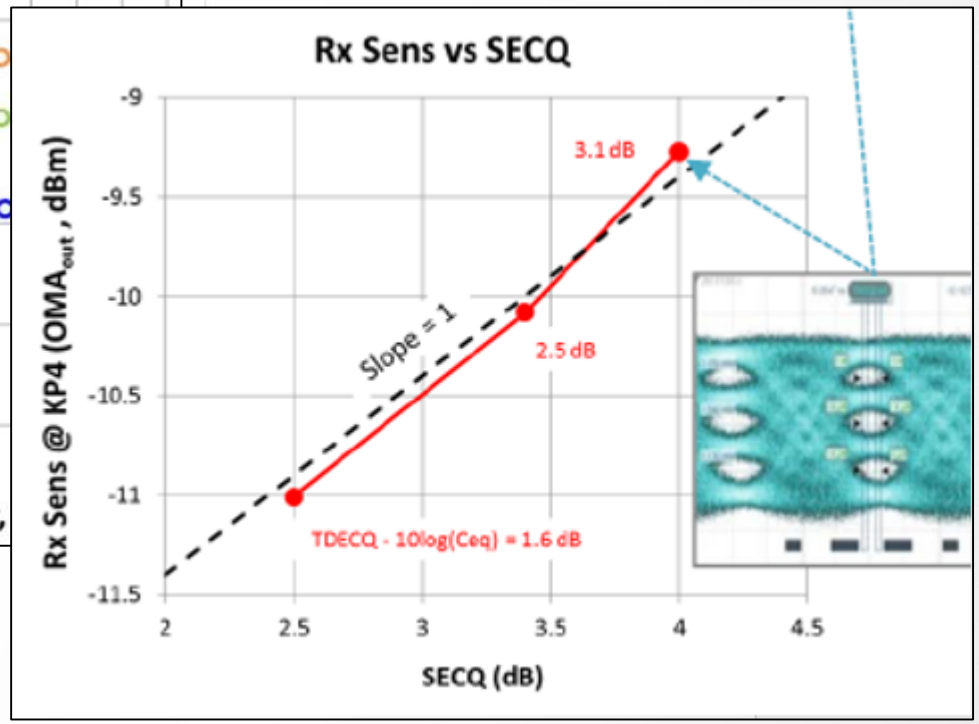
Consider a typical PAM4 receiver and two transmitters A and B. If the TDECQ of transmitter A is 2 dB and for transmitter B is 3.2 dB, should I be able to make any predictions about the power levels required at the receiver to achieve a specific BER/SER with each transmitter?

Latest results from IEEE 802.3cd project:

http://grouper.ieee.org/groups/802/3/cd/public/July18/tamura_3cd_01c_0718.pdf
(used with permission from the author)



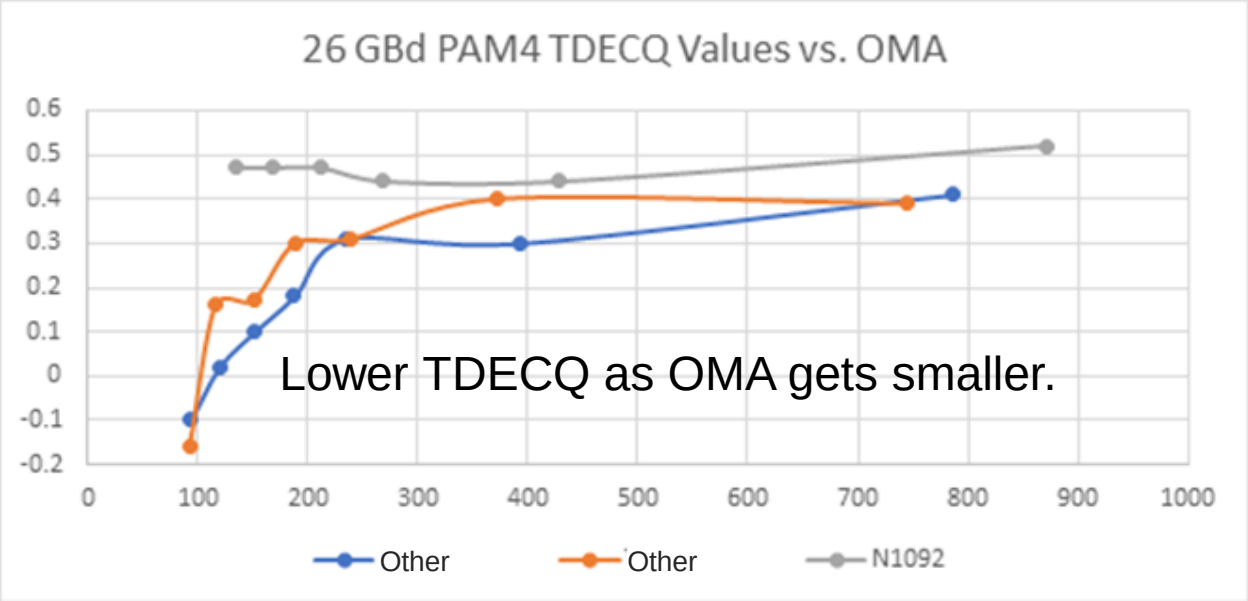
As the TDECQ receiver definition was refined, excellent correlation is seen with real transceivers.

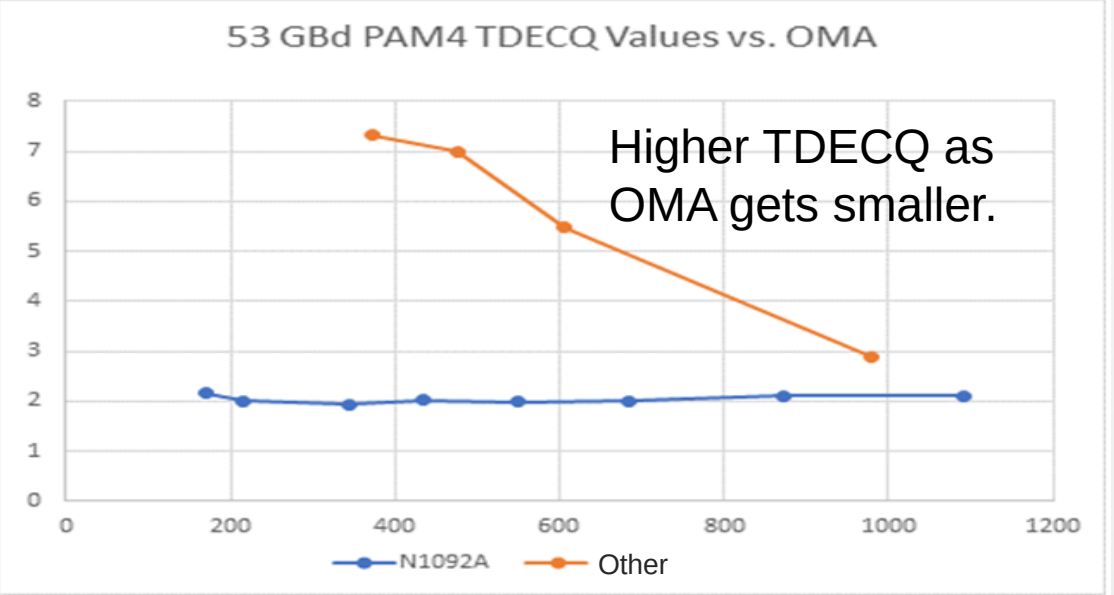


TDECQ: What to watch out for as signal level is lowered…

ARE YOU GETTING UNEXPECTED RESULTS?

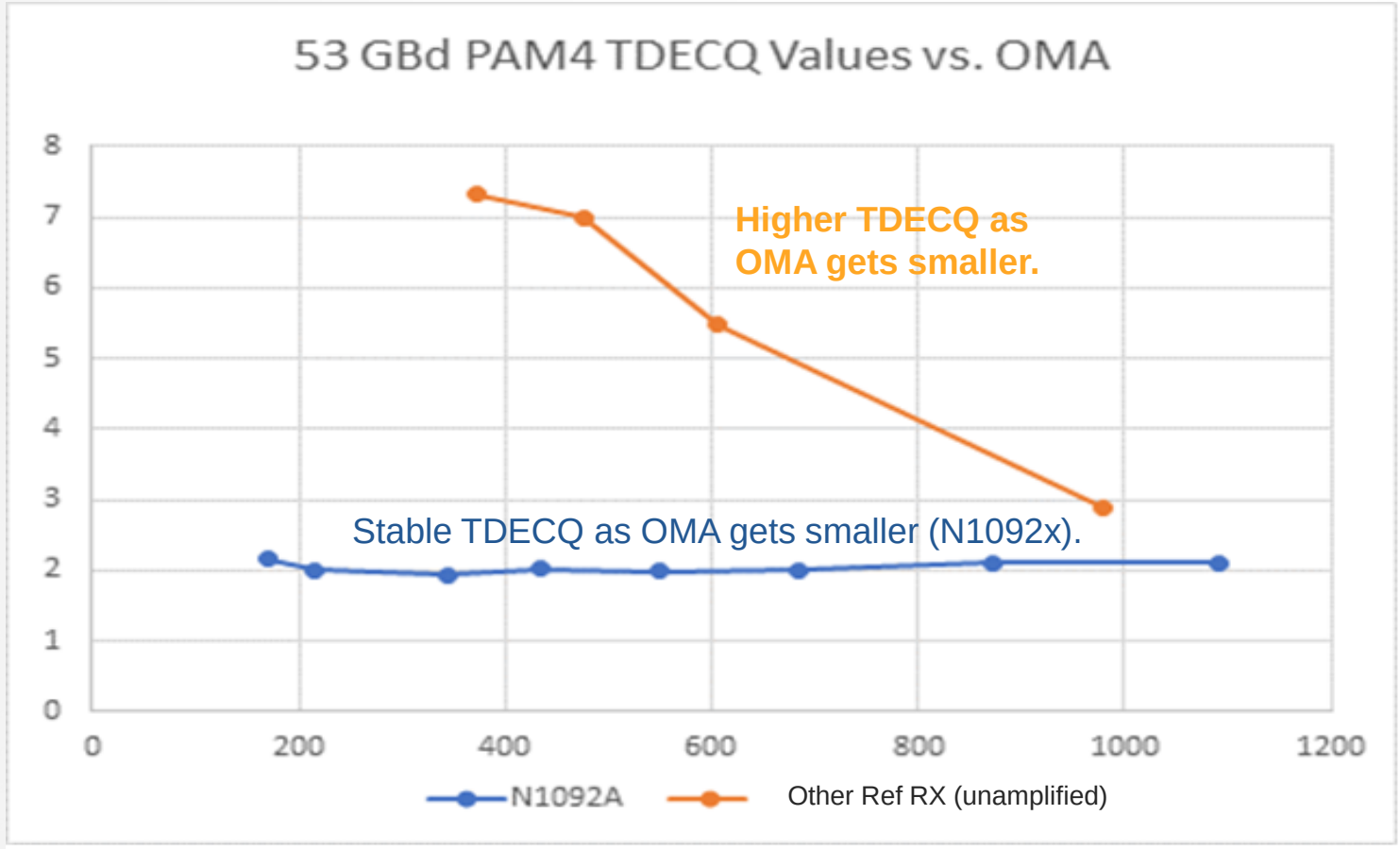
- Signal attenuation should not alter the TDECQ value
- Oscilloscope noise is mathematically removed in the TDECQ calculation. Are there practical limits to this process?
- If TDECQ errors occur with small signal levels, what direction do we expect the result to go?
- Have you observed a TDECQ result that changes as OMA gets lower (worse)?





TDECQ - what happens as OMA gets smaller?

HIGH NOISE RECEIVERS CAN IMPACT TDECQ ACCURACY

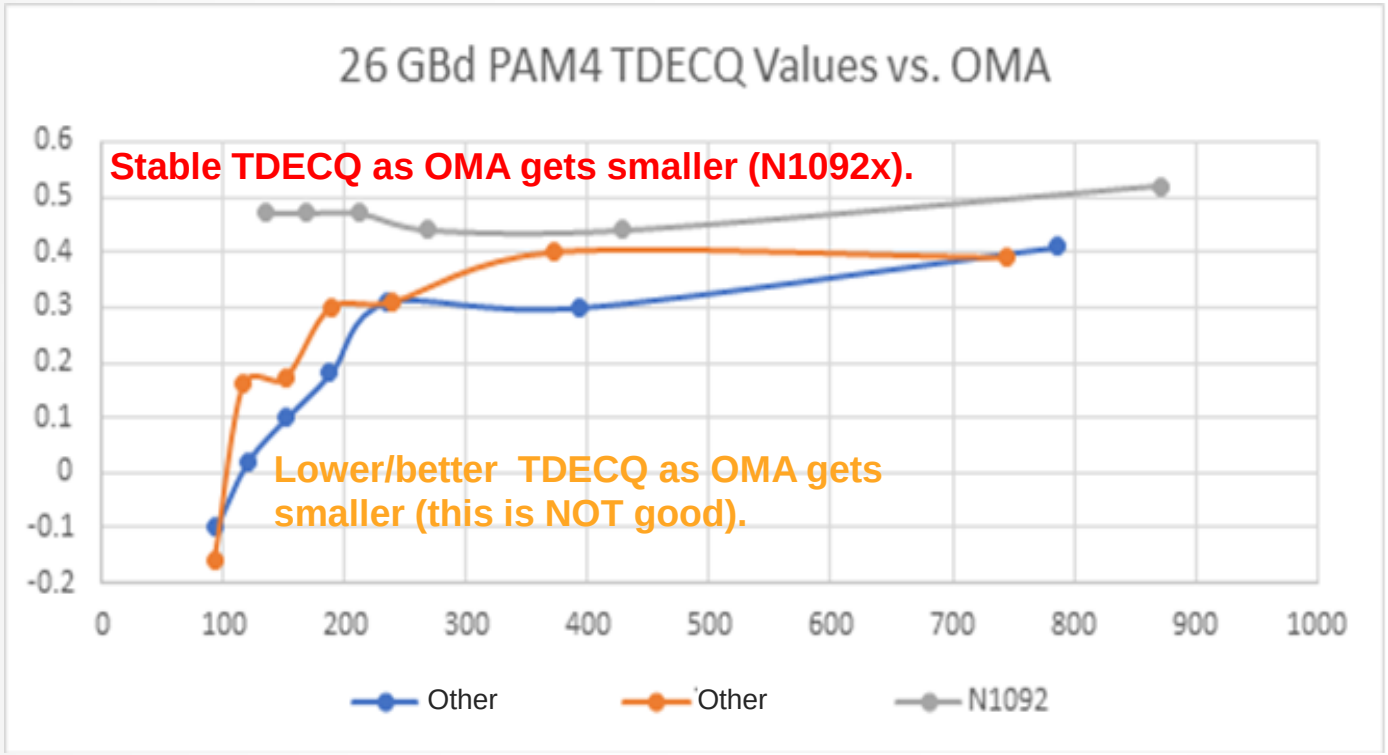


High BW receivers will often have higher intrinsic noise that will impact TDECQ accuracy on low-level signals.

Recommendation: Use a low noise reference receiver whenever possible. (e.g. Keysight N1092x) and remember to perform vertical calibrations to allow accurate corrections of internal noise (module calibration with no light).

TDECQ - what happens as OMA gets smaller?

DEGRADED (CLOSED) EYE SIGNALS CAN IMPACT TDECQ ACCURACY



Closed eye signals:

1. Degraded samples can get misinterpreted to a nearby level (SW thinks it is correct, but it's not).

2. Misinterpreted samples can lead to a better TDECQ result than expected ("lower TDECQ is not always the right answer")

Recommendation: Use thoroughly tested TDECQ algorithms.
(e.g. Keysight FlexDCA FW Rev 5.8 and later).

Transmitter Transition Time for Optical PAM4

NEW MEASUREMENTS ADDED TO IEEE 802.3CD

Transmitter transition time is defined as the **slower** of the time interval of the rising/falling transitions of a PAM4 signal.

Test Conditions:

- 20% to 80% of Outer OMA levels
- Measured with Square Wave or SSPRQ pattern.
  - SSPRQ: Use specific symbol sequences
    - 00000333333 (rise time)
    - 33333000000 (fall time)
  - Measured with specific Ref RX BW and 4th Order BT response

Keysight Oscilloscope Solutions for Optical 400G/TDECQ

FULL COVERAGE FOR ALL OPTICAL 26/53 GBD PAM4 APPLICATIONS

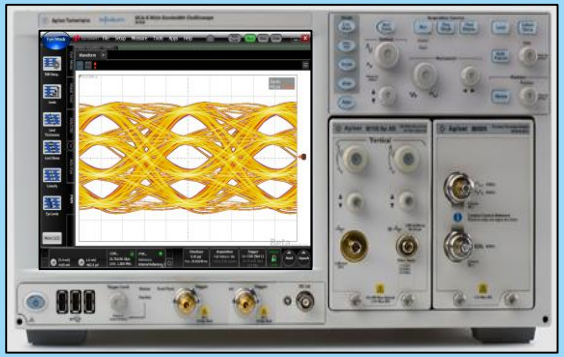
N1092A/B/D “DCA-M”

- 20-28 GBd NRZ Ref Receiver
- 26 AND 53 GBd TDECQ Ref Receiver
- Multimode and Single-Mode
- 1, 2 or 4 channels
- High sensitivity receiver design (low noise receiver)
- Fastest sampling combined with 160fs typical trigger jitter
- Lowest cost 4 channel solution
- “Ideal” frequency response (option IRC)
- TDECQ with Option TFP or 9FP

86100D DCA-X with 86105D/86115D module

- 8.5 GBd to 28 GBd incl 26G TDECQ Ref Receiver
- Multimode and Single-Mode
- 1 or 2 @ 34 GHz optical channels (1 to 4 optical per mainframe)
- 1 @ 50 GHz Electrical Channel
- “Ideal” frequency response (option IRC)
- < 100 fs rms timebase jitter (86100D-PTB)
- TDECQ with Option TFP or 9FP

86100D DCA-X with 86116C module



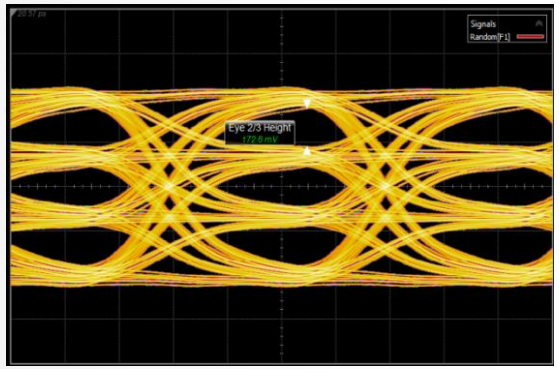
- 25/26/28GBd (OPT 025)
- TDECQ Ref Receiver 26G (opt 025) 53G (opt 041)
- Single-Mode
- 1 @ optical channel per module
- 1 @ 80 GHz Electrical Channel
- “Ideal” frequency response (option IRC)
- < 100 fs rms timebase jitter (86100D-PTB)
- TDECQ with Option TFP or 9FP

Including compliant optical/electrical clock recovery solutions (N1078A) for 26/53 GBd applications!

Output (Transmitter) Characterization:
Key PAM4 Electrical Measurements

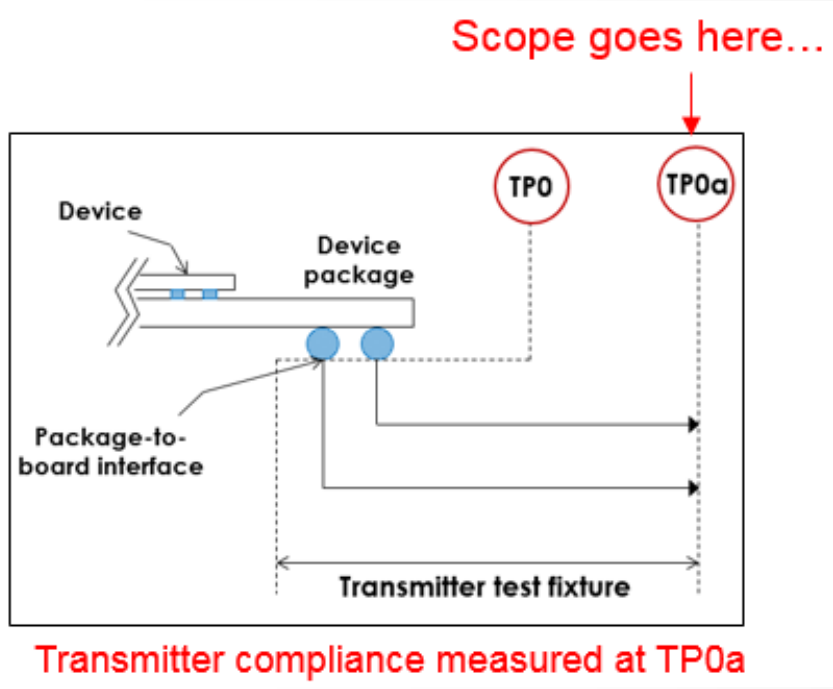
Key PAM4 Measurements for Electrical Transmitters

IEEE 802.3BS ANNEX 120D 200GAUI-4 AND 400GAUI-8 (TP0A)



What are the key PAM-4 TX parameters that get measured?

- **Output waveform**
  - Level Separation Mismatch Ratio
- **Signal-to-noise-and-distortion ratio** (SNDR)
  (Note – there is still some debate over SNDR specs in IEEE 802.3cd)
- **Output Jitter**
  - J_{RMS}
  - J3u, J4u
  - Even-Odd Jitter (EOJ)



Transmitter compliance measured at TP0a

Output Jitter (J3u/J4u, J_{RMS}, and EOJ)

NEW MEASUREMENTS PERFORMED ON 12 SPECIFIC EDGES OF A PRBS13Q PATTERN

- J3u/J4u, J_{RMS}, and Even-Odd Jitter (EOJ)… you may recognize some of these acronyms from other (older) Standards
- So they should be pretty straight forward to measure, right?
- **While the IEEE Output Jitter names may sound familiar, they are measured very differently!**
  - Traditional Jn (e.g. J5, J9) and EOJ parameters were measured using all edges of an NRZ pattern.
  - IEEE 802.3bs/cd now measure J3u (802.3cd) and J4u (802.3bs), J_{RMS}, and EOJ on 12 specific edges of a PRBS13Q (PAM4) pattern!

Table 120D–4—PRBS13Q pattern symbols used for jitter measurement

Label	Description	Gray coded PAM4 symbols	Index of first symbol	Index transition begins	Index transition ends	Index of last symbol	Threshold level
REF	Reference for symbol index	3333333	1	—	—	7	—
R03	0 to 3 rise	10000 330	1830	1834	1835	1837	$(V_0+V_3)/2$
F30	3 to 0 fall	23333 001	1269	1273	1274	1276	
R12	1 to 2 rise	0111111 2222221	3638	3644	3645	3651	$(V_1+V_2)/2$
F21	2 to 1 fall	022222 113	1198	1203	1204	1206	
R01	0 to 1 rise	100000 113	6835	6840	6841	6843	$(V_0+V_1)/2$
F10	1 to 0 fall	21111 003	2992	2996	2997	2999	
R23	2 to 3 rise	32222 330	6824	6828	6829	6831	$(V_2+V_3)/2$
F32	3 to 2 fall	033333 2222223	7734	7739	7740	7746	
R02	0 to 2 rise	10000 223	3266	3270	3271	3273	$(V_0+V_2)/2$
F20	2 to 0 fall	122222 0000002	7282	7287	7288	7294	
R13	1 to 3 rise	011111 331	133	138	139	141	$(V_1+V_3)/2$
F31	3 to 1 fall	23333 112	7905	7909	7910	7912	

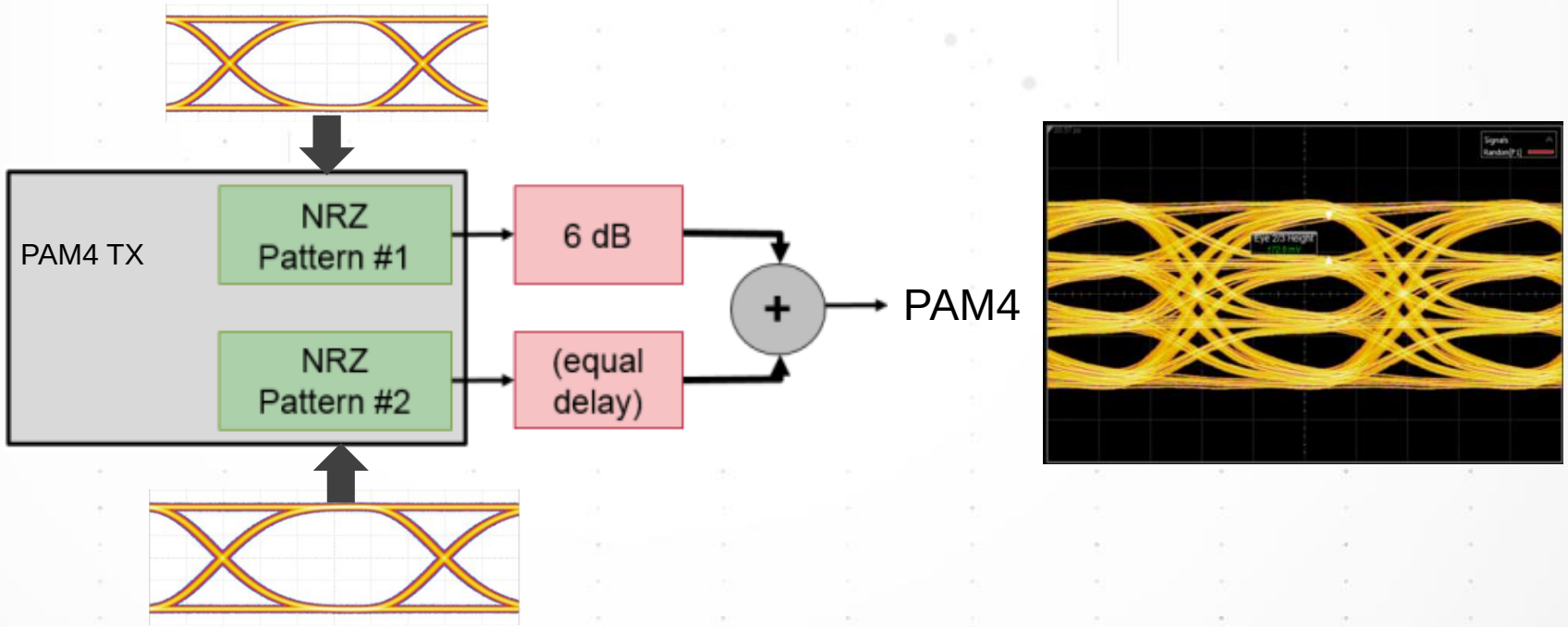
Reference: IEEE P802.3bs™/D3.5, 10th October 2017, page 357.

So don't just pull out your scope and press the Jn (J2, J5, J9) or EOJ button in Jitter Mode!

Why did the PAM4 jitter measurement methodology change?

NEW METHOD IMPLEMENTED IN IEEE 802.3BS/CD AND CEI-56G-MR/LR-PAM4

- Different TX Architectures are used to generate PAM4 signals
- Some TX designs may use different clock buffers for MSB and LSB; this can result in different uncorrelated jitter appearing on different edges.
- Measuring jitter only on JP03 (clock) patterns (original method) could miss potential issues.



Measure Output Jitter at TP0a

"12-EDGE" OUTPUT JITTER MEASURED ON KEYSIGHT DCA AND RT SCOPES

New "12 edge" jitter method in FlexDCA reduced test time from hours to < 1 minute.

- **J3u/J4u and J_{RMS} jitter**
  - Measure RJ/PJ on 12 specific transitions using a PRBS13Q pattern (exclude correlated jitter).
  - Data from all edges is combined and analyzed

- **Even-Odd Jitter (EOJ)**
  - Measured on PRBS13Q (3 repeats)
  - Max from measurements on all 12 edges

- **Keysight DCA and RT Scopes** report:
  - J3u/J4u, J_{RMS}, EOJ "ALL" measurement (per the Standard)
  - FlexDCA also reports individual results for each of the 12 edges
    - Rise: 0 to 3, 1 to 2, 0 to 1, 2 to 3, 0 to 2, 1 to 3
    - Fall: 3 to 0, 2 to 1, 1 to 0, 3 to 2, 2 to 0, 3 to 1

Measurement Setup:
- Receiver: 4th Order Bessel-Thomson low-pass filter with 33 GHz BW
- CR PLL BW 4 MHz and a slope of 20 dB/decade

Output Jitter

Src: D1A Rate: 26.562533 GBd Pat. Length: 8191

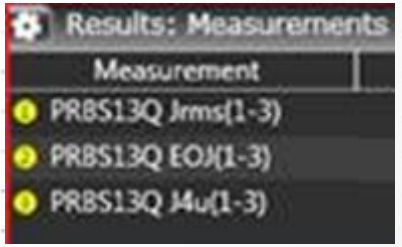
Measurement	Current
J4u (All)	1.6 ps
Jrms (All)	240 fs
EOJ (All)	450 fs

FlexDCA DCA Results

Output Jitter

Src: D5A Rate: 26.562500 GBd Pat. Length: 8191

Measurement	To L0	To L1	To L2	To L3
J4u (All)	1.968 ps			
From L3	1.709 ps	1.754 ps	2.052 ps	---
From L2	1.781 ps	2.026 ps	---	2.032 ps
From L1	2.078 ps	---	2.056 ps	1.762 ps
From L0	---	2.028 ps	1.762 ps	1.739 ps



RT Scope Results

TX Test at TP1a

REQUIRES COMPLIANT REF RX AND ROBUST CLOCK RECOVERY DESIGN

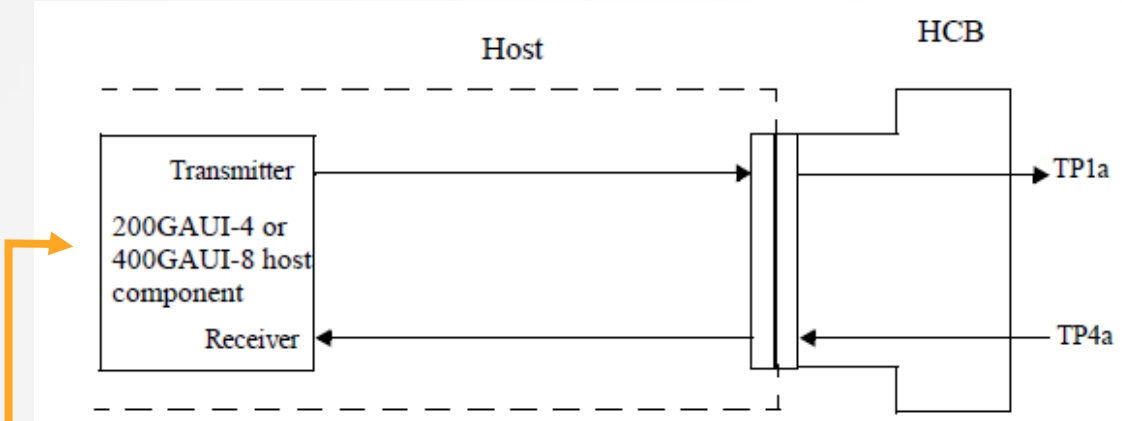
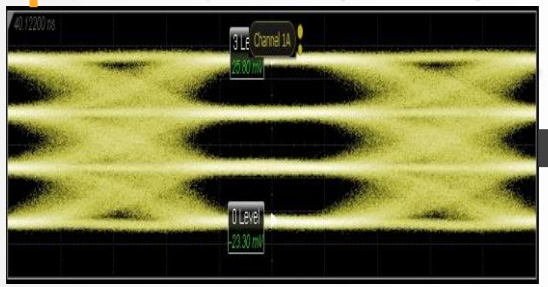
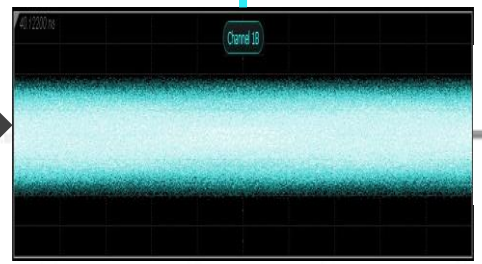


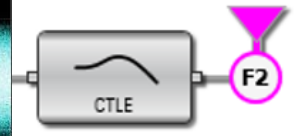
Figure 120E–5—Host 200GAUI-4 or 400GAUI-8 C2M compliance points

Total Loss per Spec: 12.2 dB

- Channel Loss: 10.5dB
- Host TX Package Loss: 1.7 dB







Keysight UXR-Series
Real-time Oscilloscope

Keysight DCA-X Family
Equivalent-time Oscilloscope

- Screen captures of actual degraded signals used in the N1076B/N1078A Hardware CR production test process
- Tested with “closed eyes” at 26/53 GBd (e.g. CR locks at 26 GBd with IL > 20dB loss at 13.28 GHz)

Keysight Oscilloscope Solutions - Electrical

HIGHEST PERFORMING SOLUTIONS FOR TESTING 400G/PAM4 DESIGNS

Electrical – Equivalent-Time (Sampling) Scope

New

Keysight N1000A DCA-X with N1060A "MegaModule"
(includes built-in clock recovery and precision timebase)

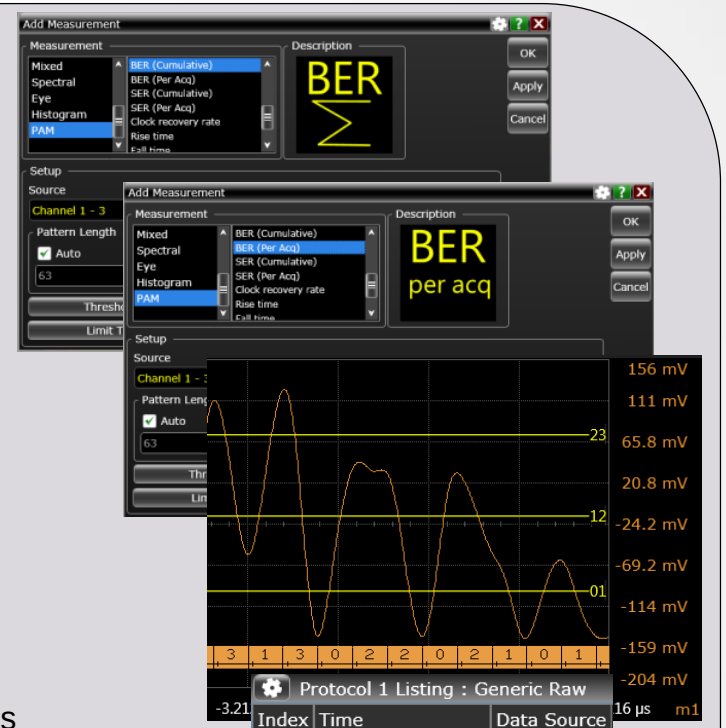
- Channels: 2
- Bandwidth: 50 GHz / 85 GHz (95 GHz typ)
- Jitter: < 50 fs rms typ.
- Electrical Clock Recovery – integrated HW Clock Recovery works with PAM4 signals up to 64 Gbaud
- 86100D-9FP PAM-4 Analysis SW (works with any DCA module, optical or electrical)
- N1091BSCA IEEE 802.3bs/cd
- N109256CA CEI-4.0 (56G-VSR/MR/LR)
- **NOTE – 75 / 85 / 100+ GHZ BW remote head modules also available.**

New

Electrical – Real-time Scope

Keysight UXR-Series

- Channels 2-4
- Bandwidth: up to 110 GHz
- Sample Rate: 256 GSa/s on all channels
- PAM-4 Serial Data Analysis Wizard
- Software Clock Recovery
- N8827A/B PAM-4 Analysis SW
- N6472A/N6473A PAM4 SW Applications
- PAM-4 SER/BER "Error Capture" and "Decode" capabilities
- Use as a PAM4 Error Detector with M8070A BERT SW



Index	Time	Data Source
3	-3.2125266079 µs	0
4	-3.2124881448 µs	2
5	-3.2124496817 µs	2
6	-3.2124112186 µs	2
7	-3.2123727554 µs	3
8	-3.2123342923 µs	3
9	-3.2122958292 µs	3
10	-3.2122573660 µs	2
11	-3.2122189029 µs	3
12	-3.2121804398 µs	2
13	-3.2121419766 µs	0

Keysight Z-Series scopes are also well suited for PAM4 analysis.

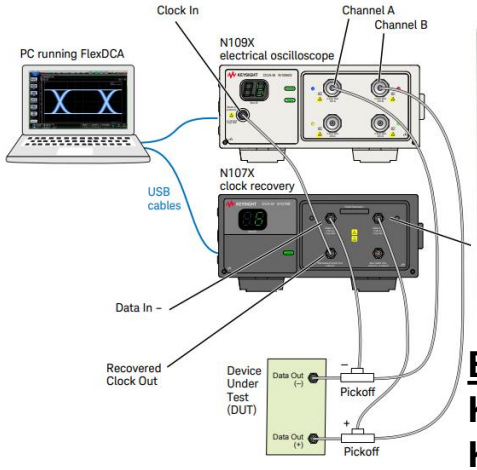
New TX Test Automation SW Apps for Keysight Scopes

AUTOMATED TX TEST FOR IEEE 802.3BS/CD AND CEI-56G-VSR/MR/LR

- **Electrical TX Test Automation SW for IEEE 802.3bs/cd**
  - Updated to IEEE 802.3bs Draft 3.5 including “12 edge” Output Jitter
  - Expanded coverage to include TX test for IEEE 802.3cd
  - **N6472A SW App for RT Scopes**
  - **N1091BSCA SW App for DCA platform**

Electrical – Real-time Scope
Keysight DSO Z-Series

- **Electrical TX Test Automation SW for OIF-CEI-4.0 56G VSR/MR/LR**
  - Updated to final CEI-4.0 Implementation Agreement (IA)
  - Expanded coverage to include TX test for 56G-MR/LR
  - **N6473A SW App for RT Scopes**
  - **N109256CA SW App for DCA platform**



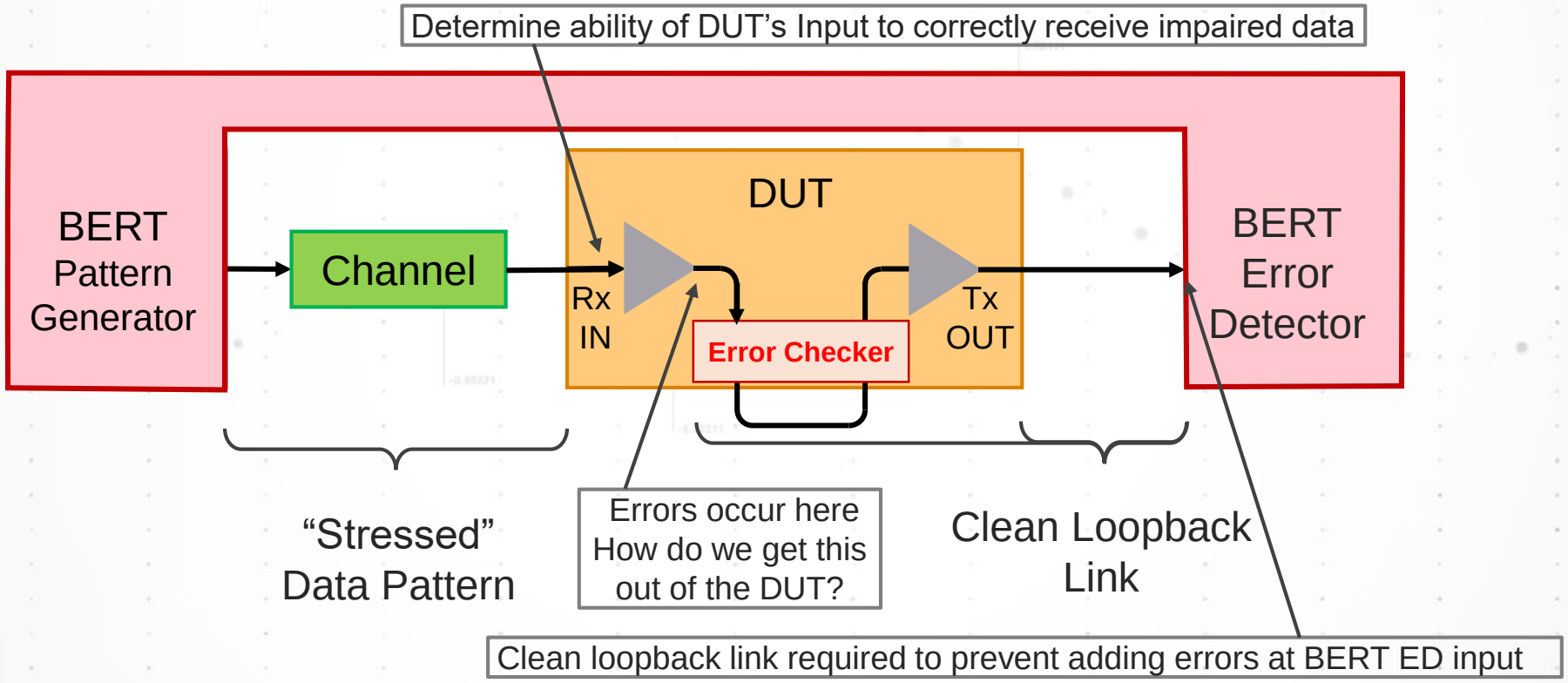
Electrical – Sampling Scope
Keysight 86100D/N1000A DCA-X
Keysight N109xA DCA-M

Receiver Testing

Input Testing Links Which Don’t Run Error Free (by design)

- The Bit Error Ratio Tester will continue to be the principle tool for Input testing, with modified set-up

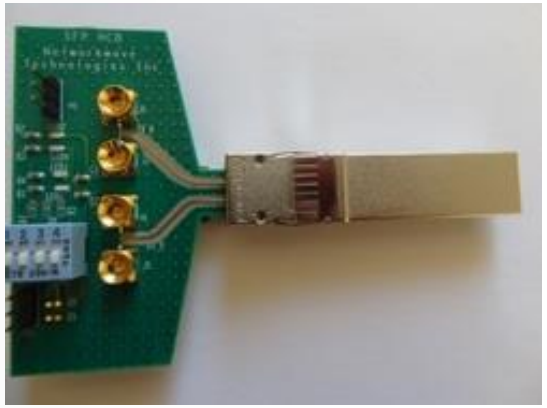
Traditional BERT Input test setup:



- Will the loopback path be error free in links designed to use FEC for error free operation?

Chip to Module tests

- Use a pair of compliance boards
  - Host Compliance Boards – emulate the optical module
  - Module Compliance Boards – emulate the host (switch card)
  - Both are required for stress calibration - even if you are only testing a host or a module



  - S parameters verified as a mated pair, but some standards suggests allocation for each board
  - Validate your compliance boards before using them !!!

Test point definition

Standardized naming convention used in parameter reference tables

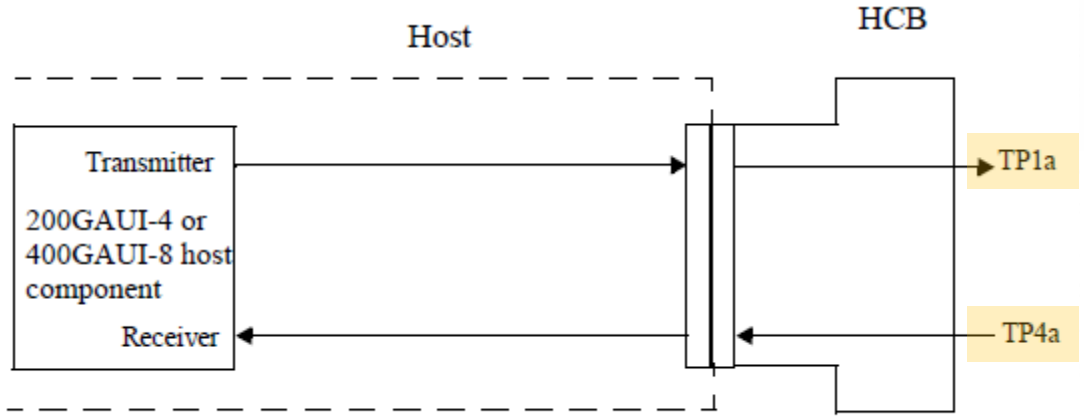


Figure 120E–5—Host 200GAUI-4 or 400GAUI-8 compliance points

Output tests: Scope de-embedded to TP1A

Input tests: Stressed pattern calibrated at TP4, through mated HCB + MCB

Input tests: Stressed pattern calibrated at TP1a, through mated MCB + HCB

Output tests:: Scope de-embedded to TP4

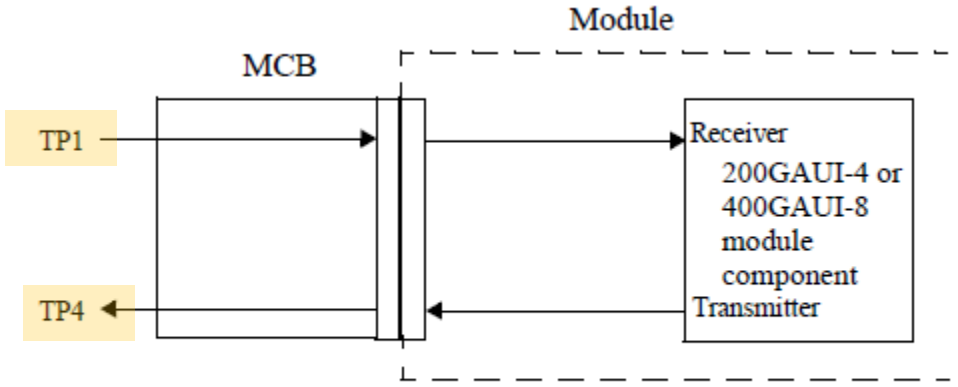


Figure 120E–6—Module 200GAUI-4 or 400GAUI-8 compliance points

Reference: IEEE 802.3bs draft D3p5 page 370

IEEE 802.3bs / cd C2M AUI Input Test (Annex 120E

Host Input test

- All Input testing performed with a series of 5 stressed input tests
  - No interference test for C2M AUI
- ‘Classical’ stress mix: Sinusoidal Jitter, Random Jitter, Bounded Uncorrelated Jitter
  - 5 tests differ only in SJ frequency and amplitude (PLL Tracking)

Table 120E–6—Applied sinusoidal jitter

Parameter	Case A	Case B	Case C	Case D	Case E	Units
Jitter frequency	0.04	1.333	4	12	40	MHz
Jitter amplitude	5	0.15	0.05	0.05	0.05	UI

Reference: IEEE 802.3bs draft D3p5 page 379

  - RJ and BUJ amplitude initially set to Tx Output limits, but RJ and pattern generator amplitude are adjusted to end up with specified eye opening: Eye Width (1E-5): 0.20 UI; Eye Height (1E-5): 30 mV
    - De-Emphasis is applied at test transmitter for best eye opening with selected CTLE
  - Reference receiver used for stress calibration (more on stress calibration later)
- Crosstalk applied in counter propagating direction
  - Aggressors: PRBS31Q, at same symbol rate, but asynchronous to test data generator clock

IEEE 802.3bs / cd C2M AUI Input Test

Host Input Test (continued)

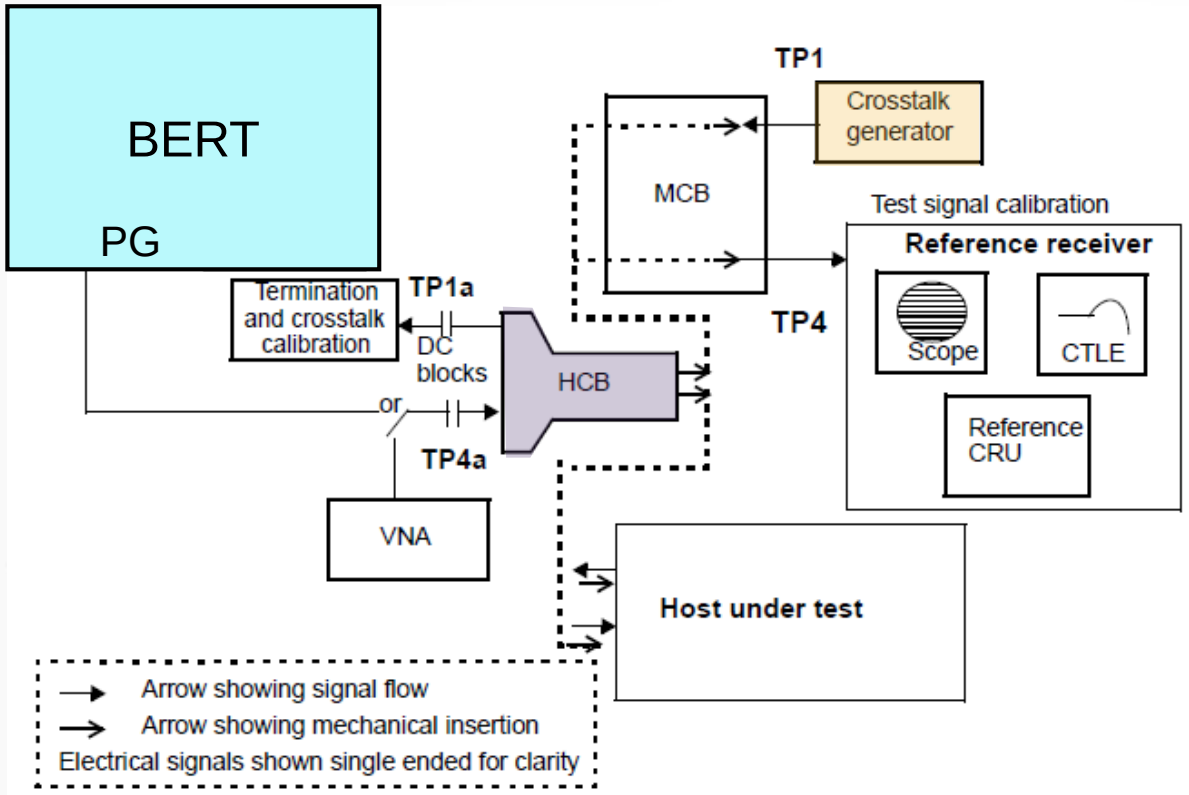


Figure 120E–11—Example host stressed input test

Reference: IEEE 802.3bs draft D3p5 page 378

- Actual crosstalk generator only used in calibration
  - Compensating for crosstalk on HCB
  - Crosstalk generated by host during test
    - Inherently asynchronous to data
- BERT can serve as pattern generator, error counting performed by DUT
- Test pattern: PRBS31Q or scrambled idle
- Test to pre-FEC BER < 1E-5

IEEE 802.3bs / cd C2M AUI Input Test

Module Input Test

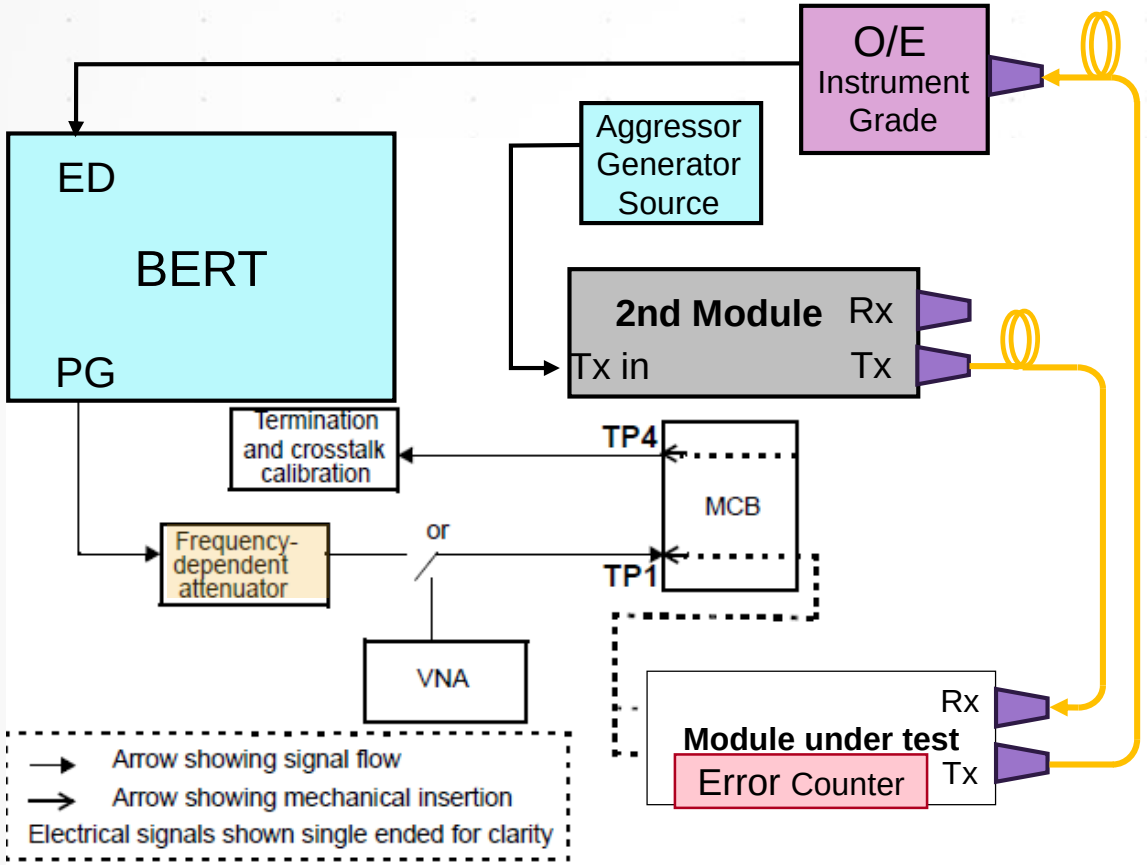


Figure 120E–12—Example module stressed input test

Reference: IEEE 802.3bs draft D3p5 page 381

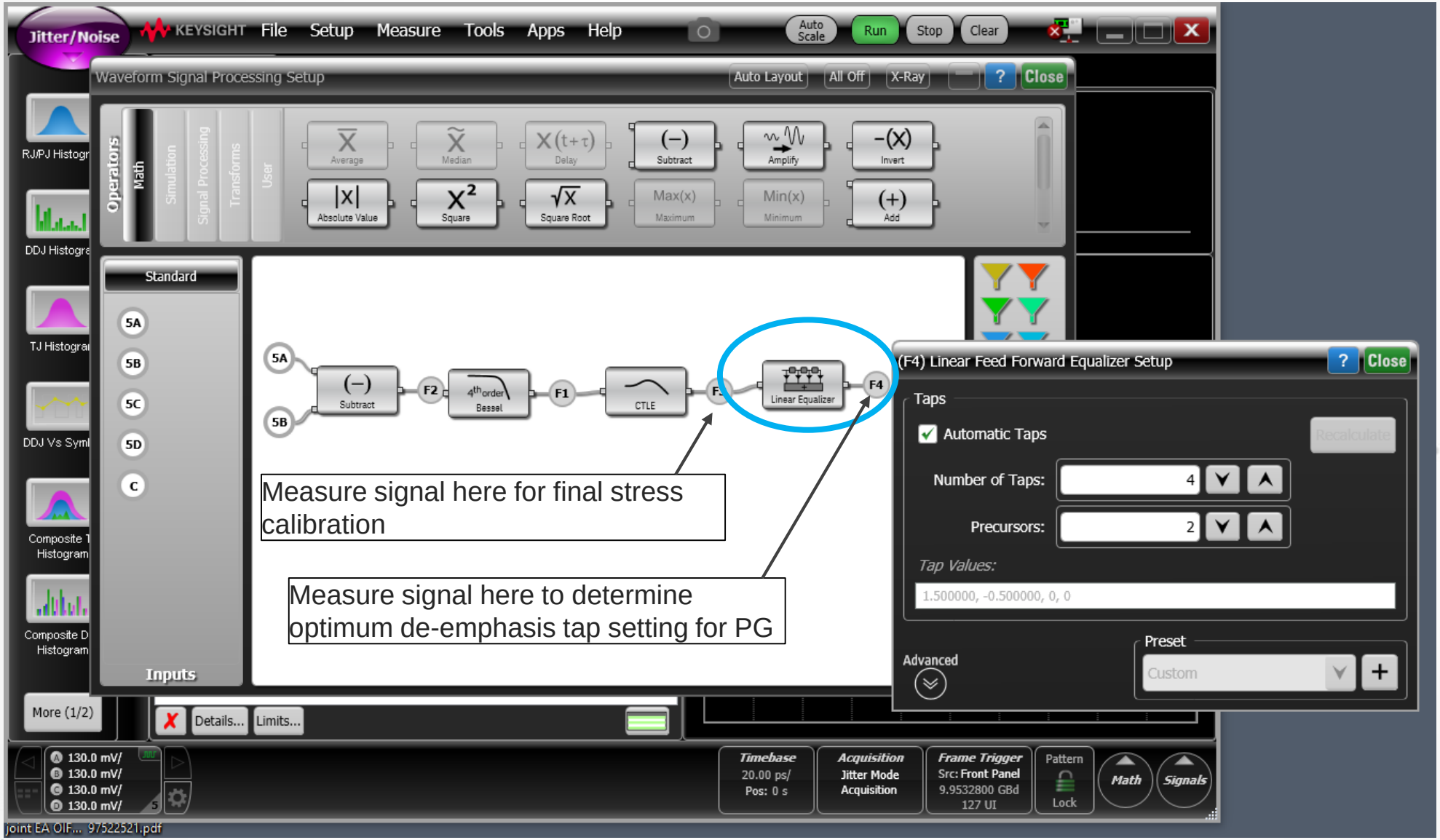
- Added frequency dependent attenuator (ISI)
  - Two sets of 5 tests perform – short and long channel
- Similar stress 'recipe' as in host input test
  - Same 5 SJ frequencies and amplitudes
- Calibration targets: EW-5: 0.22 UI, EH-5: 32 mv
- Crosstalk generator used in calibration
  - Optical aggressor signal applied to DUT Rx input during test
    - Second DUT can be used as optical source
    - Aggressor must be asynchronously clocked
- Use BERT for PG and DUT error counter, (if available) or BERT ED with suitable instrument grade O/E (loopback error potential applies!)
  - Using second DUT as O/E may confound results – overstating actual BER
- Test to BER < 1E-5

IEEE 802.3bs / cd C2M AUI Input Test – Stress calibration

Module Input Test has added channel loss

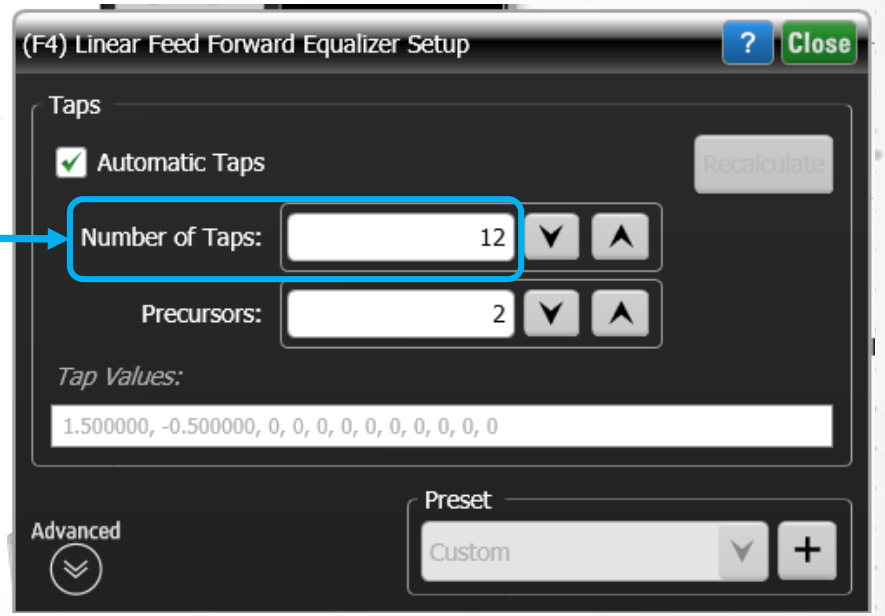
- Achieving module input stress calibration is challenging in high loss case
- Little or no added RJ will be required to “tune” eye width
- Tuning allowed:
  - Reference receiver CTLE gain selections – select from table
    - Document suggest using CTLE Gain that gives the best EW-5 * EH-5 product, but:
    - Optimum EW is often not same setting as EH
    - We have found optimum setting to achieve EW is often one step away (0.5 dB) from best EW*EH product
  - Transmitter FFE (pattern generator de-emphasis)
  - Easy way to find optimum Tx DE tap settings – use FFE in Reference Receiver, and ask to auto-optimize, then transfer tap values to pattern generator de-emphasis
    - (shown on next slide)
  - EH usually not the problem, adjusted by PG Amplitude.
    - However, Vp-p cannot exceed Tx max (900 mV) in non-deemphasized portion of the pattern

Using reference receiver to determine PG De-Emphasis



IEEE 802.3bs / cd C2M AUI Input Test – Stress calibration

- "My Eye Width is still too narrow" (< 0.22 UI) with no added RJ or BUJ
  - Testing this way is over stressing the DUT – more likely to fail compliance test
- Test setup (compliance boards, Frequency Dependent Attenuator, and cabling) which fail channel return loss requirements will likely not achieve 0.22 UI Eye width
  - Simple check, without getting out the VNA:
    when using reference receiver FFE – set a high tap count (12 or more).
    If adding extra taps opens eye, the FFE is performing reflection cancelation – test channel in setup has too much return loss



- Eye Height is usually not a problem (PG has plenty of amplitude), but non de-emphasized portion of pattern cannot exceed max Tx output (900 mV differential)

Typical calibration results

- Make EW and EH measurements in Jitter Mode for best accuracy
- Results before adding RJ to “tune” EW
- Long channel, CTLE setting: 6.5 dB, PG De-Emphasis: -0.16 (pre), 0.02 (post)

Src: F2 Rate: 26.562514 GBd Pat. Length: 8191

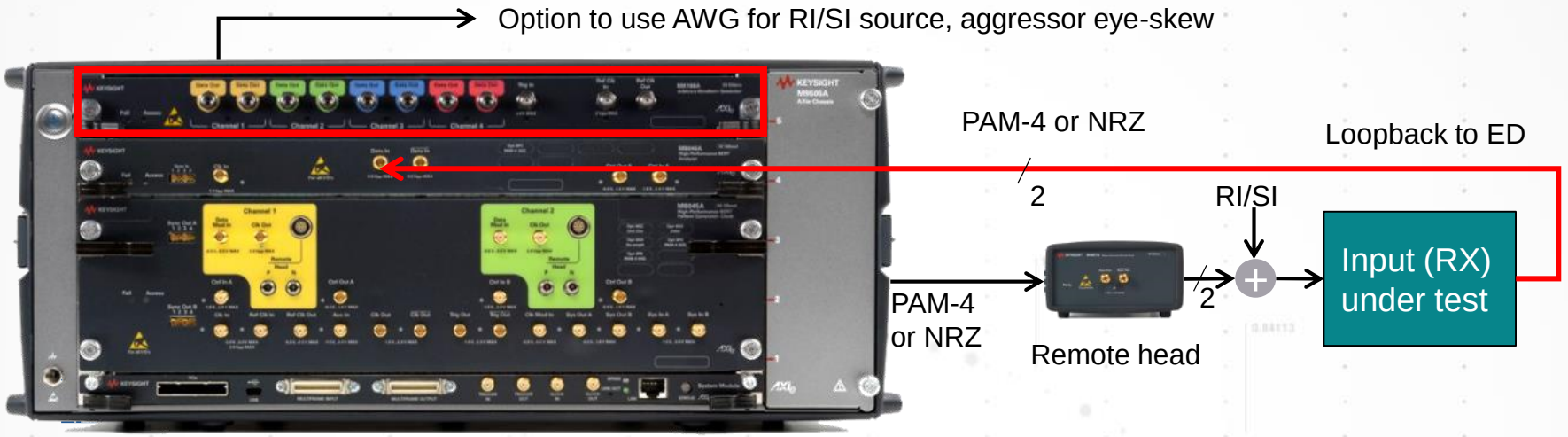
Measurement	Eye 0/1	Eye 1/2	Eye 2/3
Eye Width (1.0E-5)	232 mUI	308 mUI	249 mUI
Eye Height (1.0E-5)	34.10 mV	34.75 mV	37.95 mV
Eye Skew	5 mUI	-6 mUI	9 mUI
TJ (1.0E-5)	770 mUI	690 mUI	750 mUI
DJ (δ - δ)	580 mUI	510 mUI	570 mUI
RJ (rms)	23 mUI	23 mUI	23 mUI
BUJ (δ - δ)	35 mUI	30 mUI	35 mUI
DDJ (p-p)	630 mUI	565 mUI	610 mUI

Details Limits

Automated Compliance Input Test solutions

- Experience has shown most common cause of input testing non-repeatability is stress calibration errors
- Automated closed loop stress calibration eliminates this source of non-repeatability
  - DCA sampling scope used to measure stress during calibration
- Keysight recently introduced new Input test automation solutions for 400G applications:
  - M8091BSPA IEEE 802.3 BS RX Test SW (802.3 Annex 120E – chip to module electrical)
  - M809228XA OIF-CEI 28G RX Test SW (CEI_4.0 Clause 16 – chip to module electrical)
  - N4917BSCA 400G Optical Receiver Test Application (802.3 clauses 121, 122, & 124 optical)
- SW automates – setup de-embedding, stress calibration, cross talk calibration, DUT verification, test execution, results reporting

PAM-4 Input Testing Using M8040A BERT with M8196A AWG



M8040A 64 GBaud BERT :

- True native PAM4 or NRZ (no combiners)
- Built-in 4 tap de-emphasis
- Emulate jitter, calibrated and built-in
- Emulate aggressor w/ fast tr on 2nd channel
- Level non-linearity test

- True PAM4 / NRZ Error Detector or interface with DUT built in error counters

M8196A complements input test setup when used as:

- Random/ sinusoidal interference source with directional couplers
- Aggressor channel
- PAM-4 generator to emulate horizontally skewed eyes

Summary

- Standards are still moving – be sure you are using the most recent draft version
- TX Test – many new PAM4 measurements
  - Optical: Use a low noise reference RX with proven TDECQ algorithms
  - Electrical: Use a low noise solution with robust clock recovery capabilities (SW and/or HW)
- Use DUT internal error checkers rather than BERT Error Detector for links that do not run error free
- 400G standards have very little margin – clean test set up required to achieve stress calibration
- Verify your compliance test boards, especially return loss

Questions?