Addressing Crosstalk Challenges from Design Simulation to Actual Board Analysis and Debug

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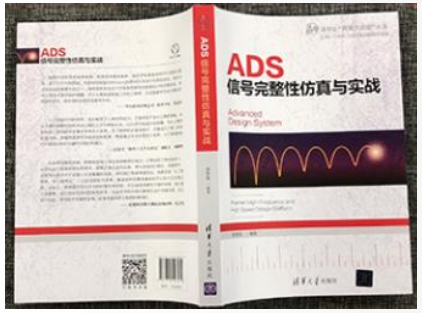
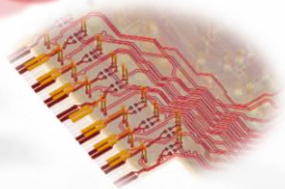
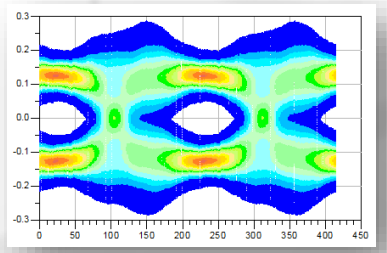


KEYSIGHT TECHNOLOGIES





Objective and Agenda

- *Objective*
  - *Show a complete closed-loop approach from simulations to measurements for design problems related to crosstalk*
- *Agenda*
  - *What is the closed-loop approach*
  - *Crosstalk simulation and correlation with measurement*
  - *Crosstalk measurement and debug/analysis*
  - *Summary*

Agenda

- *What is the closed-loop approach*
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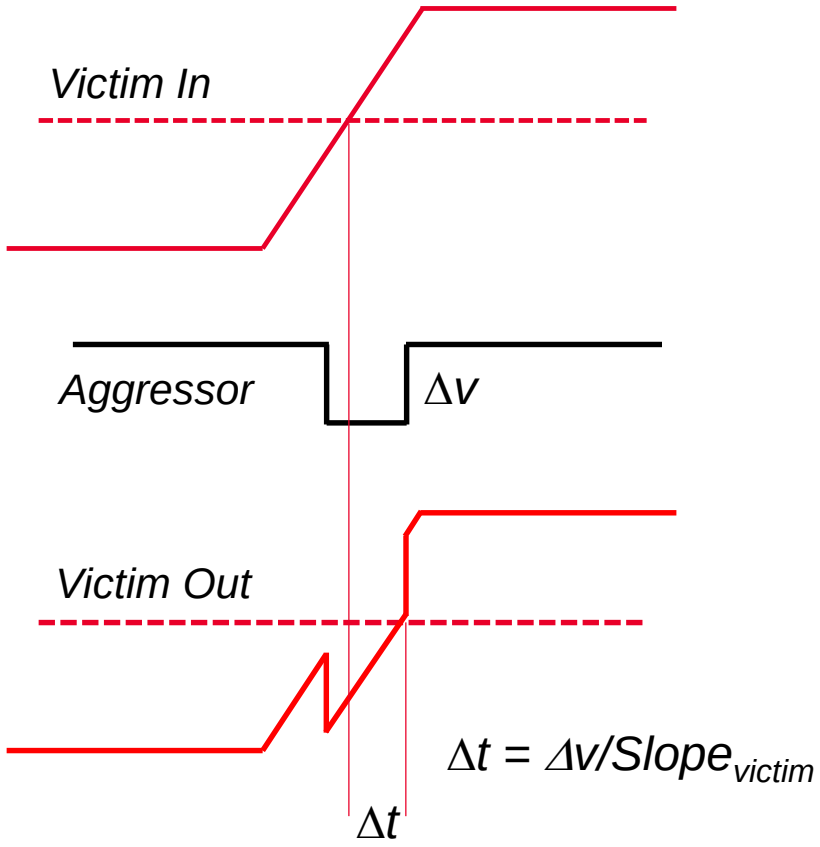
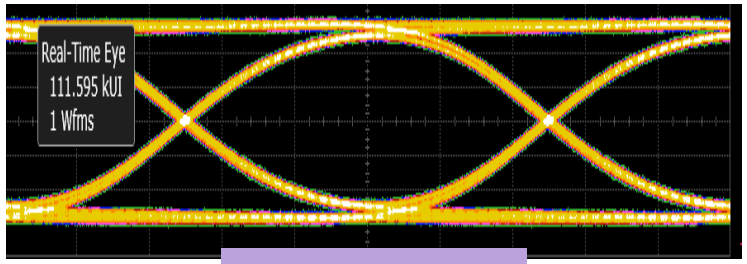
Before We Start…

CROSSTALK REFRESHER

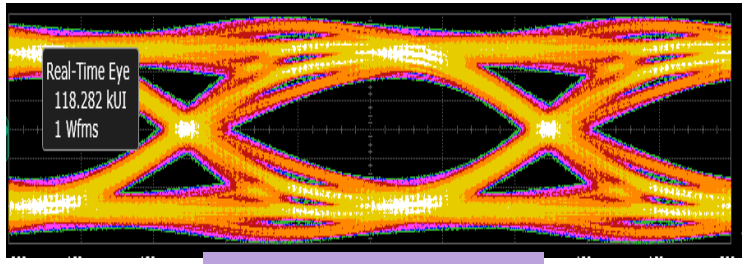
- Crosstalk is amplitude interference with aggressor's data pattern



Impact on Eye



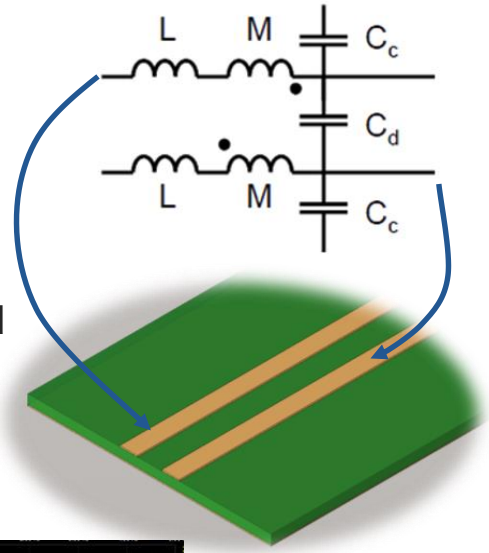
No crosstalk



With crosstalk

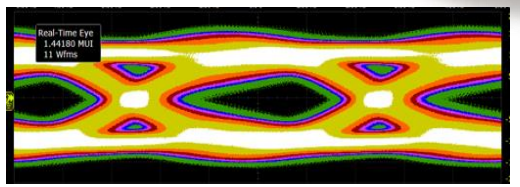
Types of Crosstalk

CROSSTALK REFRESHER

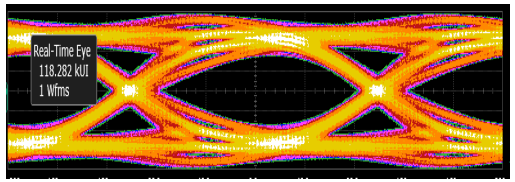


- Crosstalk is becoming a more important issue, as data rates increase, and more lanes are packed into a small space.
- Mainly caused by capacitive or inductive coupling between multiple transmission lines and/or power delivery networks.

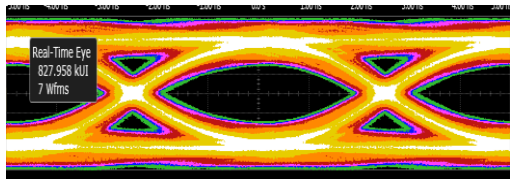
- Prominent Sources:
  - Next End Crosstalk (NEXT)
  - Far End Crosstalk (FEXT)
  - Power Supply Induced Jitter
    - Noise coupling through PLL
  - Voltage Dependent Amplitude Noise
    - Affecting data level 0 and 1
  - Simultaneous Switching Noise
    - Data line aggressing power supply



NEXT



FEXT

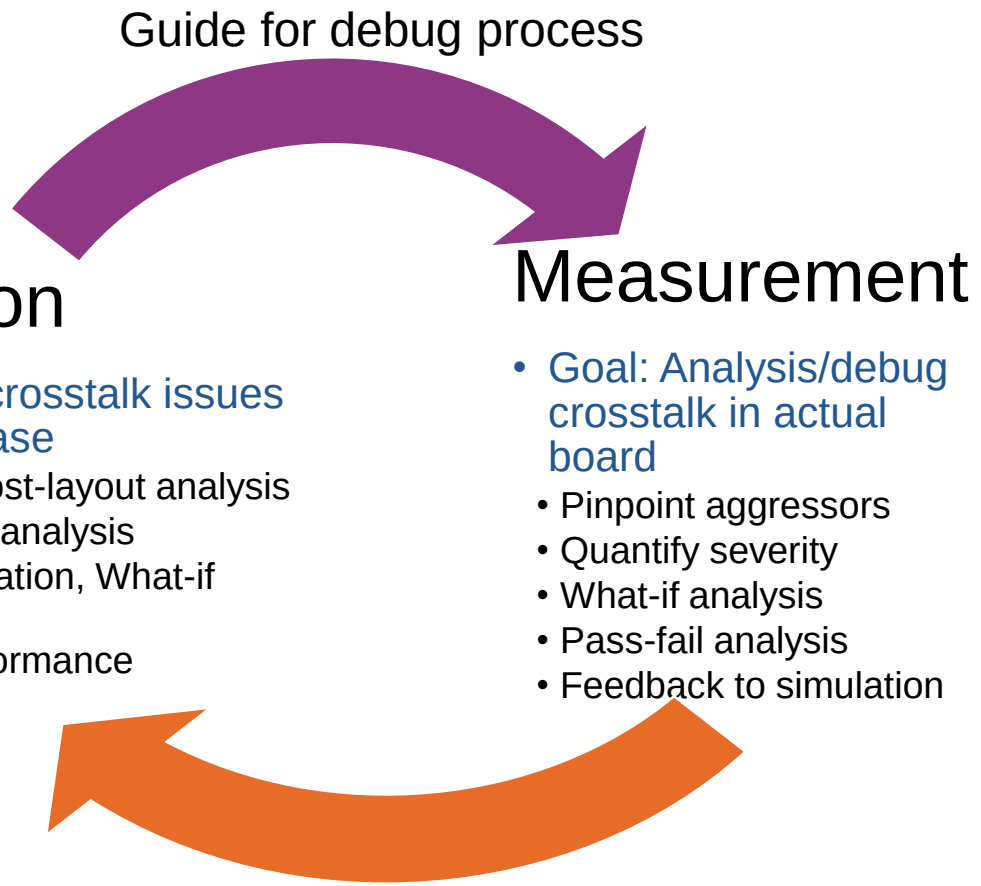


PLL

Many ways crosstalk can close the eye.

Crosstalk Consideration in Your Design Cycle

THE CLOSED-LOOP APPROACH – REDUCE BOARD SPINS!



Crosstalk Simulation vs. Measurement

Criteria	Simulation	Measurement
Development Phase	Pre-production	Post-production
Tasks/Contributions	Avoid crosstalk issues at the design phase • *Predict potential crosstalk* • *Design exploration* • *What-if analysis* • *Performance optimization*	Analyze crosstalk issues after a product is manufactured • *Pinpoint sources of aggressors (root cause)* • *Quantify severity* • *What-if analysis* • *Feedback to simulation*
Engineering Cost	Lower • *Before product is manufactured* • *Simulation effort* • *Significant time to optimize simulation*	Higher • *After product is manufactured* • *Significant time and effort to pinpoint root cause.* • *Re-spin of product can be expensive*
Requirements	*Software* • *Simulation software* • *Board layout data* • *Device models (SMD, IBIS, etc.)*	*Hardware and software* • *Instruments (e.g. oscilloscope, network analyzers, probes)* • *Analysis software*

Agenda

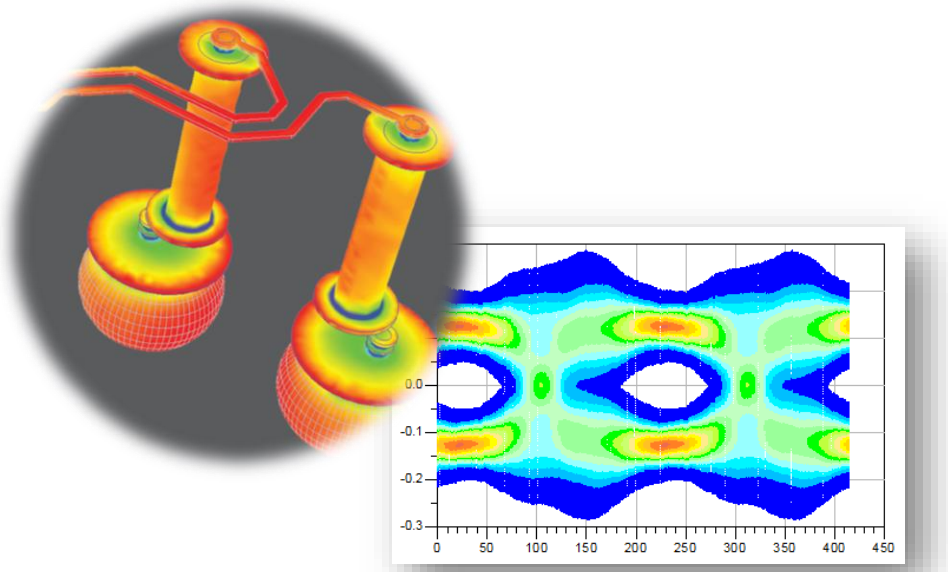
- *What is the closed loop approach*
- *Crosstalk simulation and correlation with measurement*
- *Crosstalk measurement and debug/analysis*
- *Summary*

Crosstalk Simulation

SIMULATION TECHNOLOGIES AND MODELS FOR CROSSTALK

– Simulation accuracy greatly depends on simulation models' accuracy

- **Simulation Technologies**
  - S-parameter simulation
  - Transient Convolution
  - Channel Simulation
  - Memory Designer Simulation (DDR Bus)



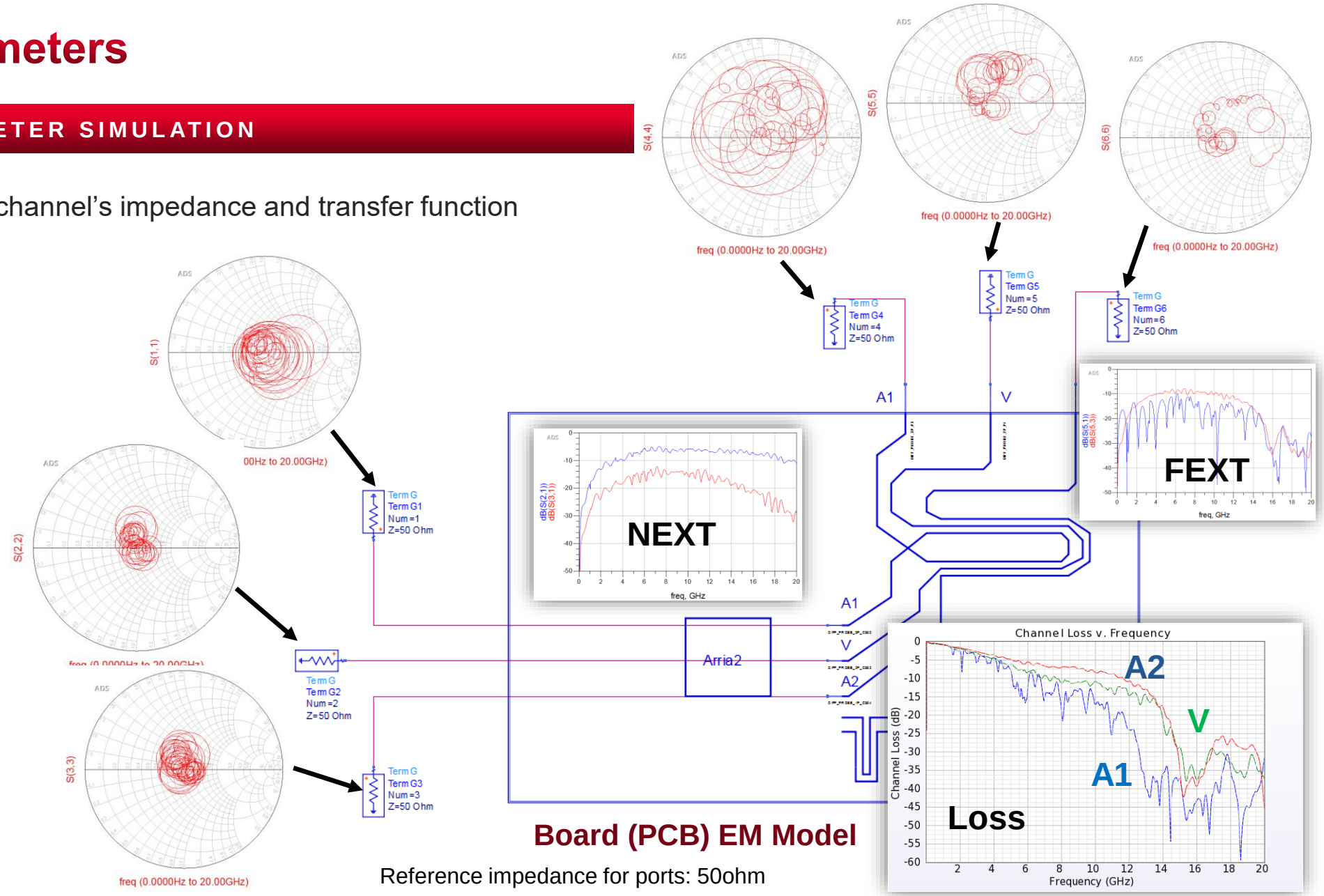
– **Simulation Models**

- Channels and PDN
  - Multilayer Library
    - Pre-layout circuit models
  - EM (Electro-Magnetic) models
    - Post-layout EM models
    - Accounts for complete electro-magnetic behaviors
    - ADS (Momentum and FEM)
    - EMPro (FEM and FDTD)
    - SIPro/PIPro EM models
- TX/RX Drivers
  - IBIS model

S-Parameters

S-PARAMETER SIMULATION

- Analyze channel's impedance and transfer function

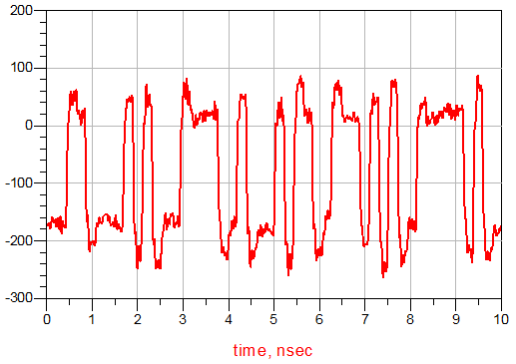


Reference impedance for ports: 50ohm

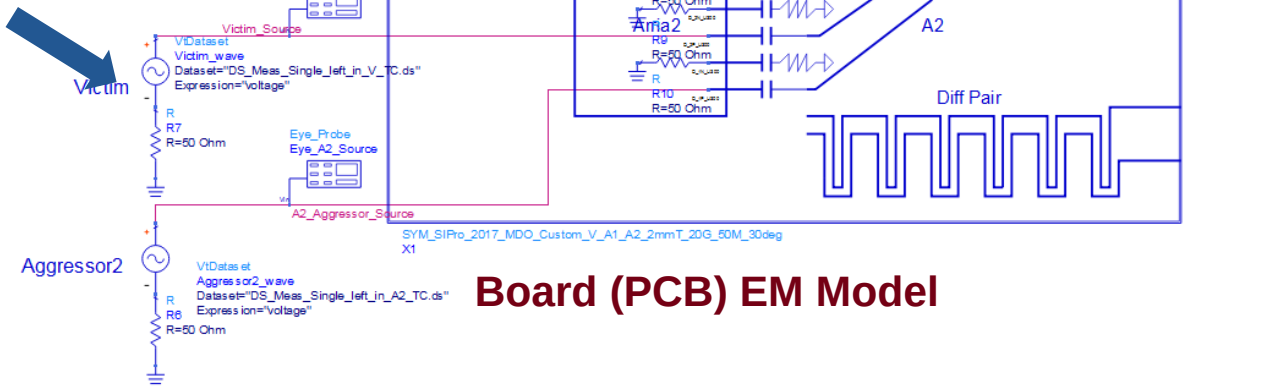
Eye Diagram – With Measured Data

TRANSIENT CONVOLUTION SIMULATION

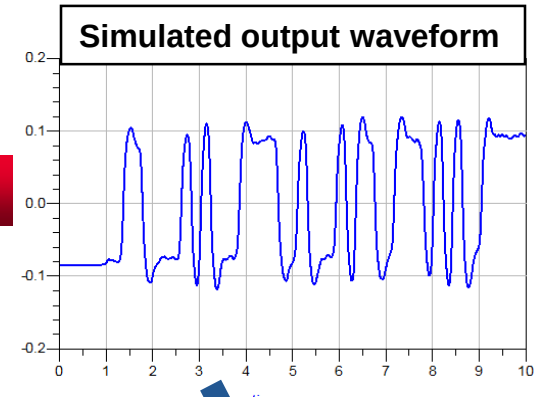
- Transient convolution simulation is required with measured data source
  - Complete time domain analysis with s-parameter channel data
- Channel loss removes the high frequency component from the output waveform

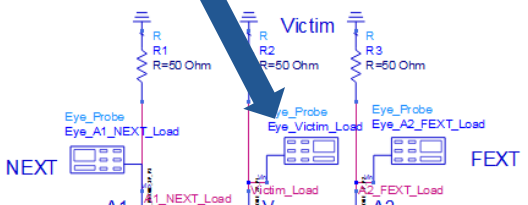


Measured input waveform



Board (PCB) EM Model

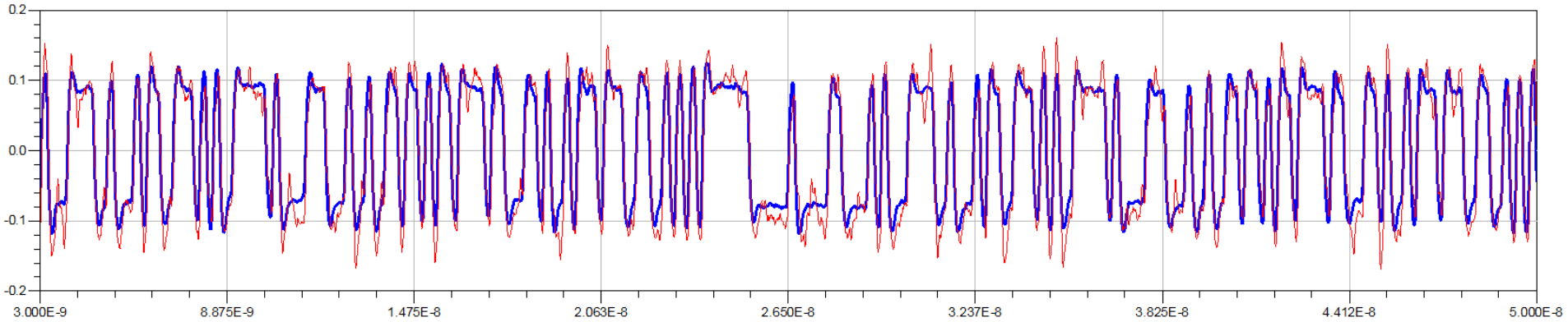




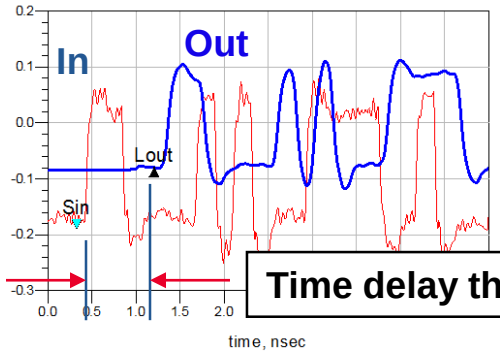
Waveform Analysis

TRANSIENT CONVOLUTION SIMULATION

- Measured (Red) vs. simulated (Blue) @ Load



- The mismat



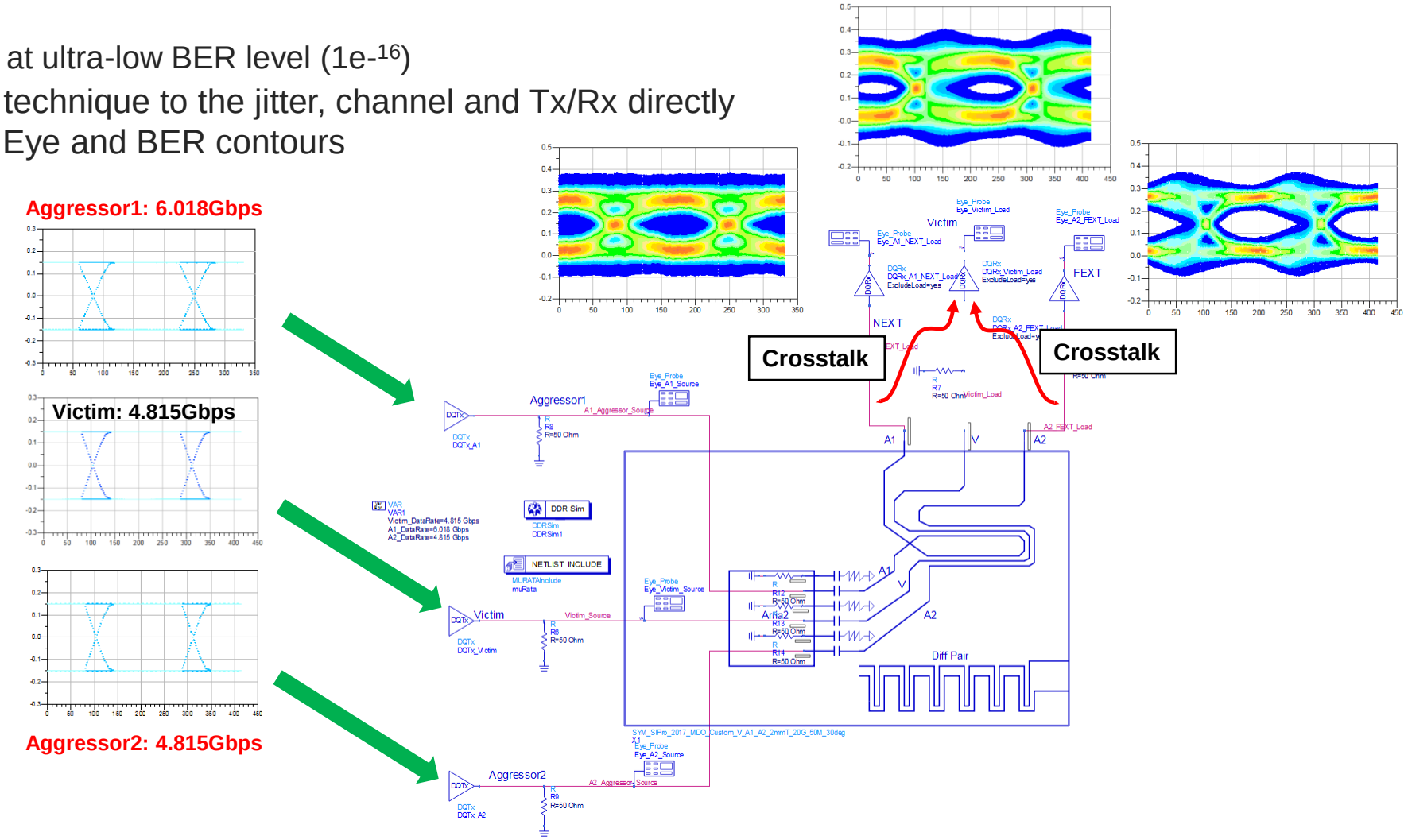
Note: Individual measurements were performed at the source and load. Therefore a manual time delay was applied to the output measured data to synchronize it with the simulation data.

Time delay through the channel = 852.5ps

Full Board/Channel Analysis

DDR BUS SIMULATION – W/ CLOCK SYNCHRONIZATION

- Statistical analysis at ultra-low BER level (1e-^{16})
  - Apply statistical technique to the jitter, channel and Tx/Rx directly to construct the Eye and BER contours

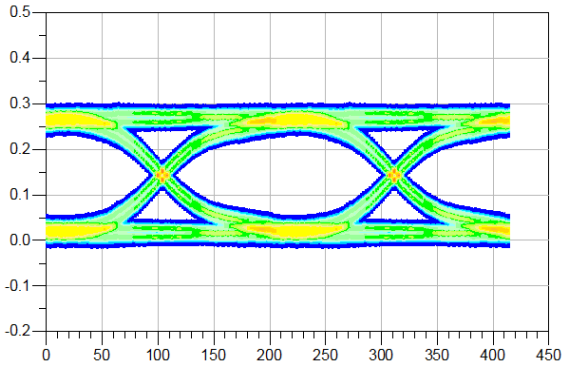


Crosstalk Contribution/Removal Analysis

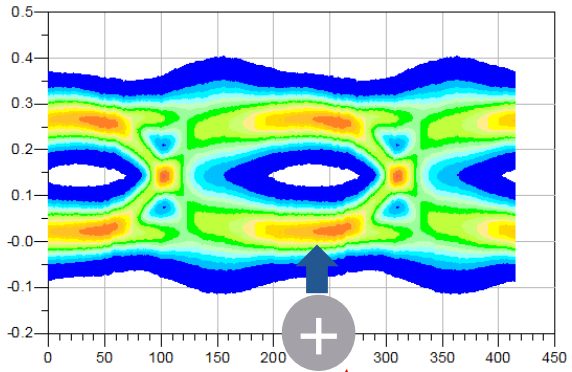
DDR BUS SIMULATION – W/ CLOCK SYNCHRONIZATION

- Crosstalk contribution/removal analysis is a simple process by turning on and off the aggressors in simulations

No Crosstalk:

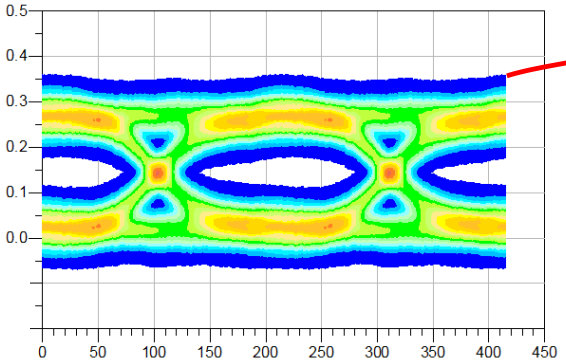


By Both Aggressors:

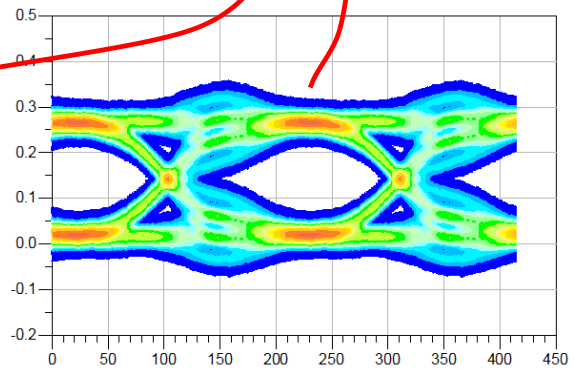


Eye Summary with no crosstalk

measurement	...tim_Load.Summary
Level1	263.6 m
Level0	21.80 m
Height	164.0 m
Width	184.8 p



By Only Aggressor 1:



By Only Aggressor 2:

Eye Summary with crosstalk

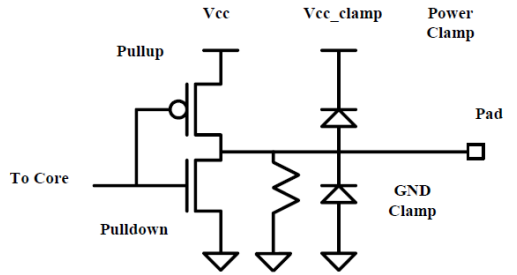
measurement	...tim_Load.Summary
Level1	265.9 m
Level0	21.93 m
Height	61.00 m
Width	112.1 p

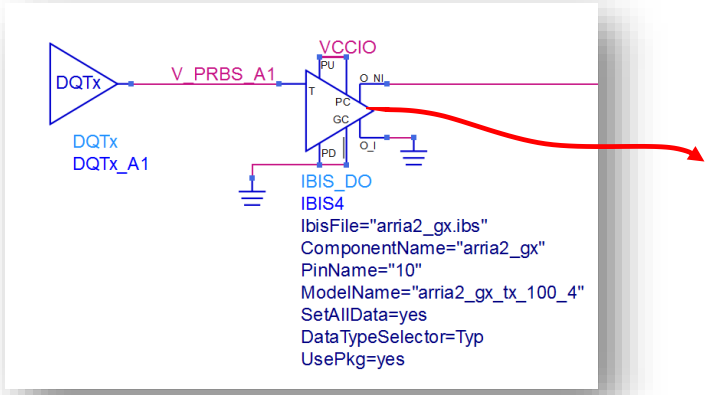
Simulation With IBIS Model

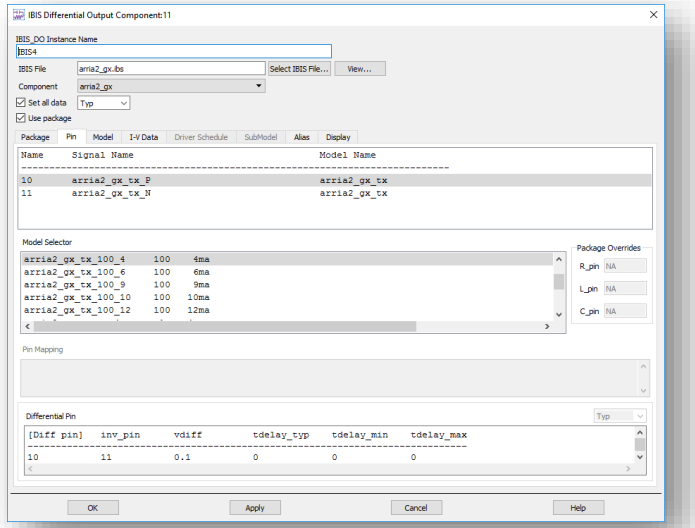
HTTP://IBIS.ORG

- IBIS (Input/Output Buffer Information Specification)
  - Digital IC design of IO buffers can have >10,000s transistors
  - SPICE simulation of only 100 bits takes many hours of simulation
  - IBIS models characterize the measured or simulated SPICE results into a more convenient behavior model
- Improves the simulation accuracy and speed

IO Buffer Representation (IBIS Open Forum)

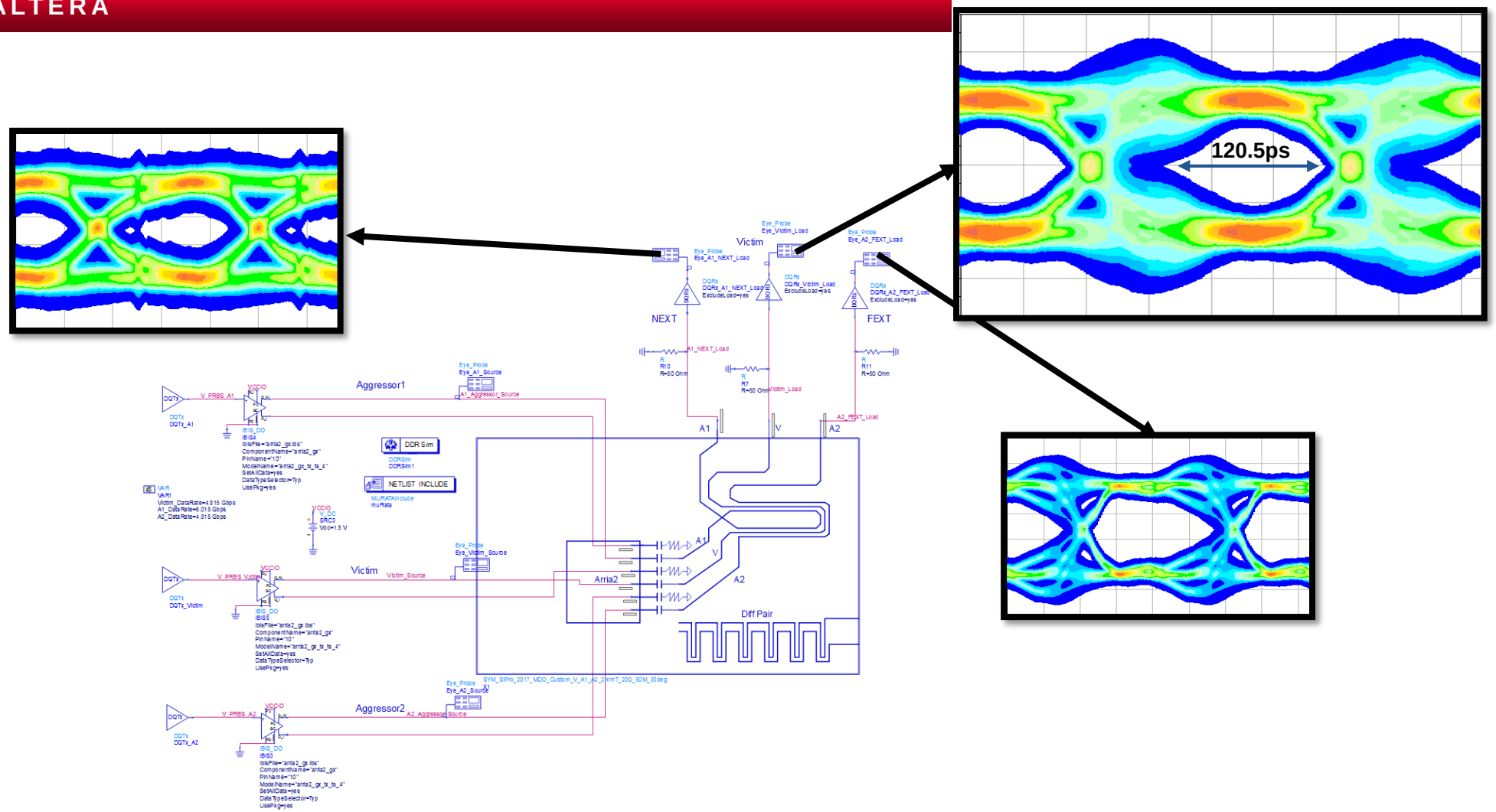






Simulation Results With IBIS Model

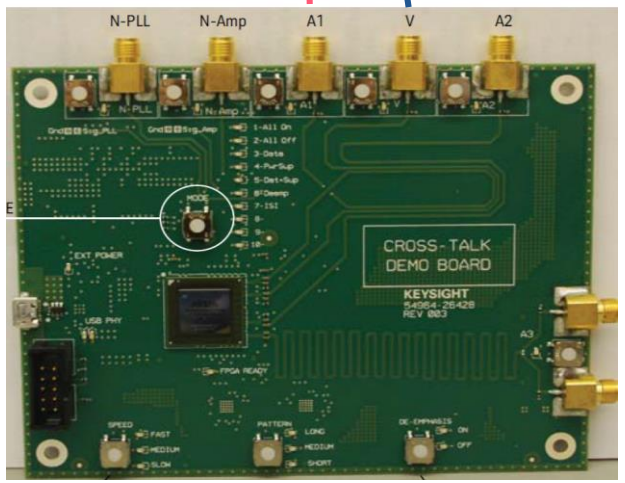
ARRIA-II GX, ALTERA



Measurement Setup With Oscilloscope

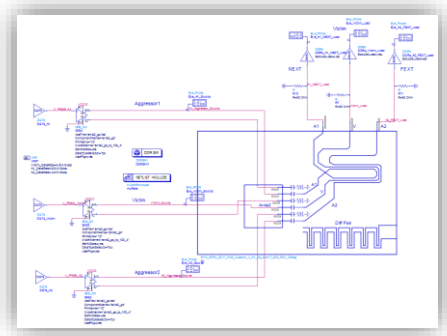
CORRELATING SIMULATION AND MEASUREMENT

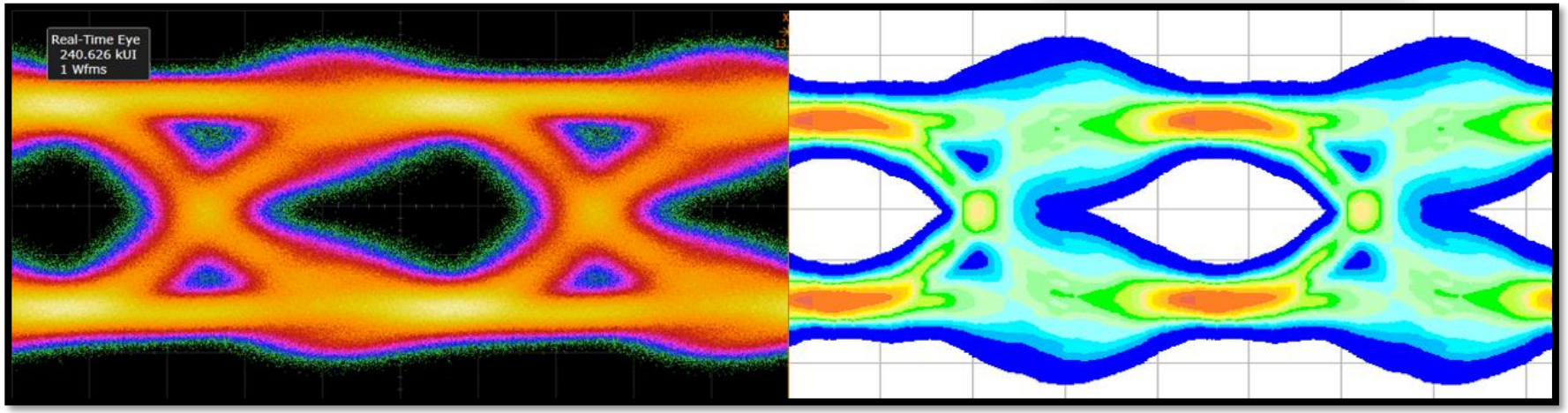
- The victim and aggressors are connected to the scope via SMA cables.
- These aggressors can be turned on and off with the button to the side of each SMA connector.



Side-By-Side Comparison

MEASURED VS. SIMULATED





Measured **Simulated**

Note: IBIS model may not match to the device measured

Agenda

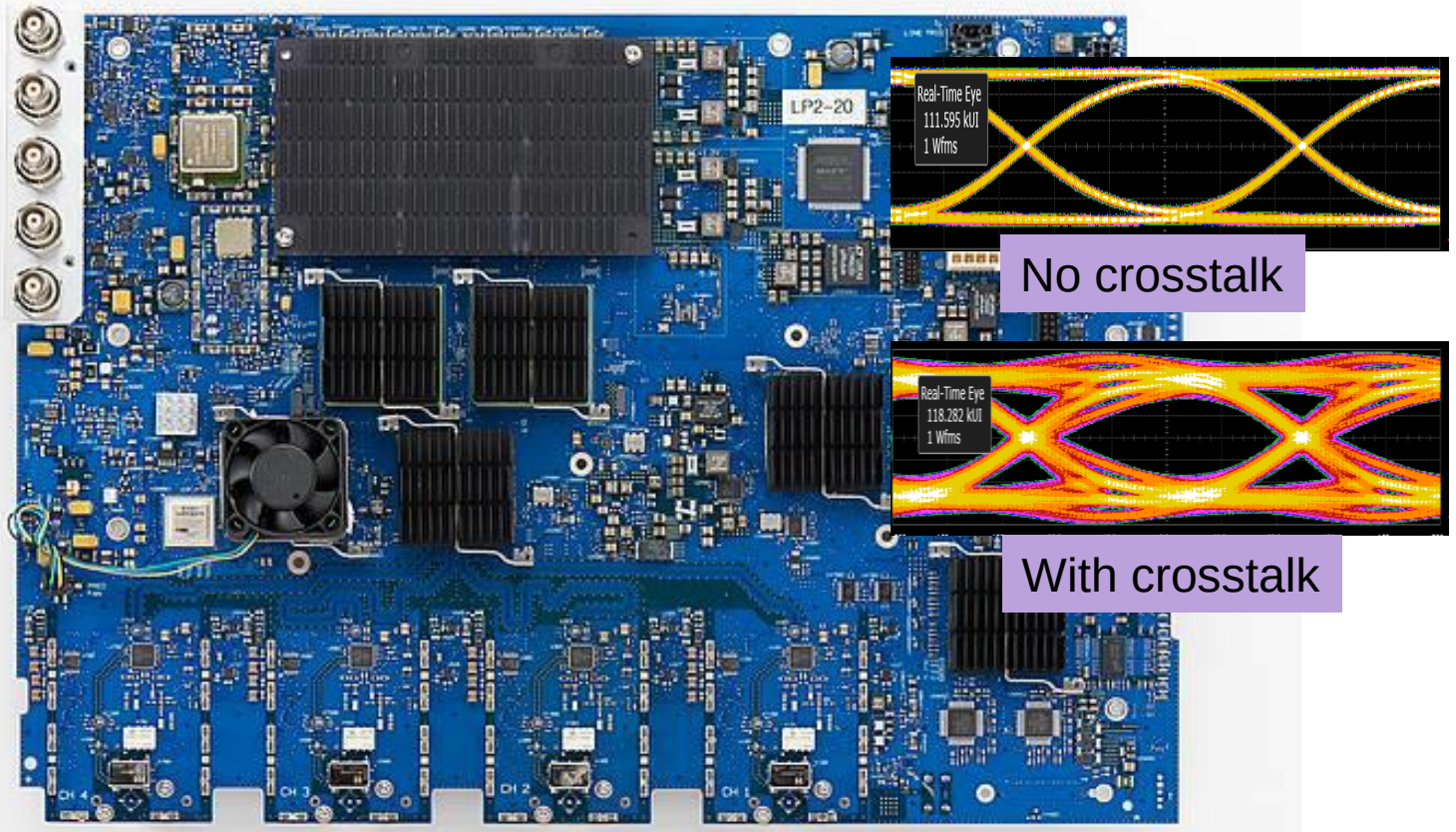
- *What is the closed loop approach*
- *Crosstalk simulation and correlation with measurement*
- *Crosstalk measurement and debug/analysis*
- *Summary*

Crosstalk Analysis and Debug

WHERE DO YOU BEGIN?

Sometimes, simulation can be different from reality. How do you deal with crosstalk issues?

Product failing due to crosstalk issues.

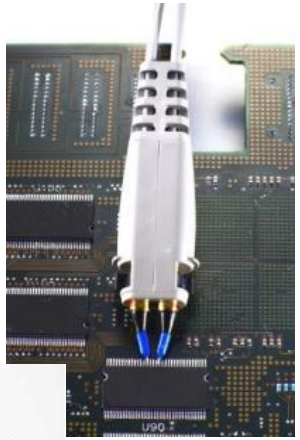


Crosstalk analysis and debug can be effectively accomplished using an oscilloscope. First step is choosing the right probing solution.

Probing High-Speed Signals on the Board

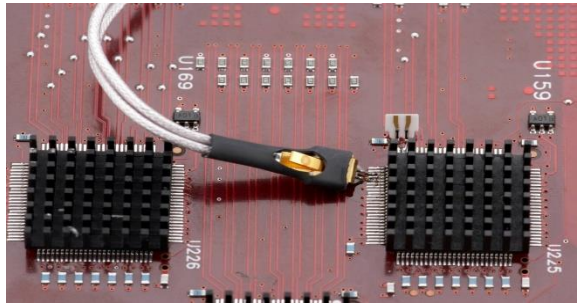
HIGH BANDWIDTH, LOW LOADING ACTIVE PROBES

Browser probe heads to look at different signals quickly and easily



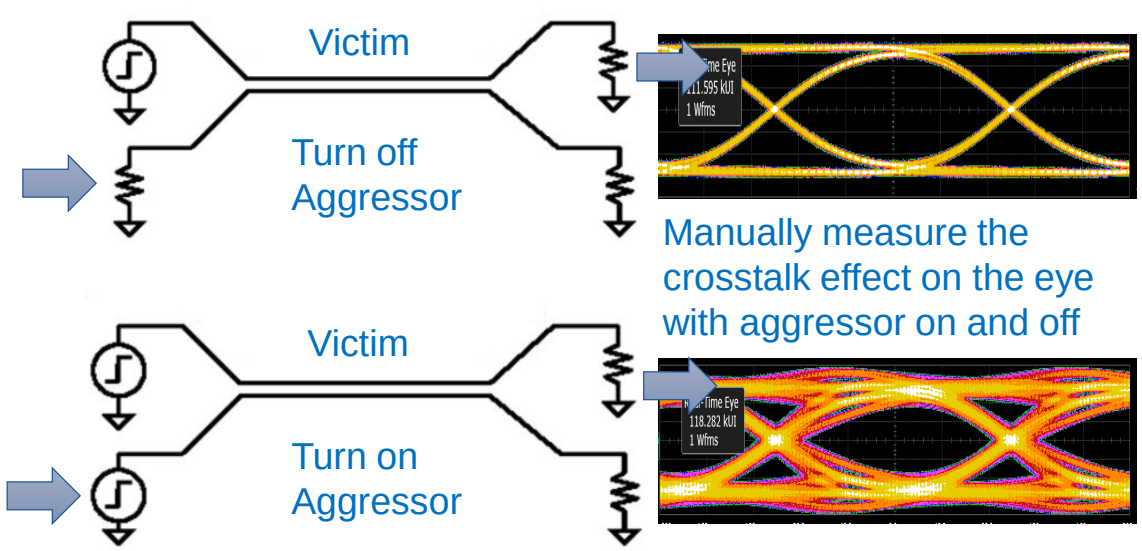
Wide variety of InfiniiMax probing solutions, 1.5 to 33 GHz

Solder-in and Zero Insertion Force (ZIF) probe heads for secure connections when debugging



Challenge1: Legacy Method of Measuring Crosstalk

- The need to troubleshoot and characterize crosstalk is not new, but the legacy methods of measuring crosstalk in digital communications systems has relied on the process of selectively disabling some channels while enabling others.



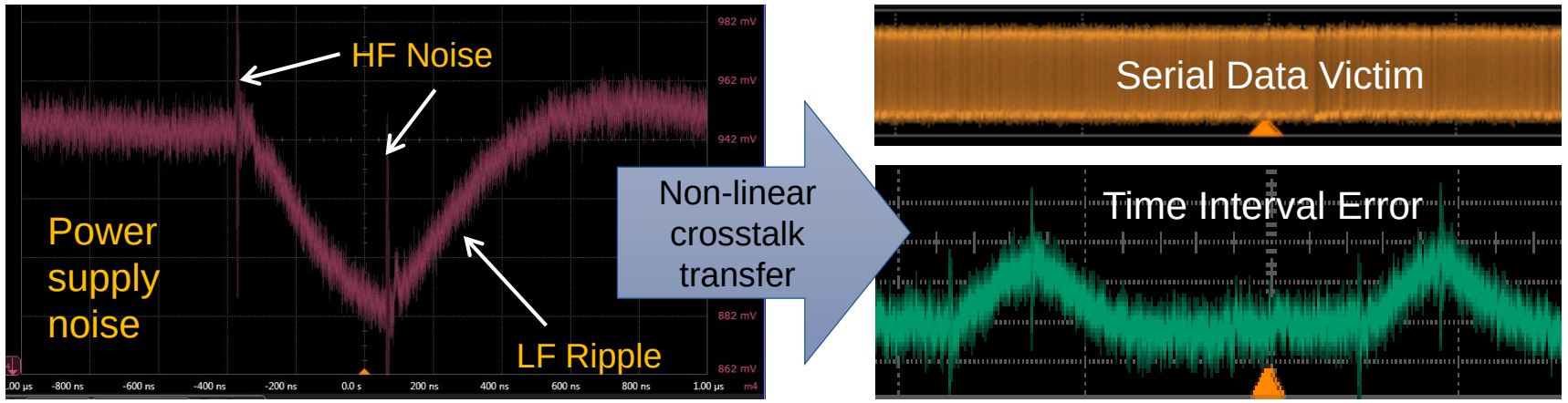
Manually measure the crosstalk effect on the eye with aggressor on and off

Challenges:

- No special test modes to turn on and off aggressors
- Huge effort and time to characterize crosstalk from multiple serial aggressors.
- Power supply cannot be turned off.

Challenge2: Power Supply, Non-Linear Crosstalk

- For serial data lines, VNA can be used to characterized the crosstalk because they are linear network model.
- However, the influence of power supply noise to serial data jitter and amplitude distortion is non-linear and no easy way to characterize the crosstalk transfer.



Power supply noise creates a non-linear transfer on the serial data timing error. The crosstalk transfer is difficult to solve and correlate.

Challenges Solved by Keysight Crosstalk Application

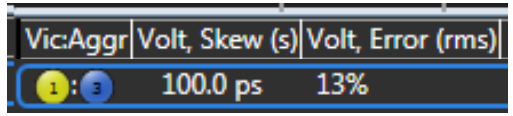
- Legacy method that requires special design test mode and power supply crosstalk can be solved with the Keysight analysis tool.
- N8833A/B Keysight Crosstalk Application Tool provides:
  - Crosstalk Identification
    - Which signals are coupling onto your victim?
  - Crosstalk Quantification
    - How much error does each aggressor add to your victim?
  - Crosstalk Removal for Analysis
    - What would your signal look without crosstalk?
    - How much margin can be recovered on your signal without crosstalk?
    - If the signal was failing spec, can it pass without crosstalk?

Assist in making important design decisions:

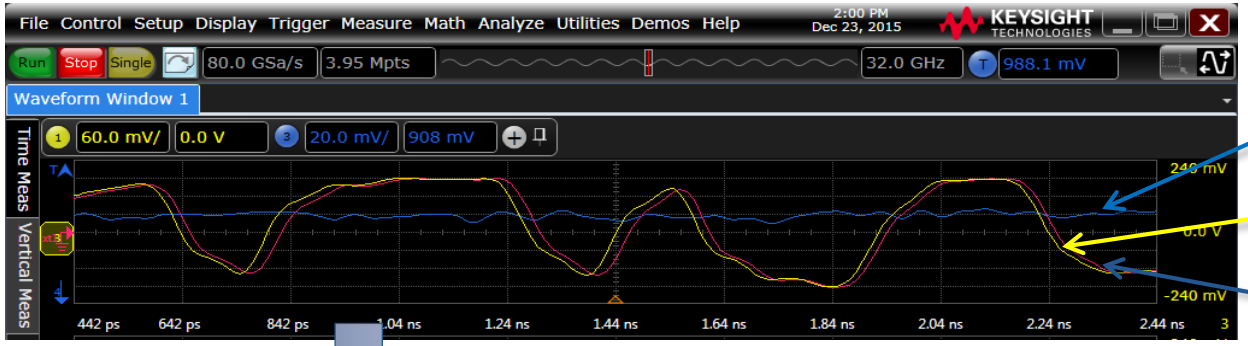
- ***Is it worth reducing crosstalk impact in design?***
- ***Where to improve?***

Results from the Keysight Crosstalk Tool

1. Crosstalk Identification
2. Crosstalk Quantification
3. Crosstalk Removal for Analysis



13% of channel 3 signal energy is coupled into channel 1 signal

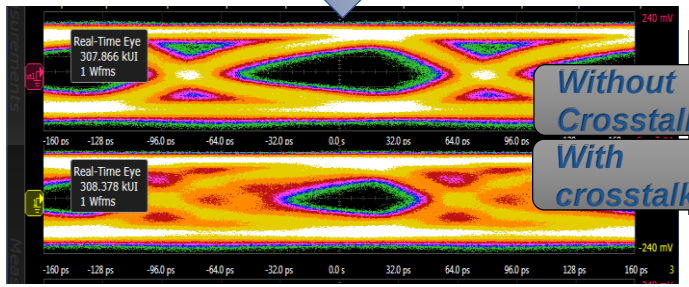


Power supply aggressor

Original serial data victim

Victim without crosstalk

Plot victim eye-diagram



Without Crosstalk

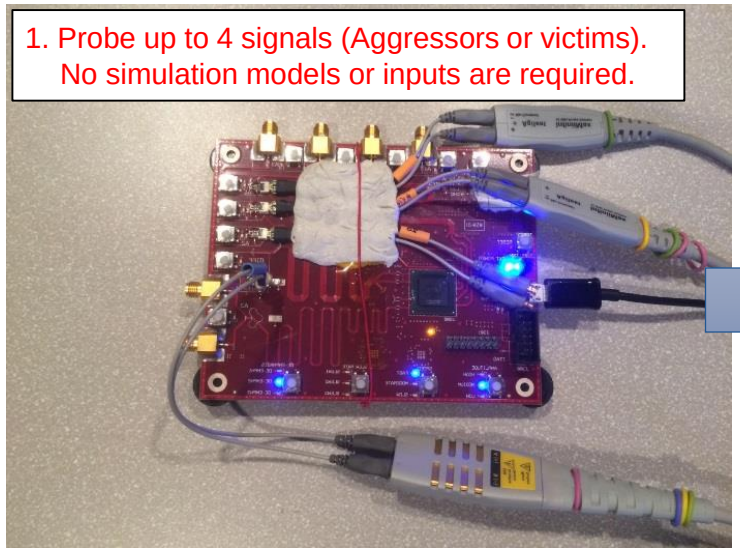
With crosstalk

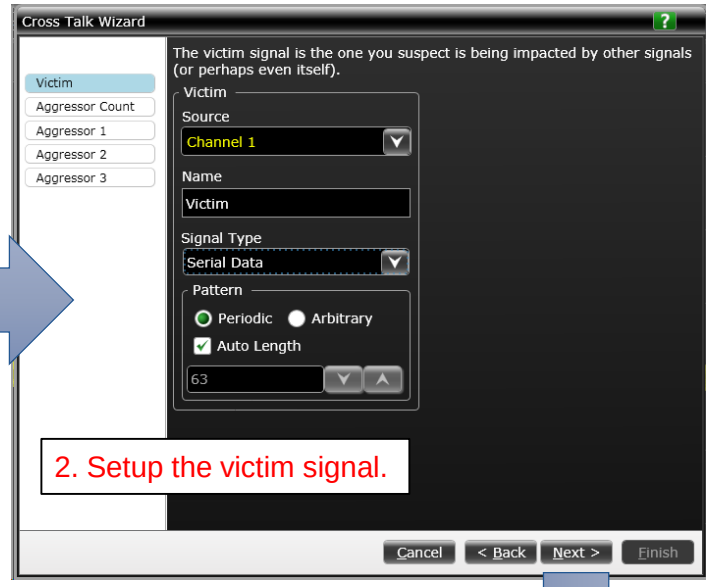
Measurement	Current	Mean
Eye Width(xt1)	113.312 ps	113.312 ps
Eye Height(xt1)	138.3 mV	138.3 mV
Eye Width(1)	68.51 ps	68.51 ps
Eye Height(1)	83.2 mV	83.2 mV

What-If Analysis for making important design decision

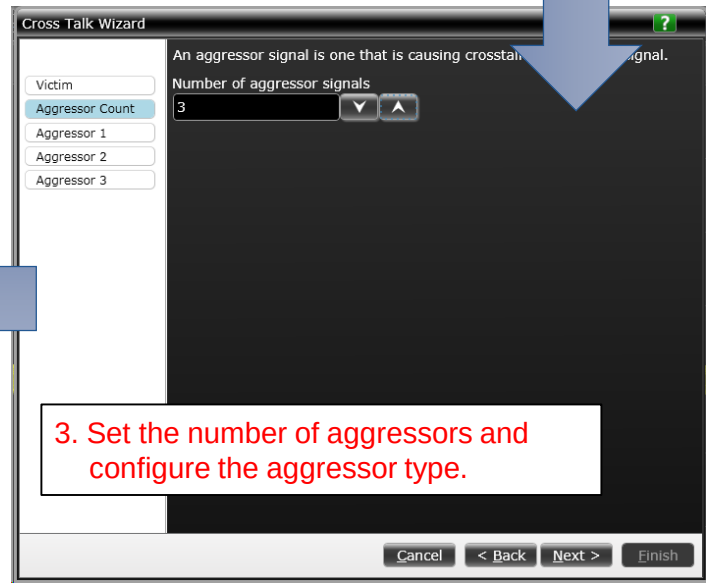
Crosstalk Analysis Setup

1. Probe up to 4 signals (Aggressors or victims). No simulation models or inputs are required.



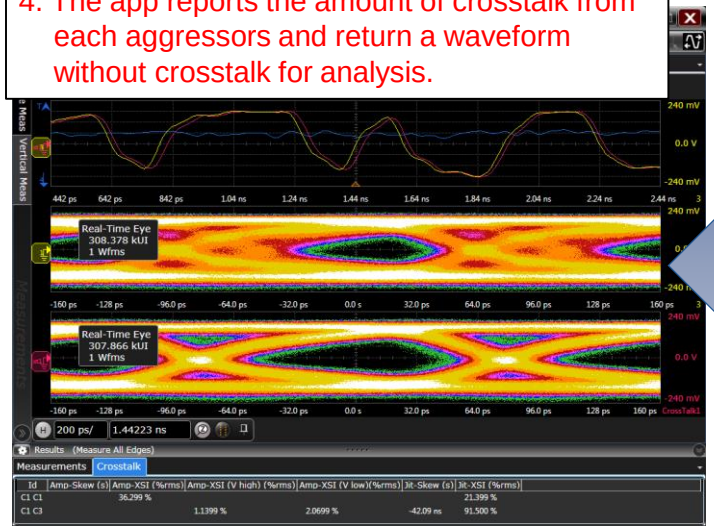


2. Setup the victim signal.



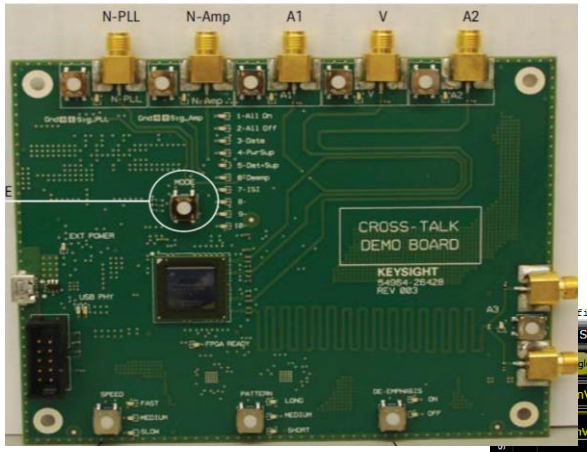
3. Set the number of aggressors and configure the aggressor type.

4. The app reports the amount of crosstalk from each aggressors and return a waveform without crosstalk for analysis.



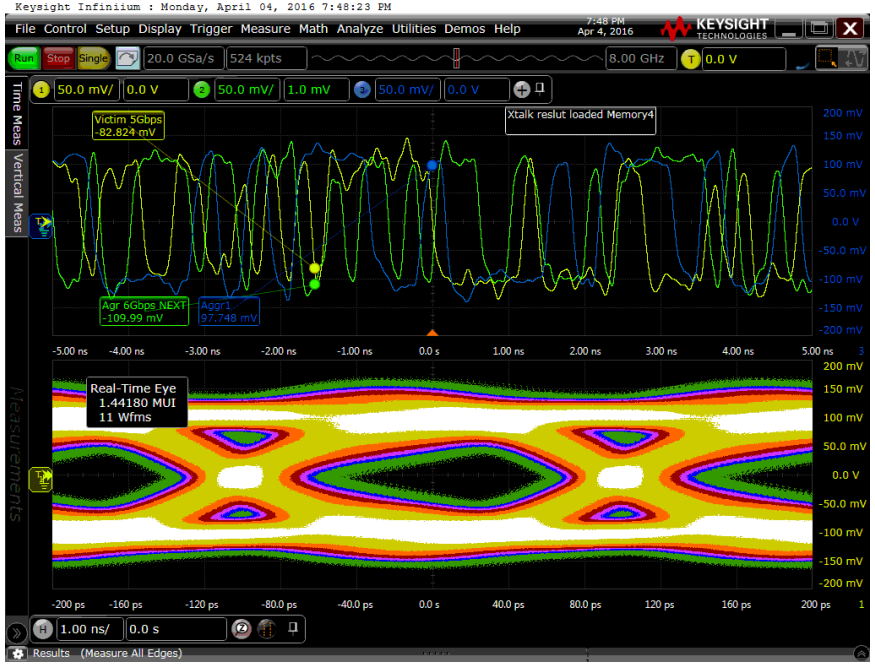
NEXT and FEXT Crosstalk on Victim

WITH KEYSIGHT CROSSTALK DEMO BOARD



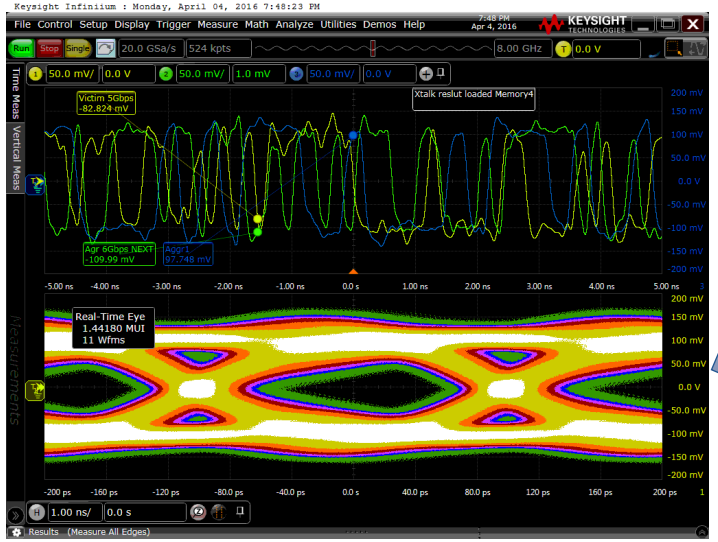
Victim eye-diagram
No aggressors

Victim eye-diagram
NEXT & FEXT aggressors

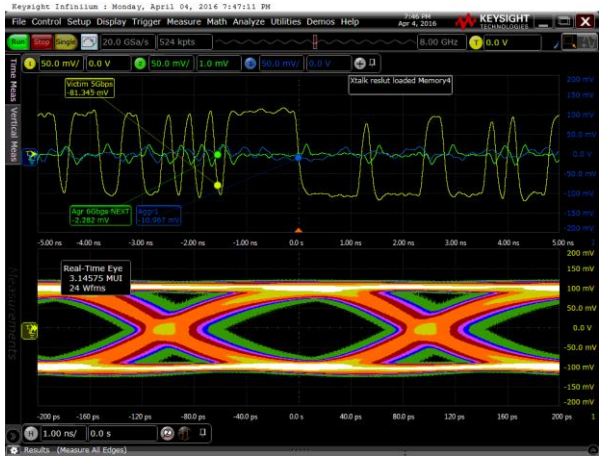


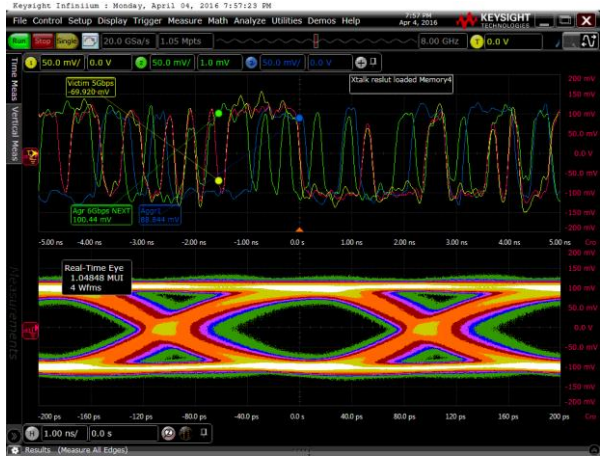
Removing NEXT and FEXT with Crosstalk Tool

With NEXT and FEXT Aggressors



No Aggressors

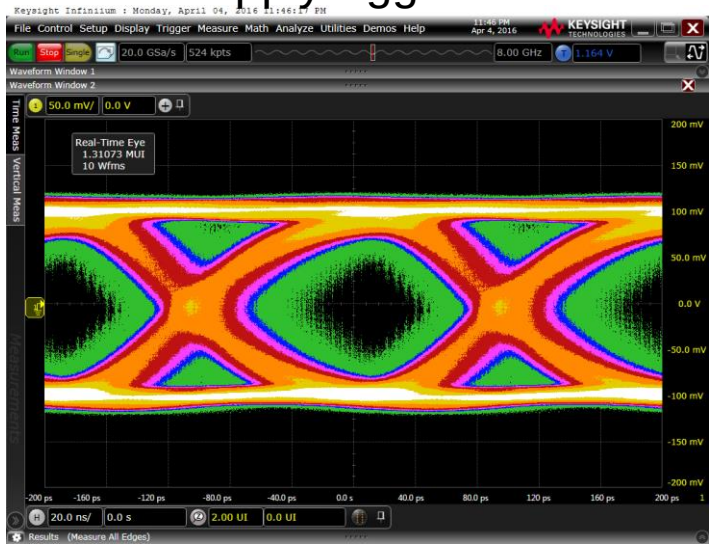




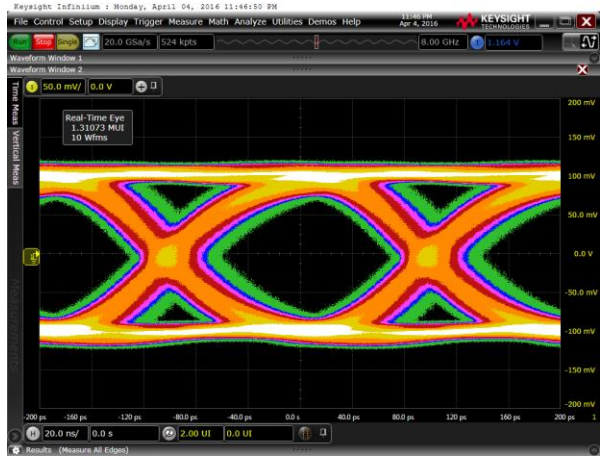
NEXT and FEXT Removed by the Crosstalk Tool

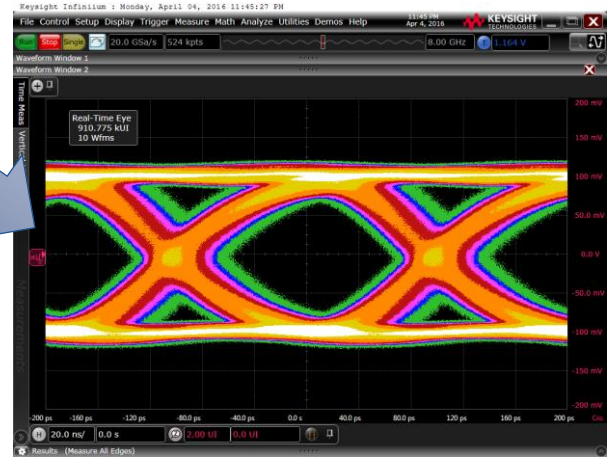
Removing PSIJ from Victim with Crosstalk Tool

Measured Victim with Power Supply Aggressor



No Aggressors





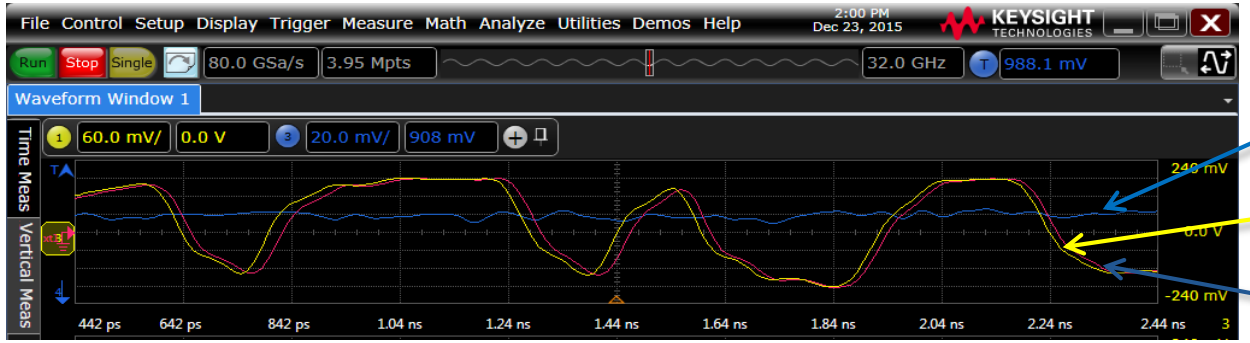
Power Supply Aggressor removed by the Crosstalk Tool

Jitter Improvement Without Power Supply Crosstalk

WAVEFORMS WITH AND WITHOUT CROSSTALK USED FOR JITTER ANALYSIS.

Crosstalk Simulation vs. Measurement

Scope Waveforms used in Simulation Environment

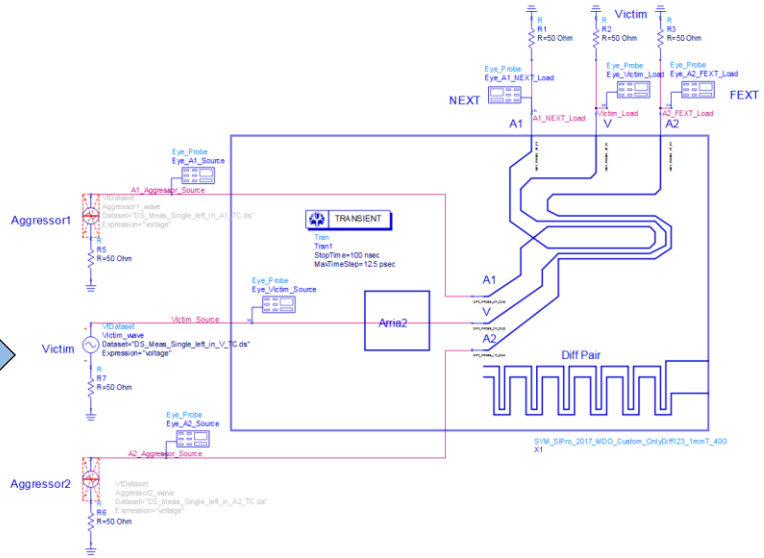


Power supply aggressor

Original serial data victim

Victim with crosstalk removed

Waveforms from the crosstalk tool can be saved and used to optimize the simulation.

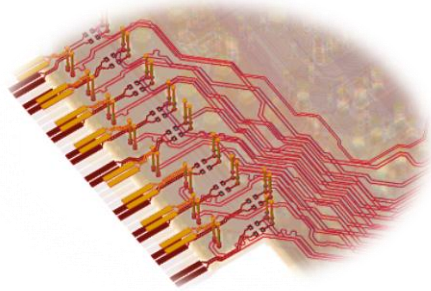


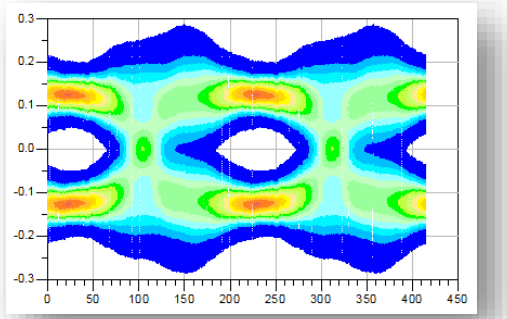
Agenda

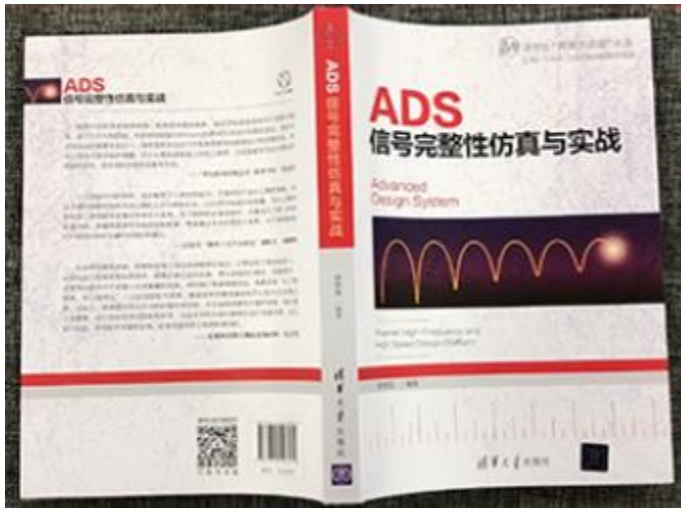
- *What is the closed loop approach*
- *Crosstalk simulation and correlation with measurement*
- *Crosstalk measurement and debug/analysis*
- *Summary*

Crosstalk Simulation and Measurement

- *Crosstalk is becoming a major challenge in design.*
- *Use close-loop approach through simulation and measurement.*
- *Simulation can help predict crosstalk issues early.*
- *Measurement with Keysight crosstalk tool can help analyze and debug issues.*







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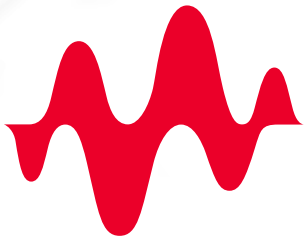

KEYSIGHT
TECHNOLOGIES