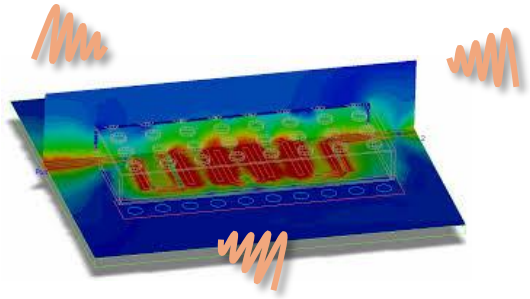
Understanding PCB Layout Effects on DC-DC Converters

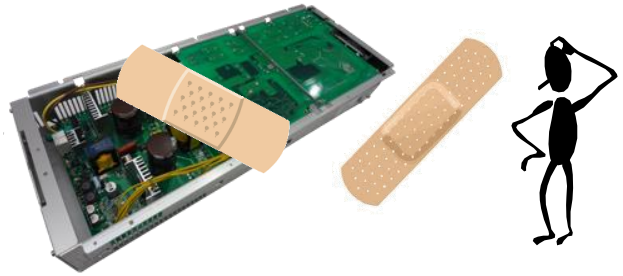
CHEN, Jason	OCT. 2019
Application Engineer	

KEYSIGHT TECHNOLOGIES

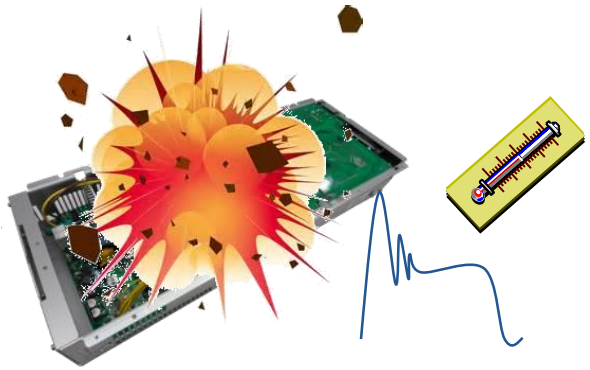
Challenges in Power Circuit Design



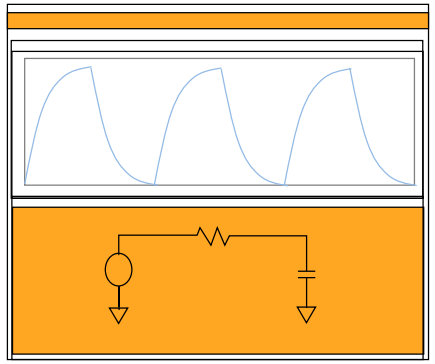
High switching frequency along with high frequency components in waveform causes unexpected EMI



High switching frequency and associated surge/ringing causes malfunction



Prototype circuit explosion due to unexpected surge

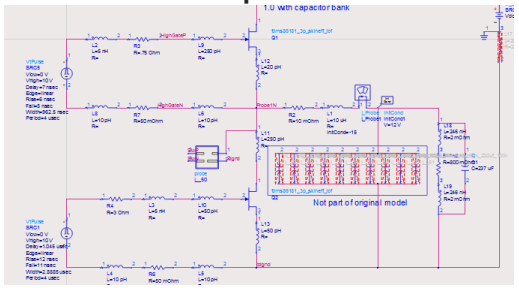


Lack of power circuit simulation tool. Conventional tool may work for low frequency circuit but not for WBG device circuit

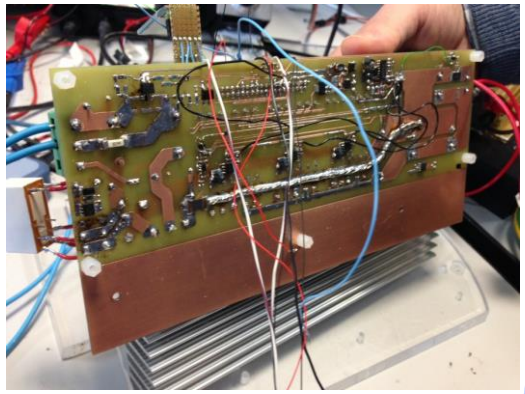
Traditional Low Speed Design Approach

PRE-LAYOUT SPICE, THEN "CUT AND TRY"

Pre-layout schematic SPICE simulation: "Best Case" performance



First prototype has some excess ringing. Cut-and-try until "best case" approached



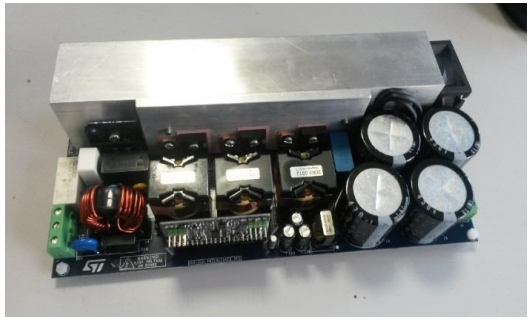
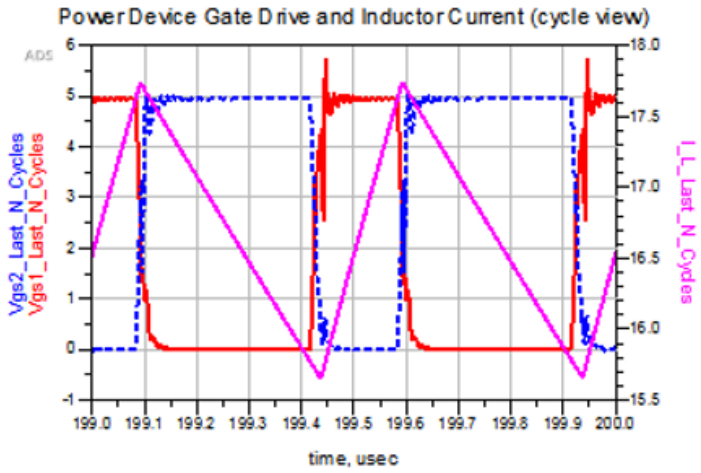
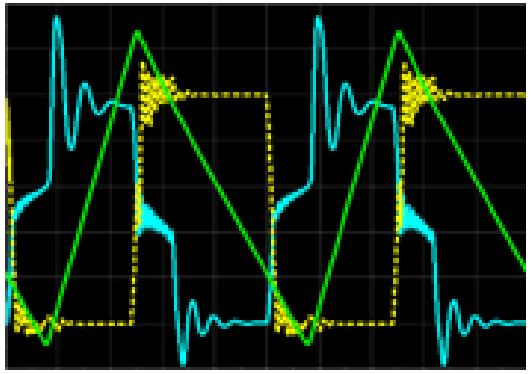
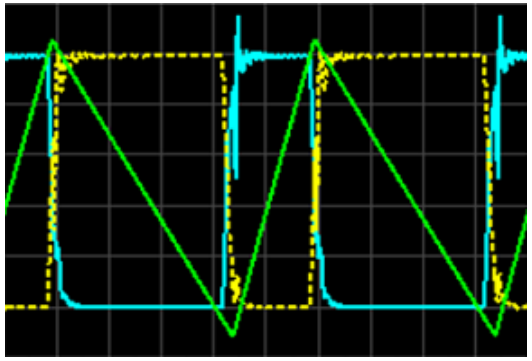


Image courtesy of ST Microelectronics

2-6 spins
$6k-$60k/spin
3-8 weeks slip/spin



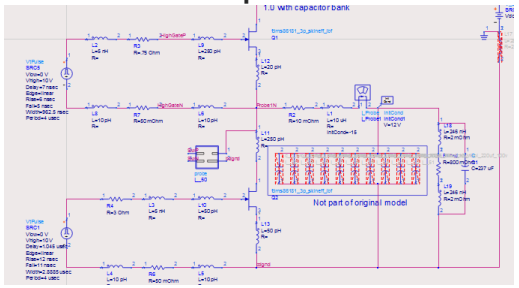


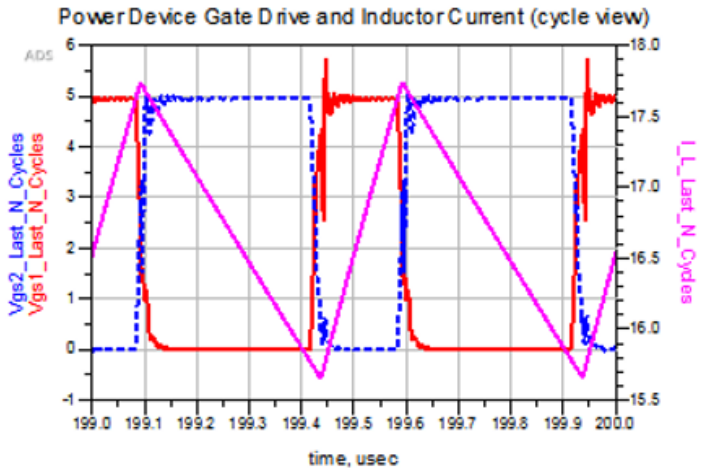


Traditional Design Approach Applied to High Speed

PRE-LAYOUT SPICE, THEN "CUT AND TRY"

Pre-layout schematic SPICE simulation: "Best Case" performance





First prototype has destructive failure.

next?

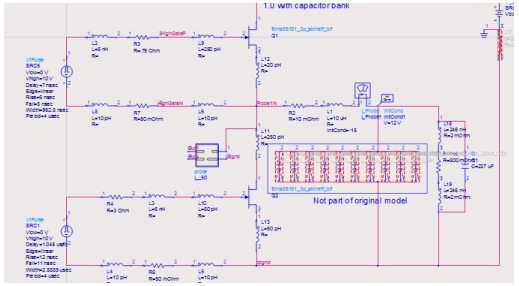
A New Approach for High Speed Design: ST Case Study

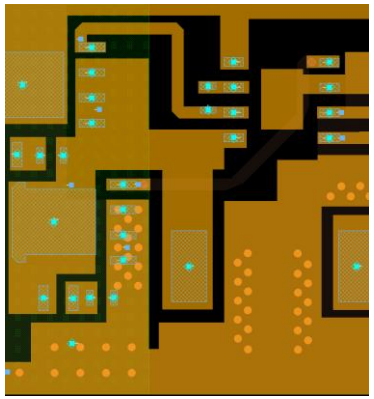
Pre-layout schematic
SPICE simulation:
“Best Case” performance

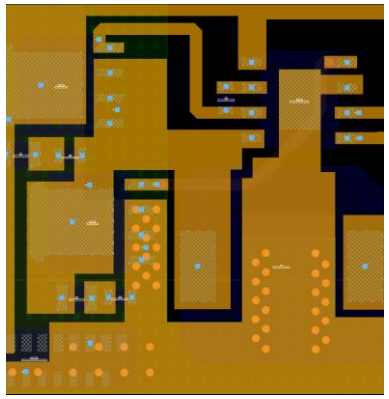
New step Post-layout = Integrated EM-circuit co-sim

First “virtual” prototype has some excess ringing.
“White box” – probe anywhere - data display – 3D visualization
Explore design space until “best case” approached

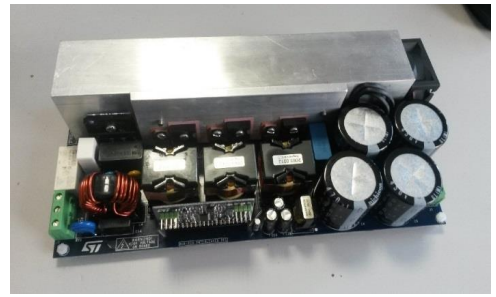
First pass success

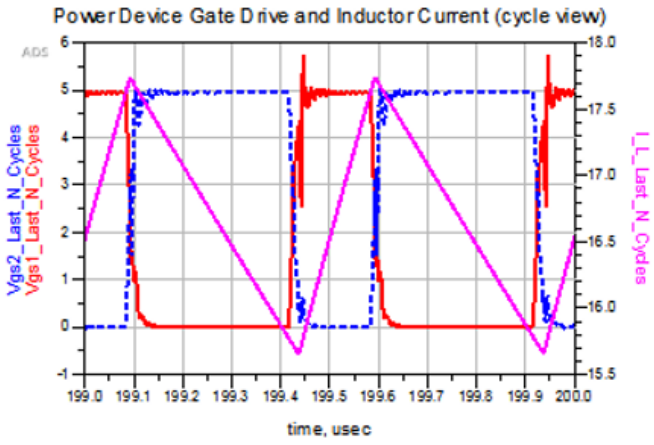


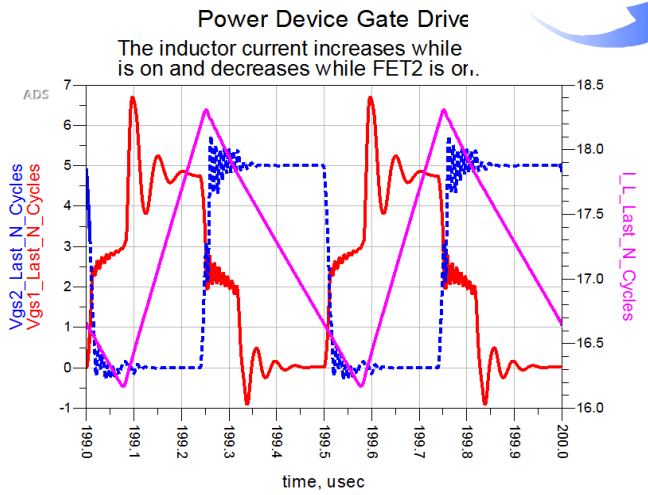


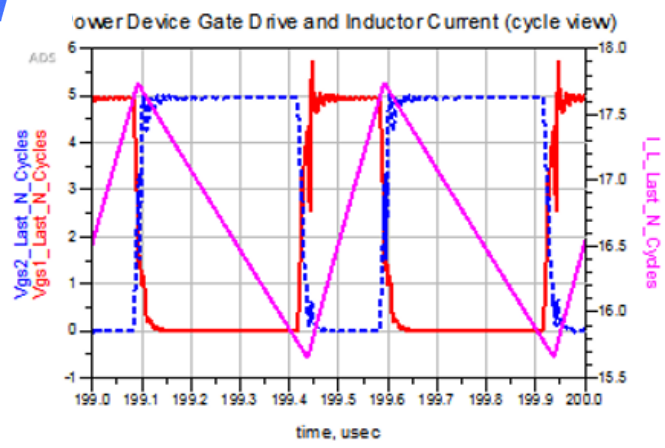


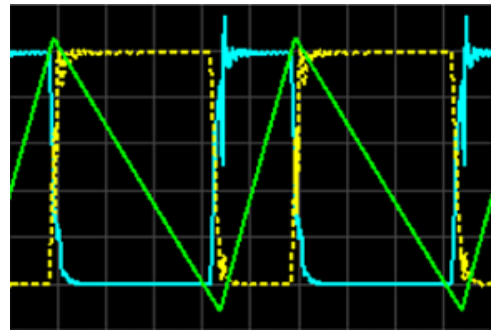
1-5 hours
/spin





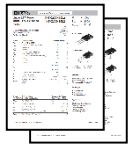




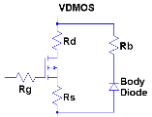


Illustrative plots: actual plots are customer proprietary

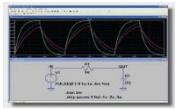
Before & After Our Solution



Unreliable vendor datasheets



poor device model to produce trustable simulation



Cheap & inaccurate SIM tool

Device selection

Device model

Circuit simulation

Prototyping / Modification

Circuit functional test

Pass

No

Repeat prototyping

Yes

Completion

Device selection

Device model

Circuit simulation

Prototyping / Modification

Circuit functional test

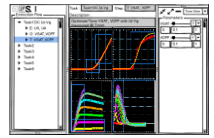
Pass

Completion

Keysight instruments

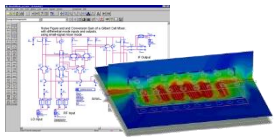
Sure selection & accurate data extraction for model creation

Keysight PE model generator



Measurement driven polynomial model based on a math model

Keysight ADS/EMPro/Momentum



Reliable time domain & EM simulation based on reliable model

Keysight Solutions for Power Electronics

PD1000A software

Test solutions

B1506A (B1505A)

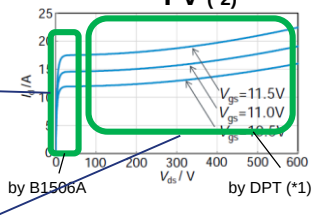
DPT(PD1500A)

ENA (E5080A)

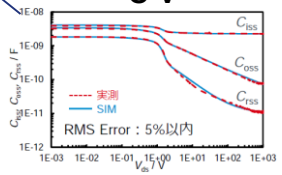
ENA w SMU

Measurement data

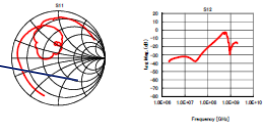
I-V (*2)



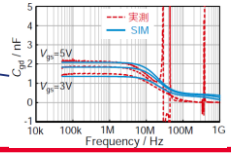
C-V



Zero-bias s-parameters

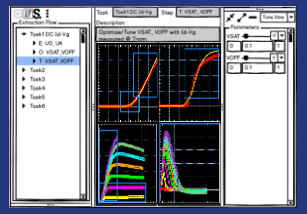


On-state C-V through S-parameters (*2)



Keysight mathematical model

W8598BP/BT Simple-use PEMG

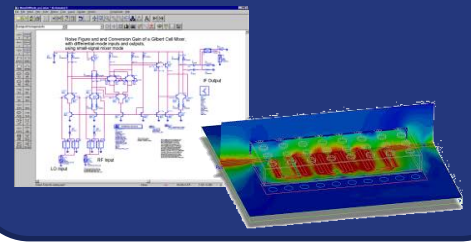


PEMG: Power Electronics Model Generator

Model parameters

Circuit/EM simulation with significantly improved accuracy

ADS / EMPro / Momentum



Physical Parasitic Effects

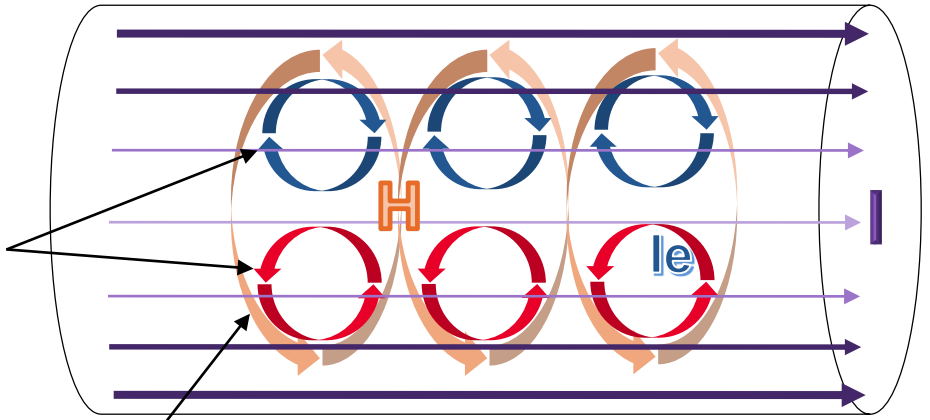
CAUSES, IMPACT, REMEDIES

Skin Effect

WHAT IS IT?

Definition: The characteristic of AC current such that the current density within a conductor is largest near the surface of a conductor, and decreases with greater conductor depth

Cause: Induced counter EMF which produces eddy currents (Ie) that oppose current flow



Magnetic field (H)

Skin Effect

CHARACTERISTICS

Current Density

Current density J decreases exponentially by the ratio of physical depth/skin depth from the surface current density Js

$$J = J_S e^{-d/\delta}$$

63% of current (I) flows within the skin depth

Skin Depth Calculation

Skin depth is highly dependent on the angular frequency

This part ~1 for $\omega < 1/(\rho\varepsilon)$ i.e. all cases we are concerned with

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \sqrt{\sqrt{1+(\rho\omega\epsilon)^2}+\rho\omega\epsilon}$$

ρ = resistivity of the conductor

ω = angular frequency of current = 2π × frequency

μ_r = relative magnetic permeability of the conductor

μ_0 = the permeability of free space

$\mu = \mu_r\mu_0$

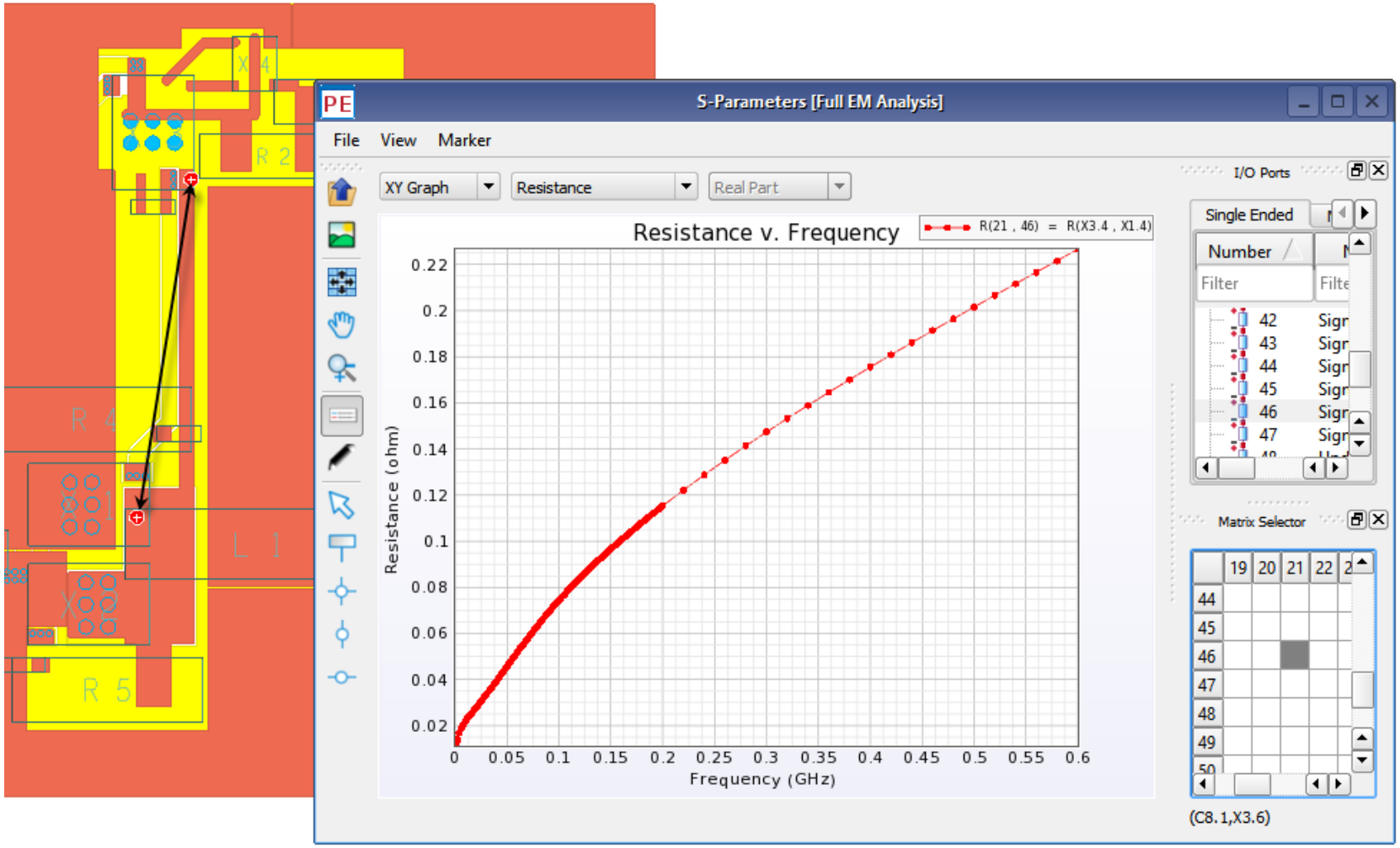
ϵ_r = relative permittivity of the material

ϵ_0 = the permittivity of free space

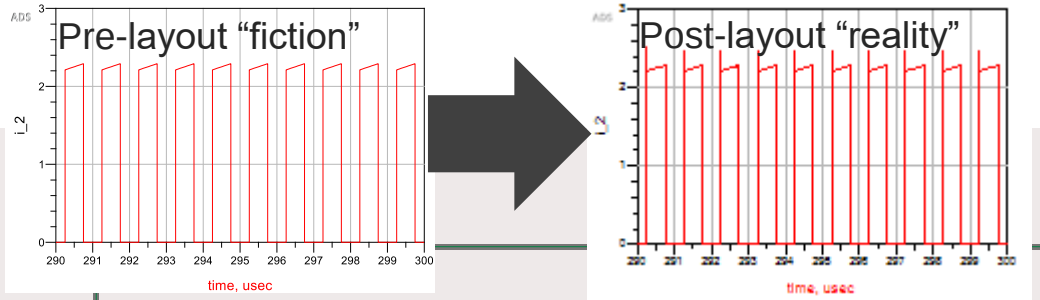
$\epsilon = \epsilon_r\epsilon_0$

Skin Depth vs Frequency		
Frequency	microns	mils
10 KHz	654	25.6
100 KHz	207	8.15
1 MHz	65	2.56
10 MHz	21	0.82
100 MHz	7	0.26

Example: Copper Trace in PEPro



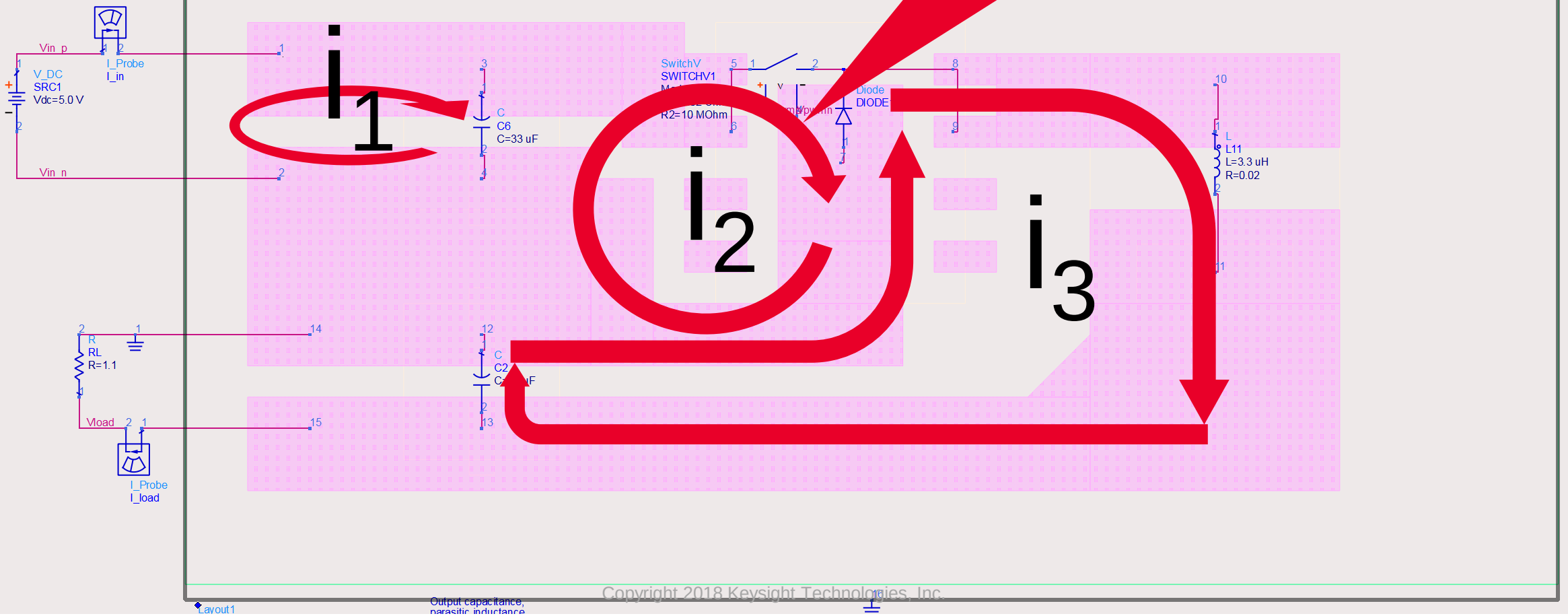
Current Loops: Layout View



When does the layout of the switched loop become important?

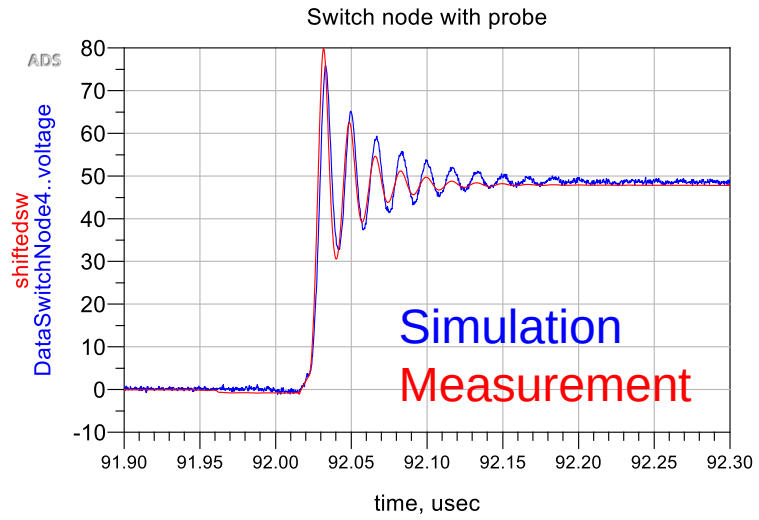
$V_{spike} = L_{parasitic} * di/dt$

$V_{spike} = L_{parasitic} * I_{on}/\tau$

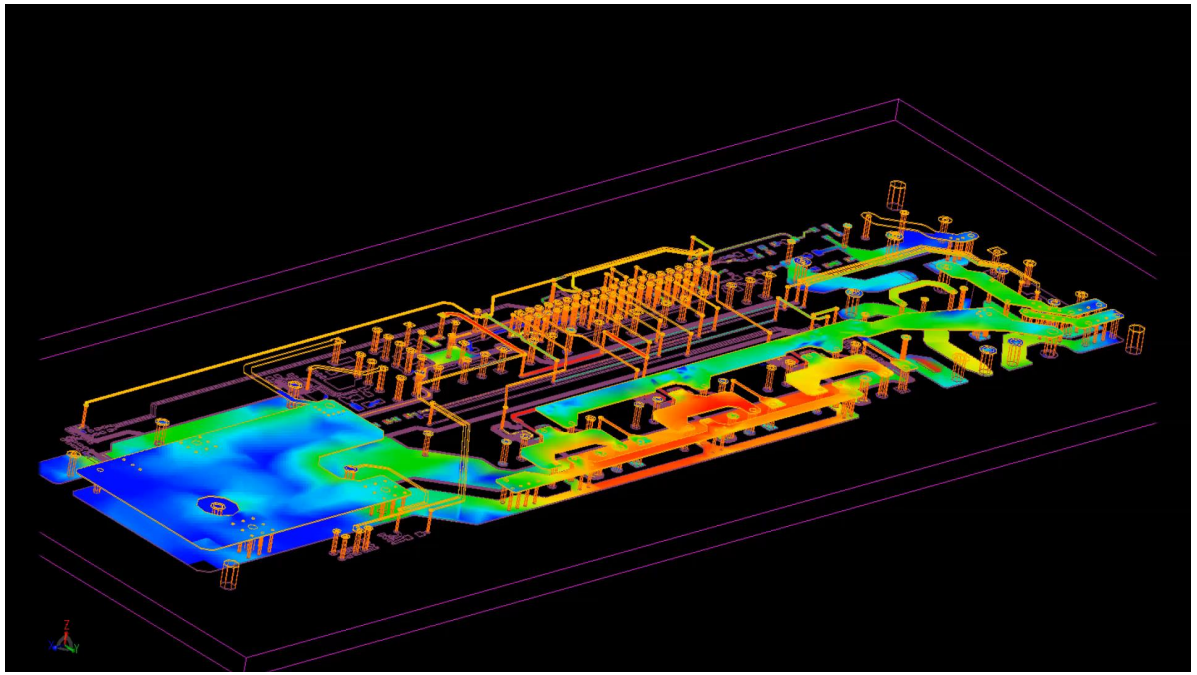


Keysight's Unique Capability: Circuit Excitation

- Like other tools, Keysight's solution shows you have a problem…



- …but unlike other tools we show you **how to fix it**. We have a unique feature called "Circuit excitation" that pinpoints the root cause.



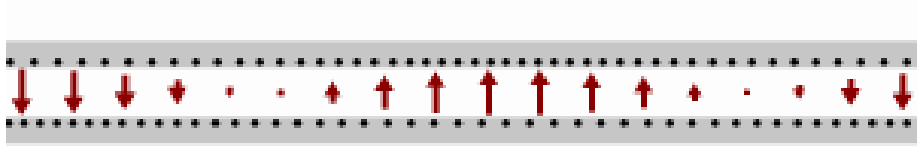
Q: How to Make a Trace Less Inductive?

1. Shorten it
2. Lower the inductance per unit length…

Q: How to Make a Trace Less Inductive Per Unit Length?

A: MAKE IT MORE LIKE A CAPACITOR!

- Fundamental reciprocal relationship between L and C for any trace (transmission line theory):
  $L = \frac{1}{v^2 C}$
  …where v is the (fixed) propagation speed, v:
  $v = \frac{c}{\sqrt{\varepsilon_r}}$
  …where c is the speed of light in vacuum



- ➔*If you increase C, L has to come down*
- It is easier to think what to do to make a bigger parallel plate capacitance $C = \frac{c}{l} = \frac{\varepsilon_0 \varepsilon_r w}{d}$ than it is to think what to do to make a smaller inductance

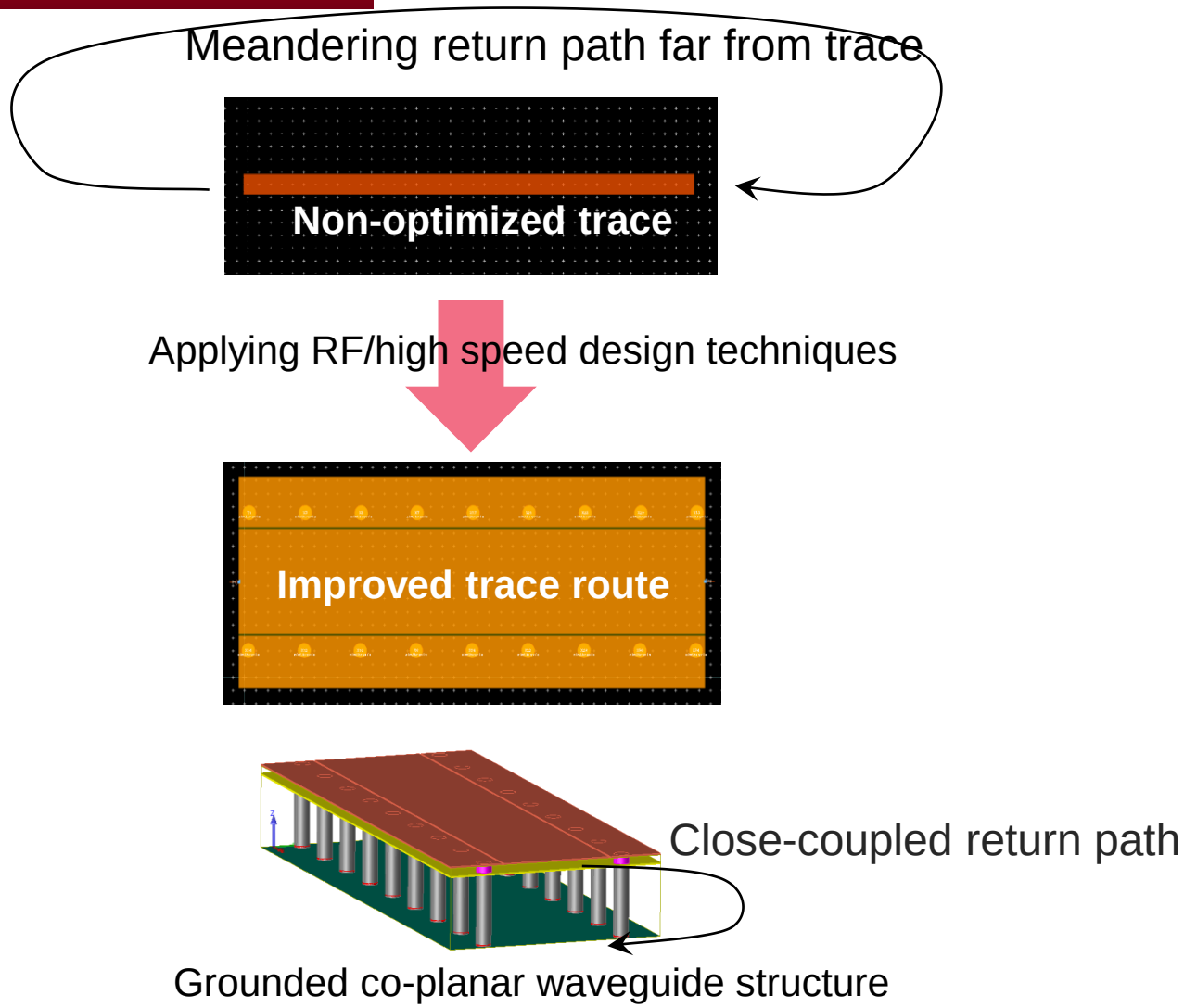
Q: How to Make a Trace Less Inductive Per Unit Length?

A: MAKE IT MORE LIKE A CAPACITOR!

- Think of a parallel plate capacitor $C = \frac{c}{l} = \frac{\varepsilon_0 \varepsilon_r w}{d}$

  Make *w* big: Make a skinny trace fatter

  Make *d* small: Current flows in loops. Bring the return path closer. Under, over, co-planar or all three.

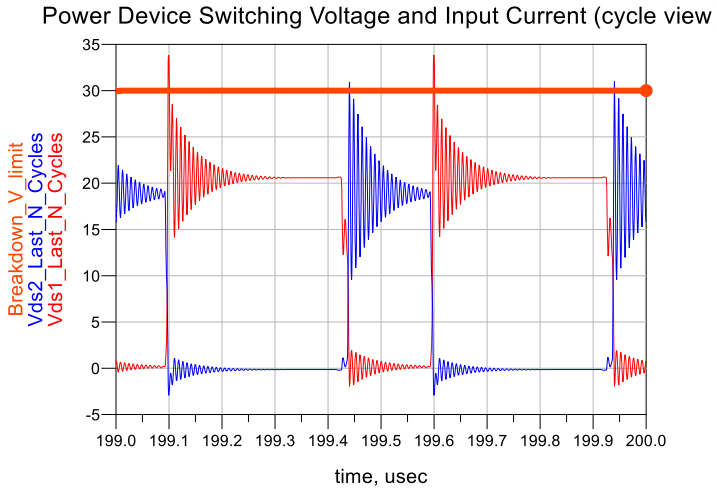


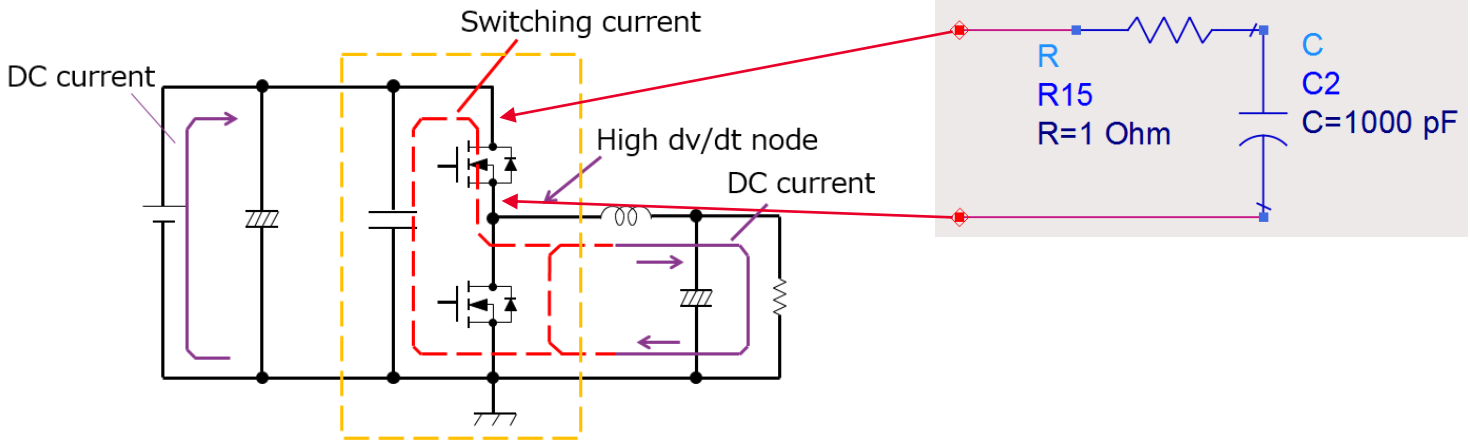
di/dt Voltage Spike Remedy

RC SNUBBERS – USED AS A LAST RESORT

Definition: A circuit which reduces spike voltage and parasitic oscillations. Parasitic oscillations occur when the surge voltage impulse excites an LC circuit.

Snubbing circuits are usually placed across high dv/dt switching nodes





RC snubbers <u>always decrease efficiency</u>.

- Rsnub dissipates heat directly
- Csnub stores energy= ½ x C_{snub} x V^2 which is dissipated every cycle

di/dt Voltage Spike Remedy

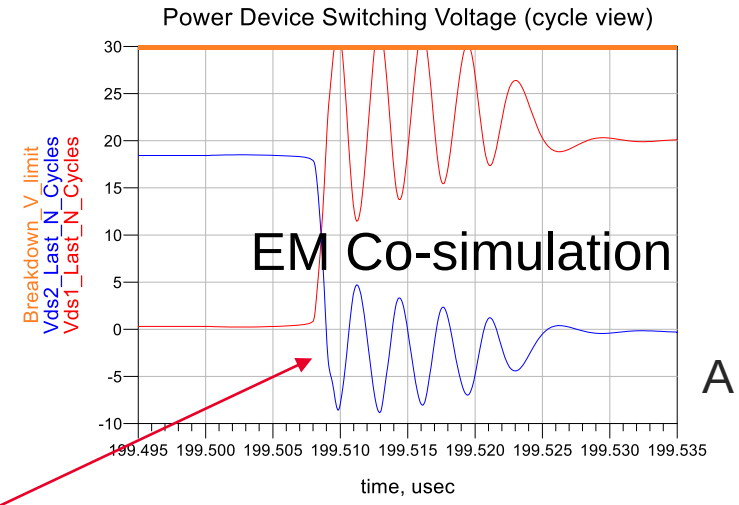
RING FREQUENCY DESIGN METHODOLOGY

Frequency ringing method: Choose R_{snub}, determine frequency of ringing, back solve for C_{snub}.

$$C_{snub} = 3 \times T_{ring}/R_{snub}$$

T_{ring} can be found by simulation. Use results determined from EM Co-simulation!

Note: There many papers on snubber design e.g. William McMurray, OPTIMUM SNUBBERS FOR POWER SEMICONDUCTORS, IEEE IAS transactions, Vol. IA-8, No. 5, Sept/Oct 1972, pp. 593-600



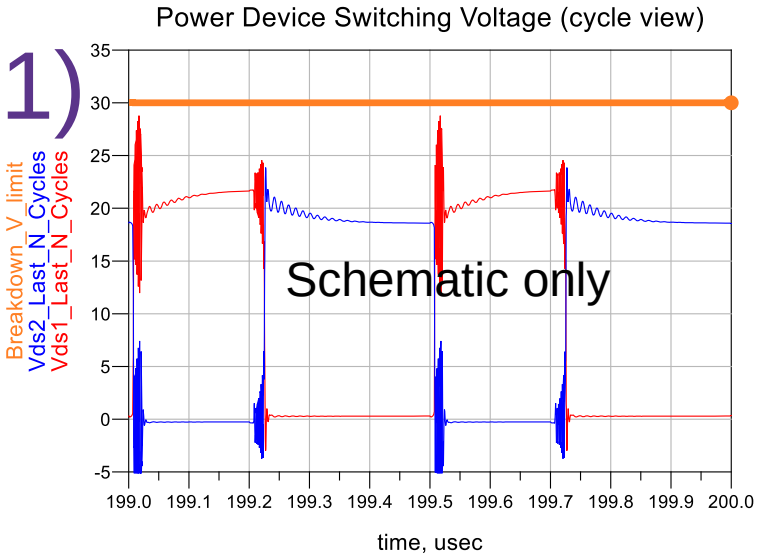
A more accurate result

T_{ring}

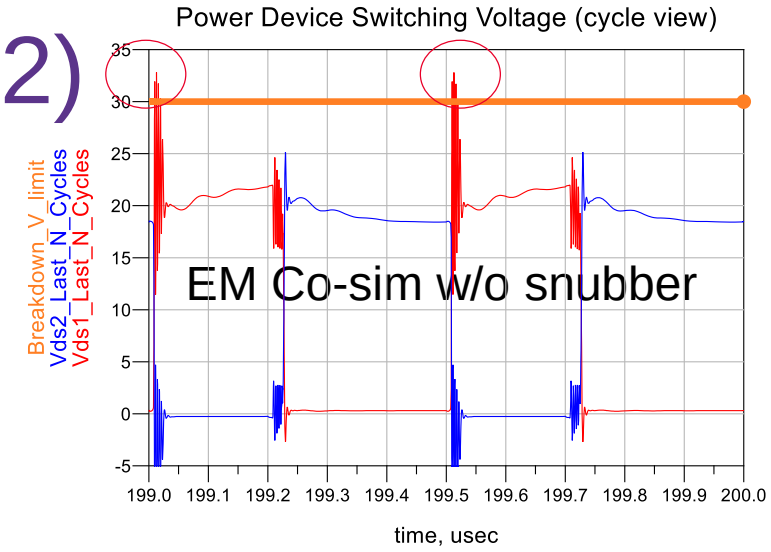
di/dt Voltage Spike Remedy

APPLYING THE RING FREQUENCY DESIGN METHOD

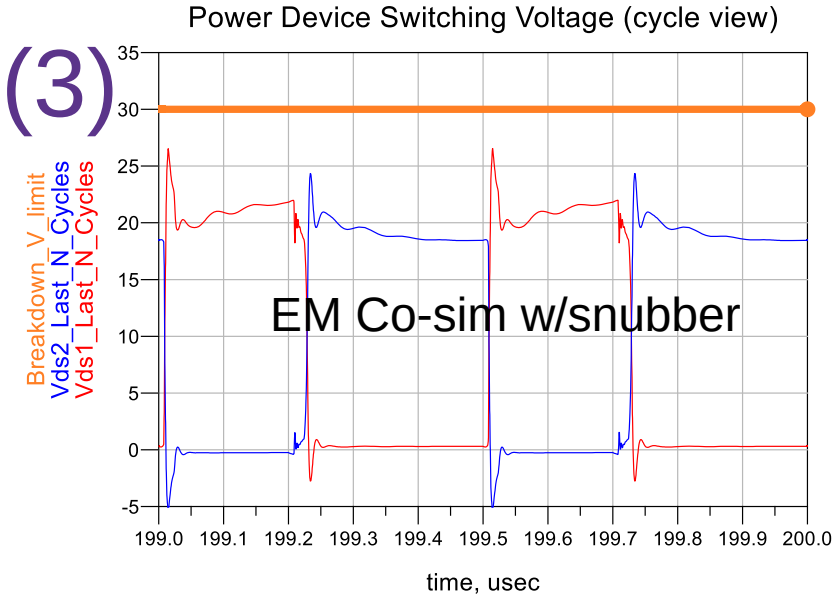
(1)



(2)



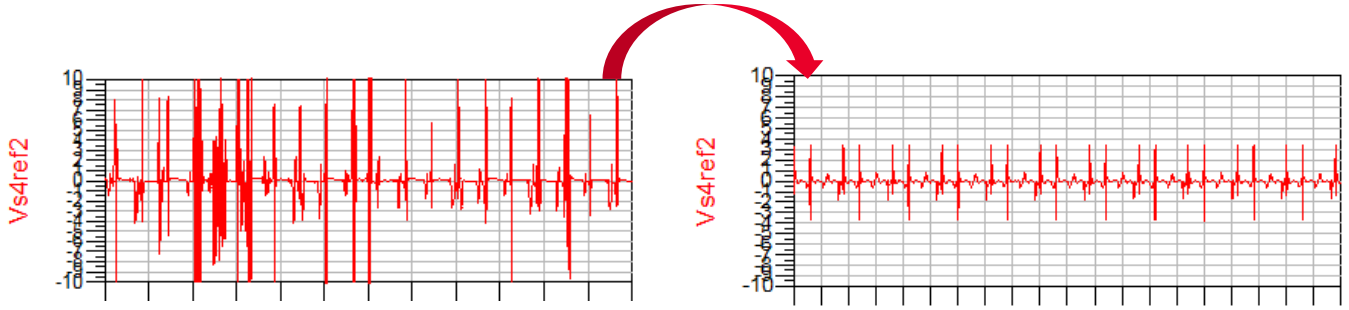
(3)



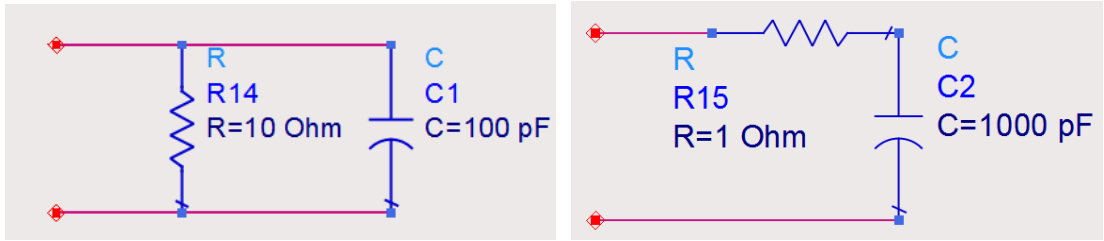
di/dt Voltage Spike Remedy Summary

TRACE LAYOUT, SNUBBING

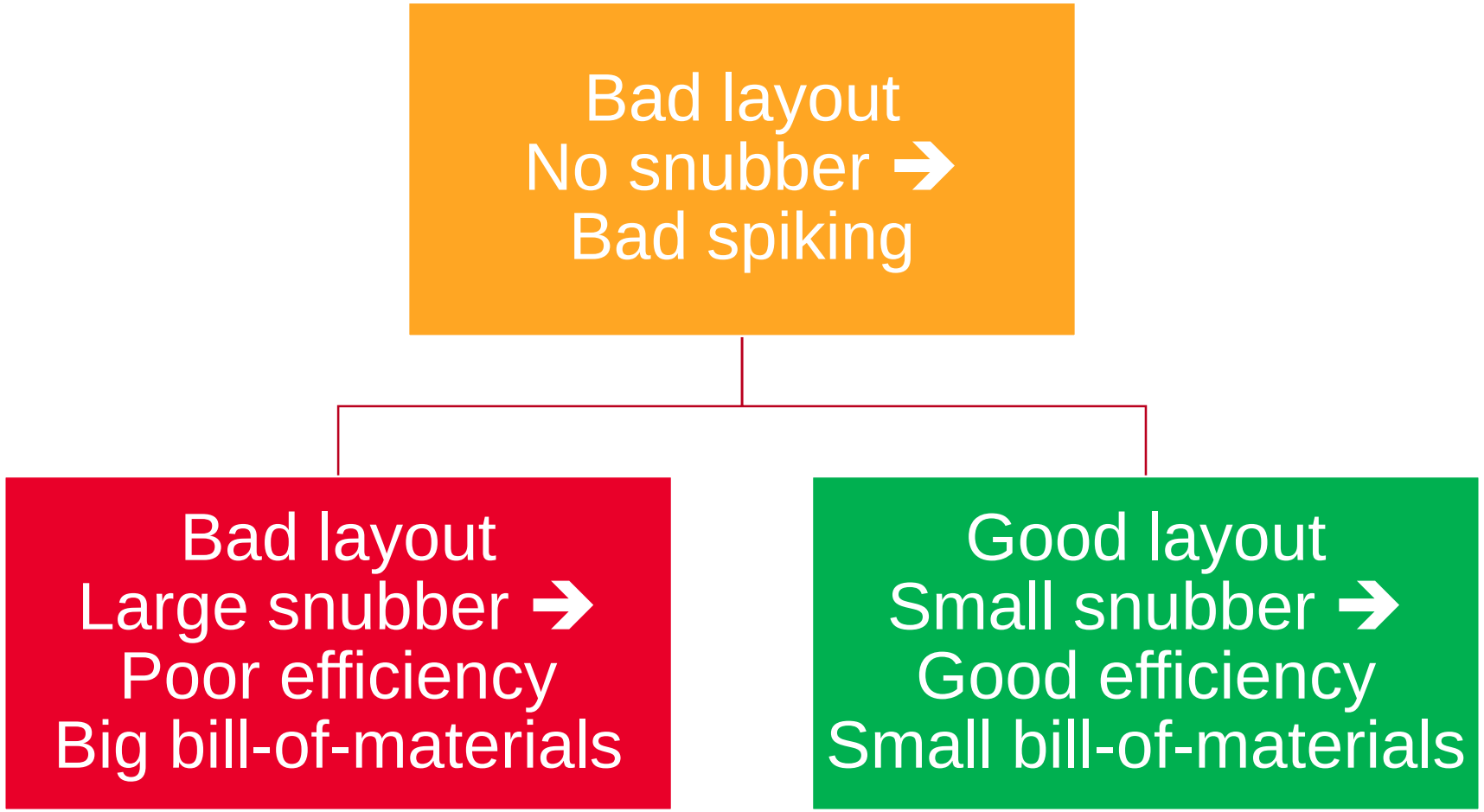
Trace layout:
Lower L di/dt by widening traces, shrinking route length, increasing capacitance, careful via placement



Loading/snubbing:
Resistive/capacitive loads and snubbing circuits can be used to control surge voltage, but sacrifices efficiency



Don’t Add a Snubber Until the Layout is as Good as it Can Be

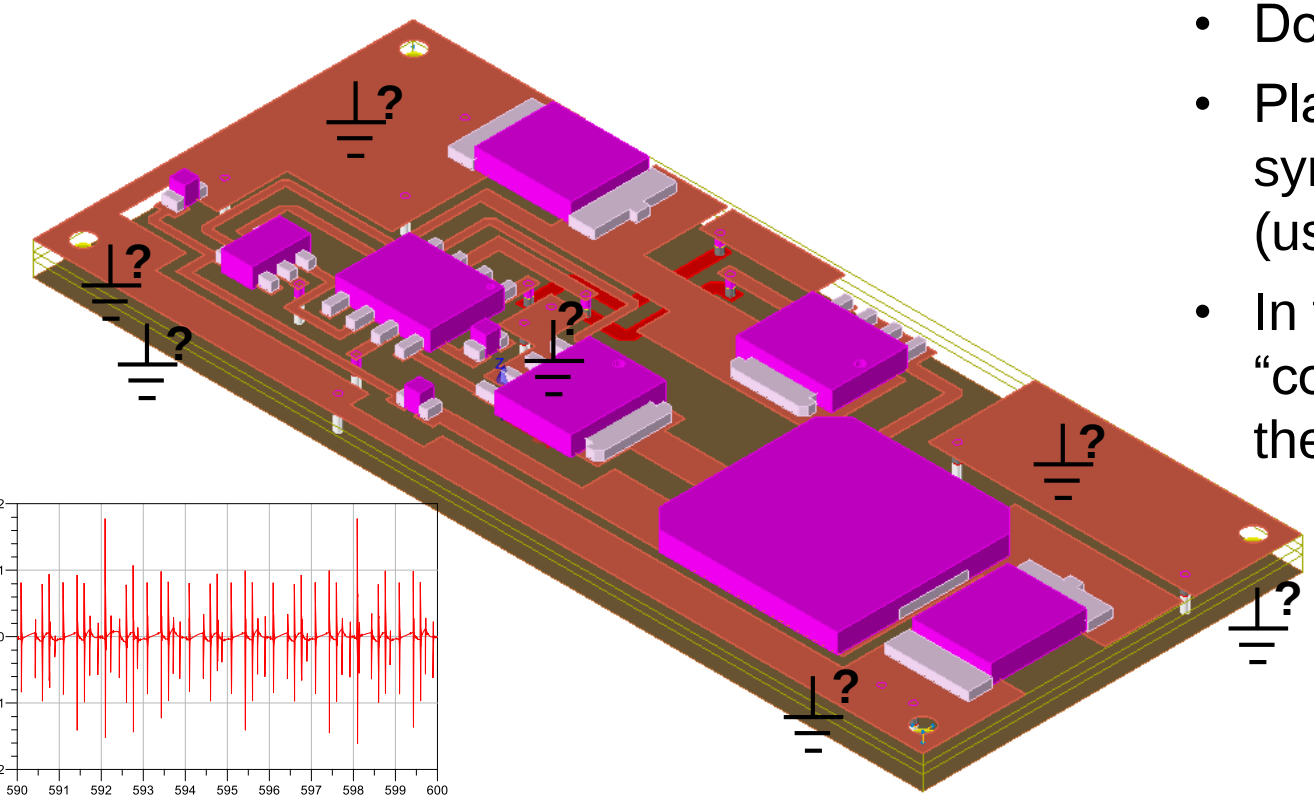


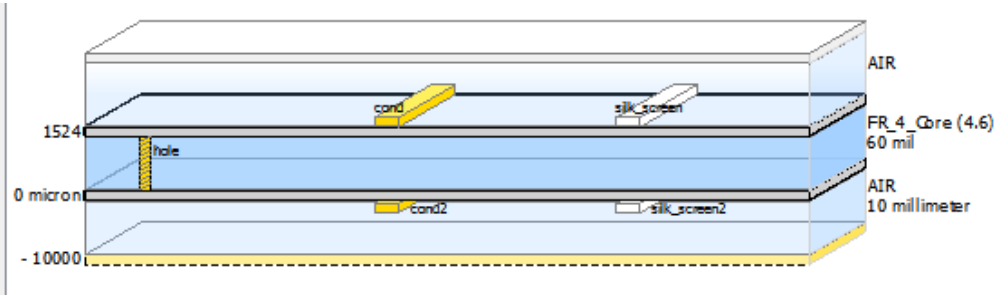
The “Ground” Myth

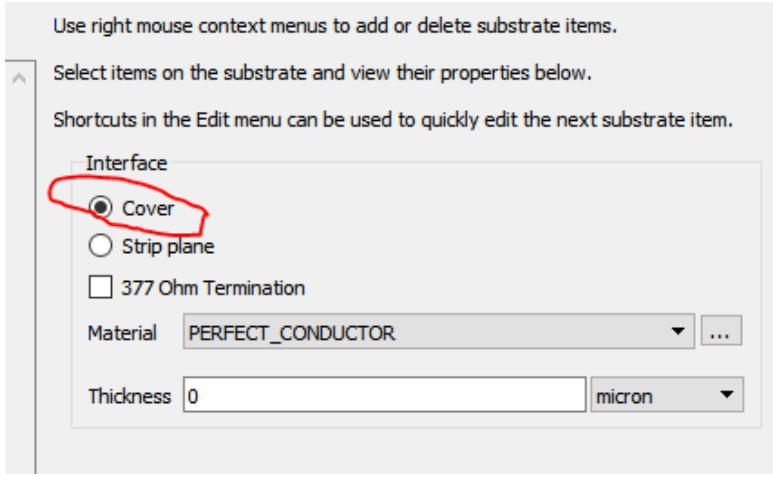
“Ground is a place where potatoes and carrots thrive!”
Dr. Bruce Archambeault,
IBM Distinguished Engineer
IEEE Fellow
http://web.mst.edu/~jfan/slides/Archambeault2.pdf

Forget ground, think “return path”

- Don’t place multiple ground symbols
- Place one and only one “chassis ground” symbol at the point that makes most sense (usually the ground ref. of the input power port)
- In the substrate editor, use a conceptual “cover” layer as “chassis ground” reference for the EM extraction



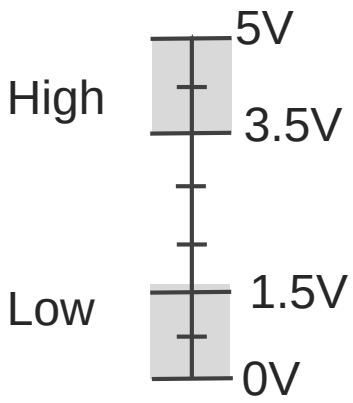


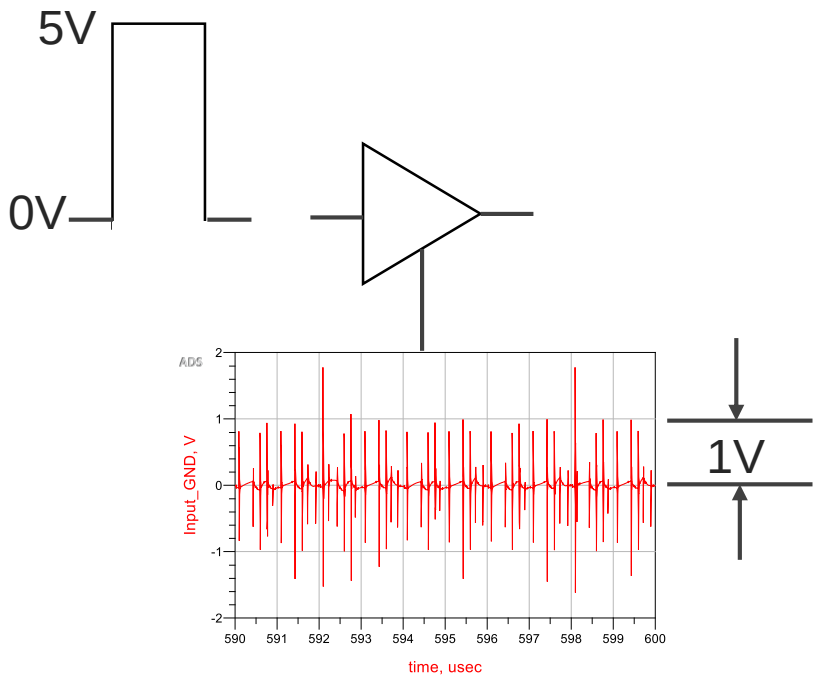


The Impact on Noise Immunity

GAINING INSIGHTS INTO THE DESIGN

- When the grounds of a logic gate contain noise, the noise immunity of the gate decreases.
- The logic gate sees the signal appearing at its input pin with respect to its local ground.

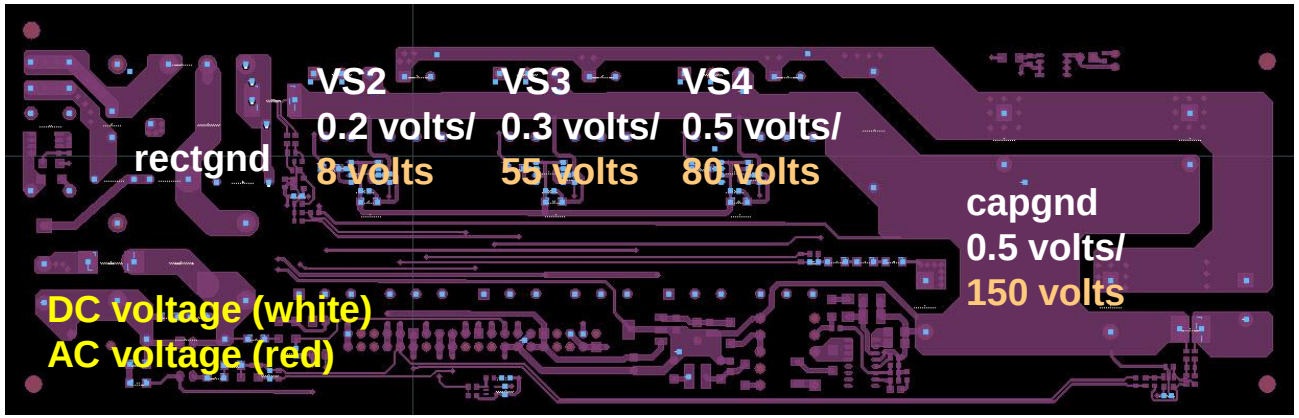




Noise margin = 1.5V – 1V

Ground Mismatch Example

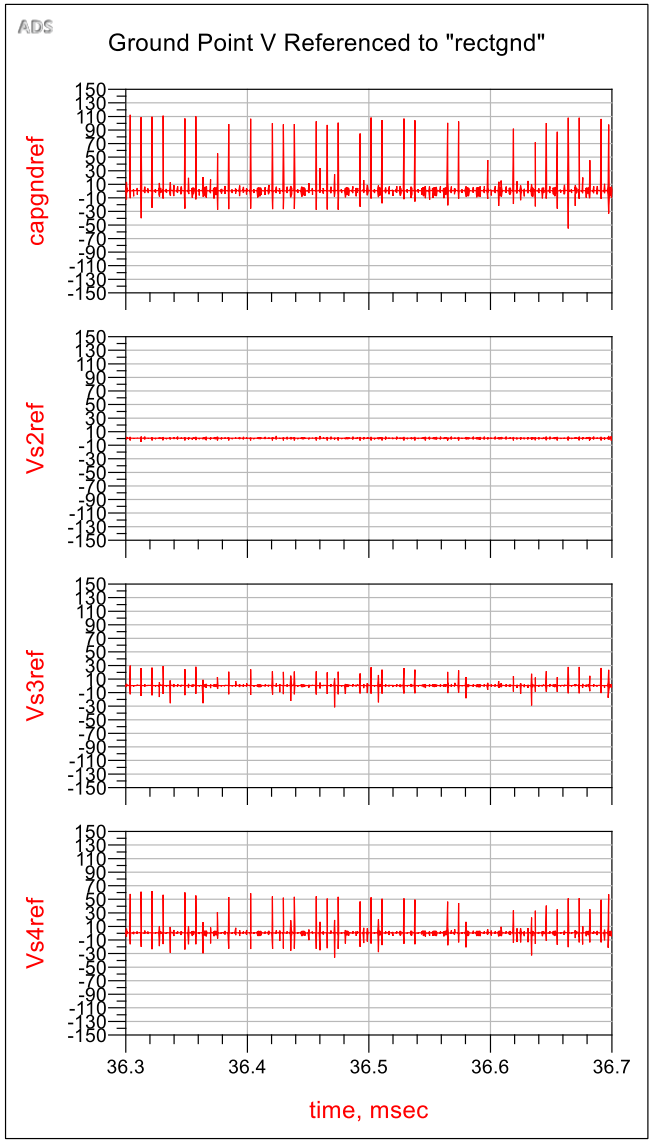
VOLTAGE VARIANCE ACROSS A GROUND PLANE



Each point on a power plane or trace has:

- IR drop (**DC component**)
- di/dt (**AC component**)
  - Different amplitude
  - Not necessarily coherent

Each point is different!



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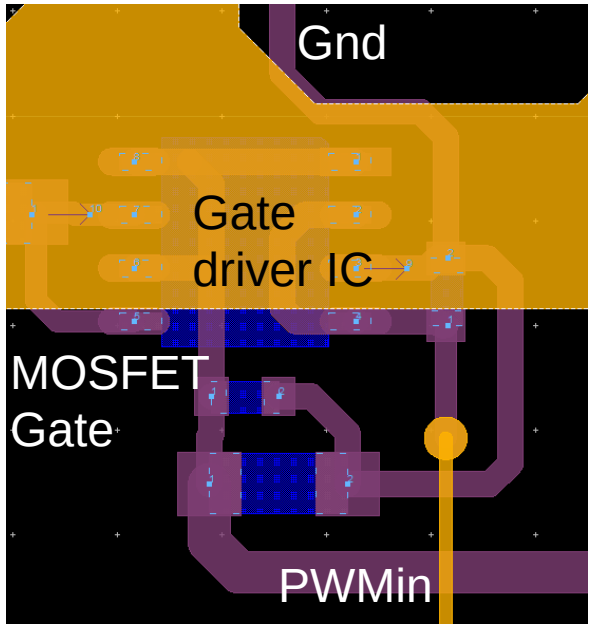
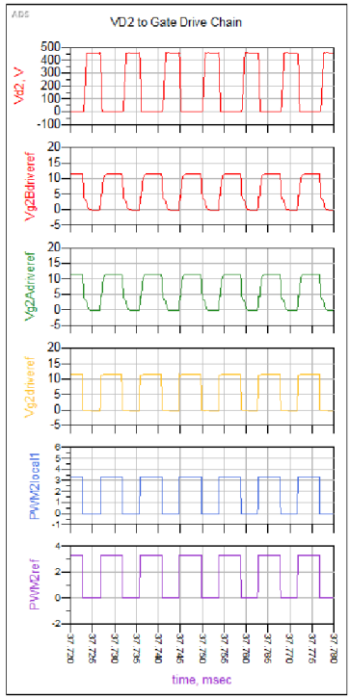
Ground Mismatch Example

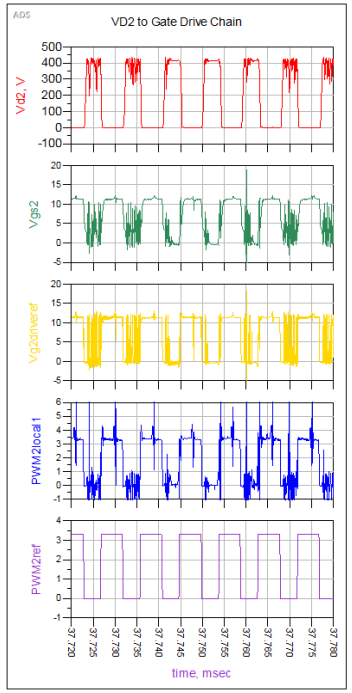
EVERYTHING IS RELATIVE!

- It is important to understand the relative voltages around a component.
- Signals going into or out of a device are referenced to the local ground
- Noise levels are different across a ground plane and not necessarily coherent





Schematic only



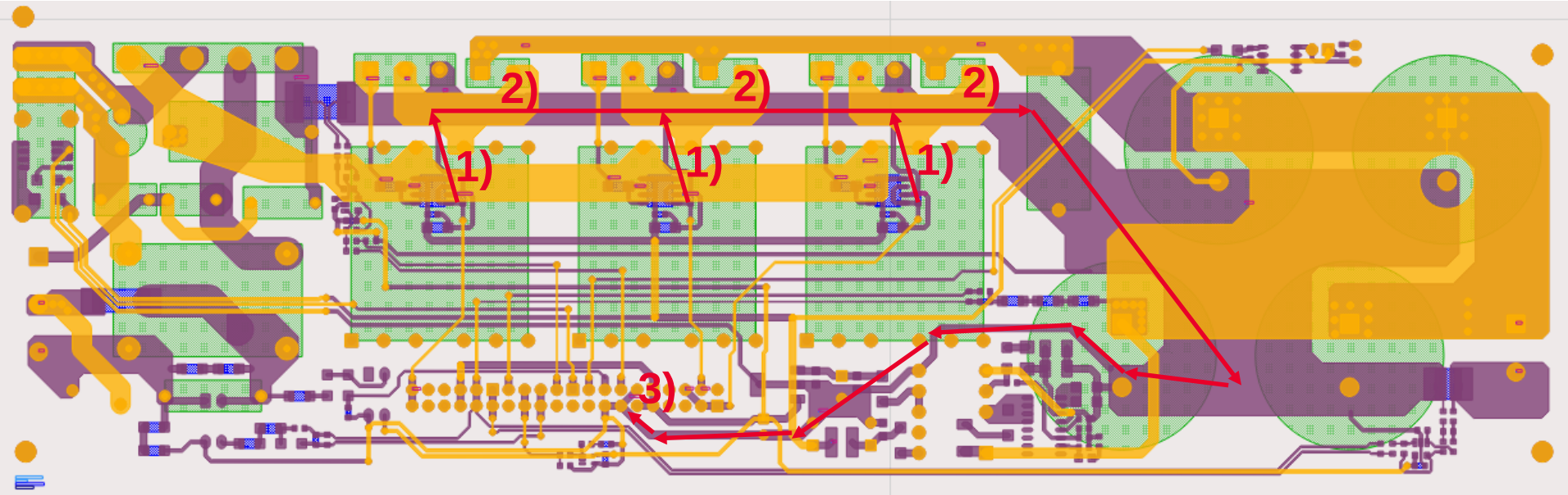
EM Co-simulation

These signals are relative to local gate driver ground

PWM signal relative to local PWM ground

Ground Mismatches:

EM CO-SIMULATION HELPED WITH DIAGNOSIS



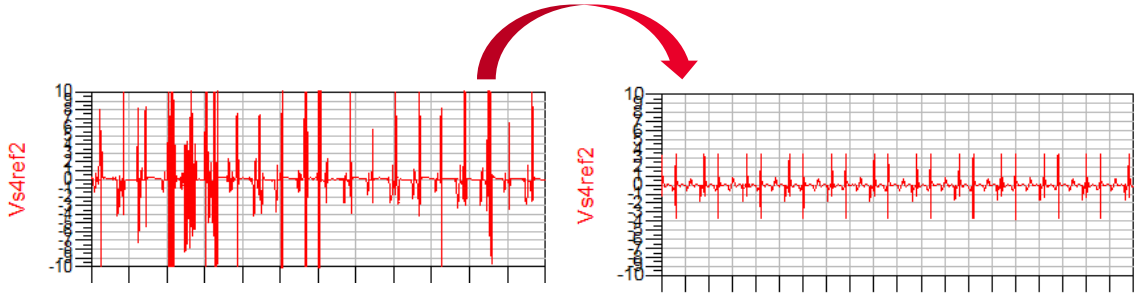
1) Gate driver grounds
2) Ground plane connecting the power transistors
3) PWM ground

Root cause: Excessive ground path from the PWM to the gate drivers, grounds are mismatched along path

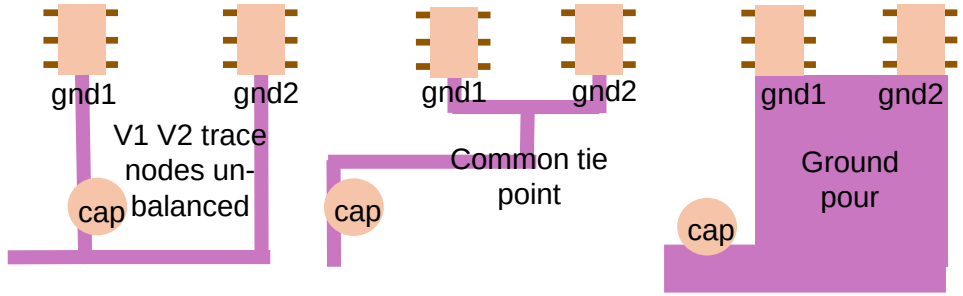
Ground Mismatch Reduction

PHYSICAL LAYOUT REMEDIES

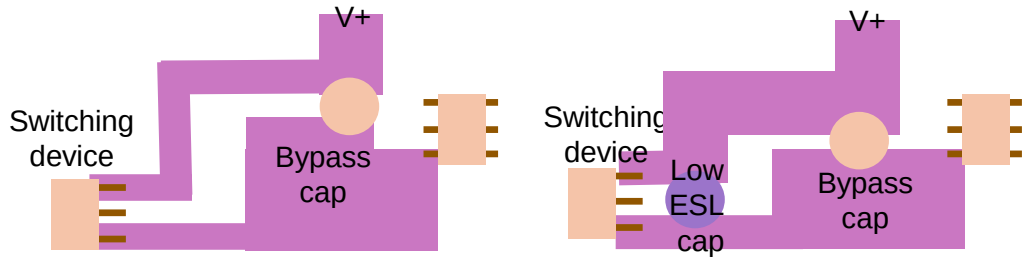
Trace layout:
Reduce IR drop & di/dt by widening traces, shrinking route length. Reduce high current loops



Ground tying:
Adjust routing to balance ground between critical nodes (V1 & V2)



Low ESL capacitors:
Add where large switching transients are generated and between critical components



Suppressing Voltage Spikes

HIGH VOLTAGE, LOW ESR CAPACITORS

Consider a 2.2 uF, 600V poly film low ESR capacitor

- 33 mOhm ESR
- 18 nH lead inductance!

Observations:

- Higher voltage capacitors have more lead inductance
- Fast switching glitches: rise times are only a few nS!
- Lead inductance may prevent the capacitor from functioning properly

TDK

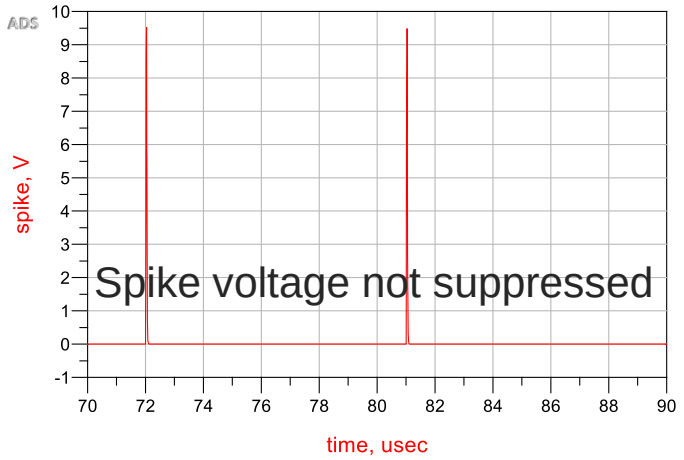
B32671Z ... B32673Z

Power Factor Correction

MKP

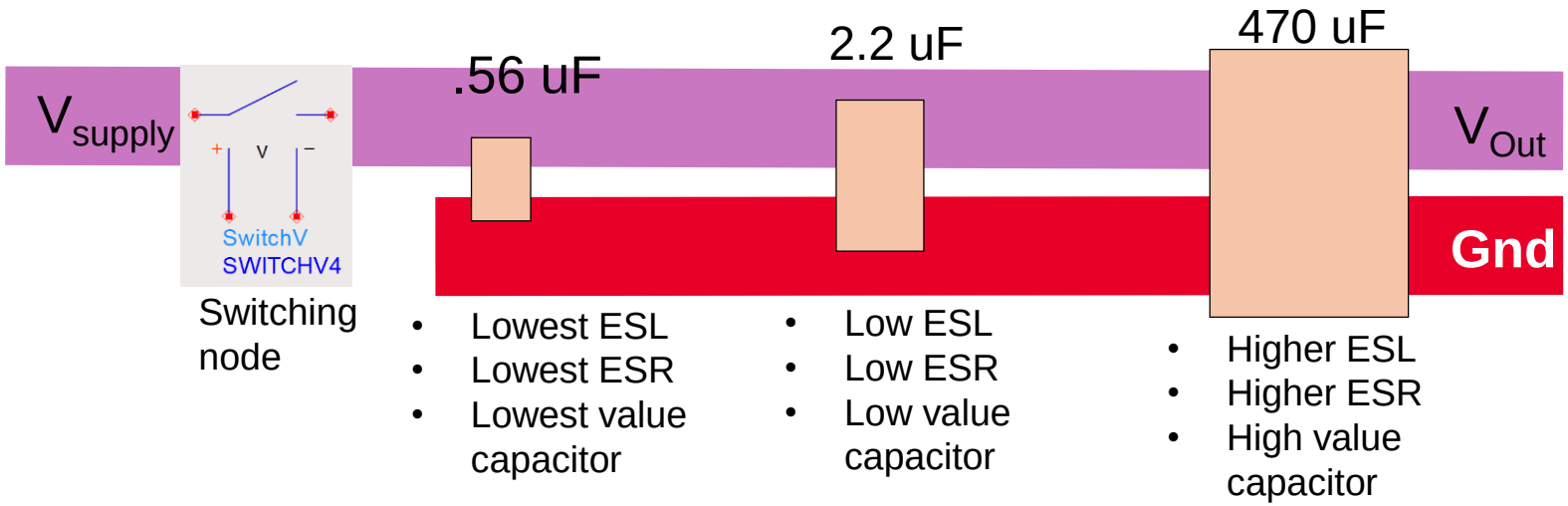
Technical data

Max. operating temperature $T_{op,max}$	+125 °C		
Dissipation factor tan δ (in 10^{-3}) at 20 °C (upper limit values)		$C_R \le 0.1$ µF	0.1 µF< C_R
	at 1 kHz	≤ 1 (typically 0.6)	1.0
	100 kHz	5.0	–
Insulation resistance R_{ins} or time constant $\tau = C_R \cdot R_{ins}$ at 20 °C, rel. humidity ≤ 65% (minimum as-delivered values)	> 30 000 MΩ	($C_R \le 0.33$ µF)	
	> 10 000 s	($C_R > 0.33$ µF)	
Total self-inductance L (lead length ≈ 3mm)	LS 15 mm	10 nH	
	LS 22.5 mm	18 nH	
DC test voltage	1.6 × V_R, 2 s		
Category voltage V_C (continuous operation with V_{DC} or V_{AC} at f ≤ 1 kHz)	T_A (°C)	DC voltage derating	AC voltage derating
	$T_A \le 85$	$V_C = V_R$	$V_{C,RMS} = V_{RMS}$
	$85 < T_A \le 110$	$V_C = V_R \cdot (165 - T_A)/80$	$V_{C,RMS} = V_{RMS} \cdot (165 - T_A)/80$
Operating voltage V_{op} for short operating periods (V_{DC} or V_{AC} at f ≤ 1 kHz)	T_A (°C)	DC voltage (max. hours)	AC voltage (max. hours)
	$T_A \le 100$	$V_{op} = 1.25 \cdot V_C$ (2000 h)	$V_{op} = 1.0 \cdot V_{C,RMS}$ (2000 h)
	$100 < T_A \le 125$	$V_{op} = 1.25 \cdot V_C$ (1000 h)	$V_{op} = 1.0 \cdot V_{C,RMS}$ (1000 h)



Suppressing Voltage Spikes

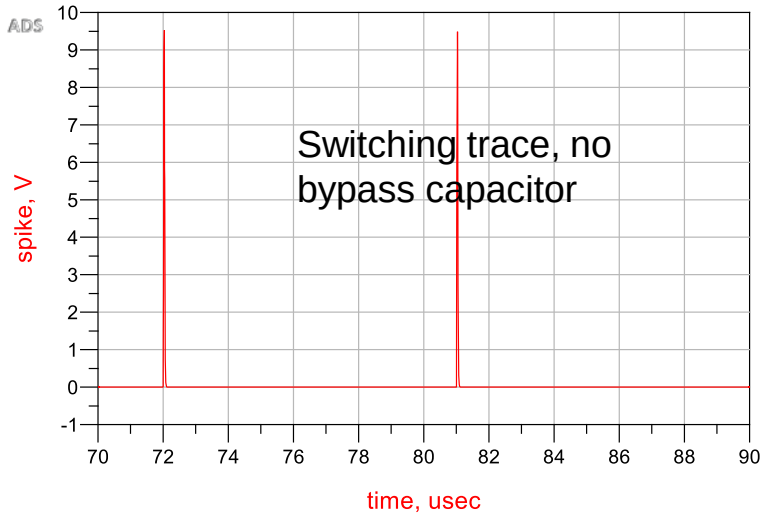
STAGGERED BYPASS CAPACITORS

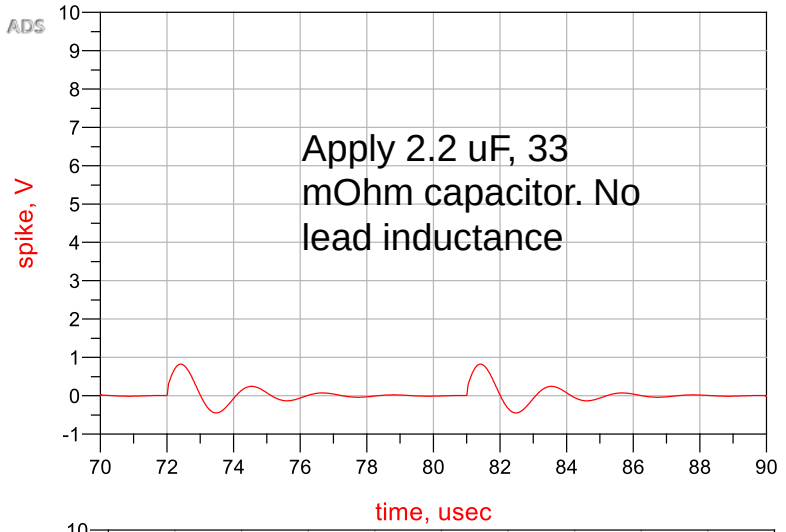


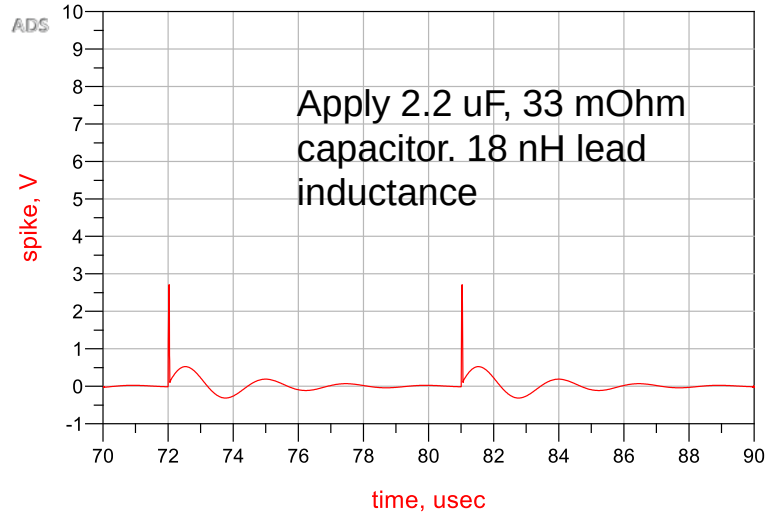
Low ESL capacitors:
Stagger capacitor types between the switching node and the output with lowest ESL capacitors nearest the switching node

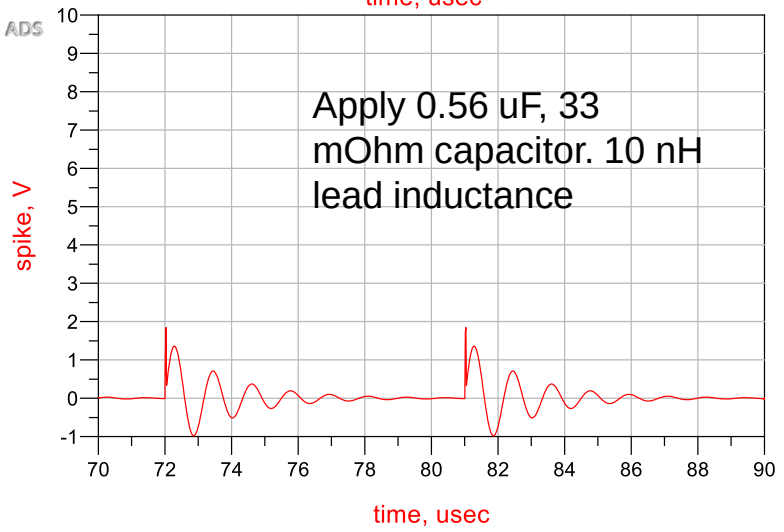
Application of HV, Low ESR Capacitors

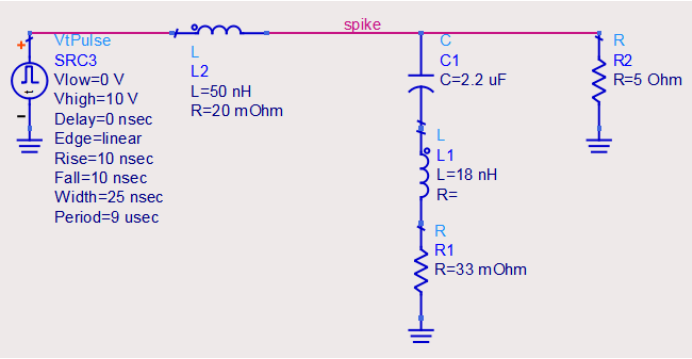
BIGGER IS NOT NECESSARILY BETTER



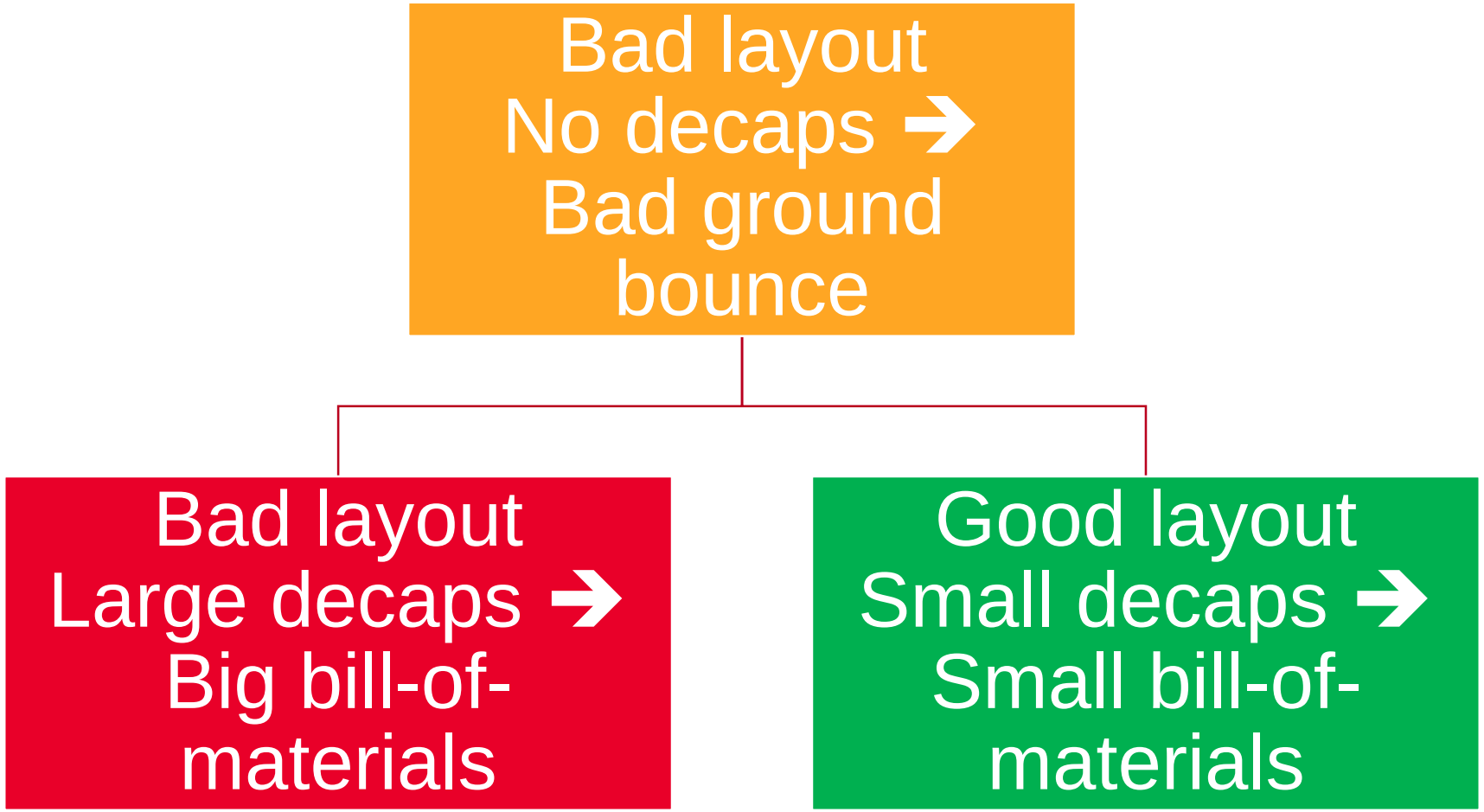








Don’t Add Decaps Until the Layout is as Good as it Can Be

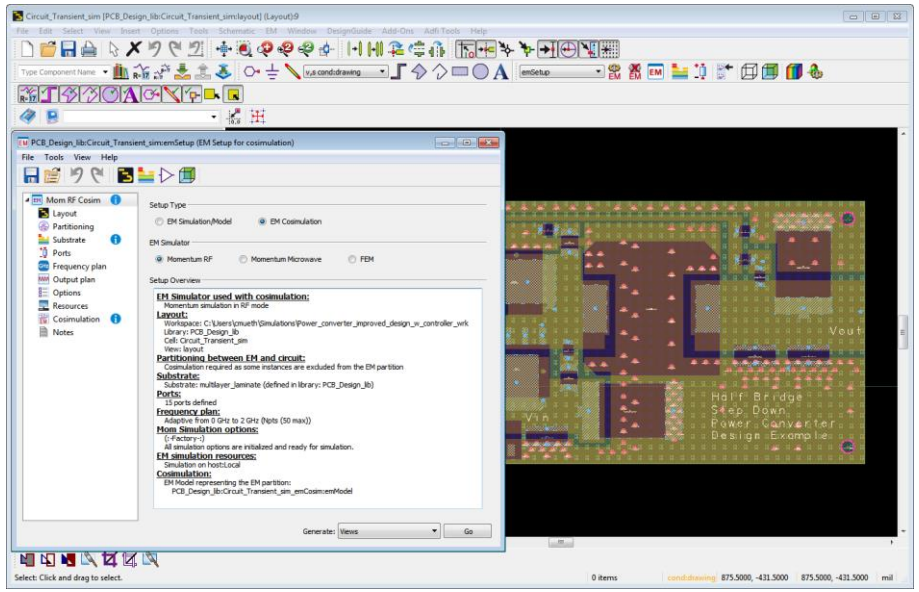


Troubleshooting Parasitic Effects

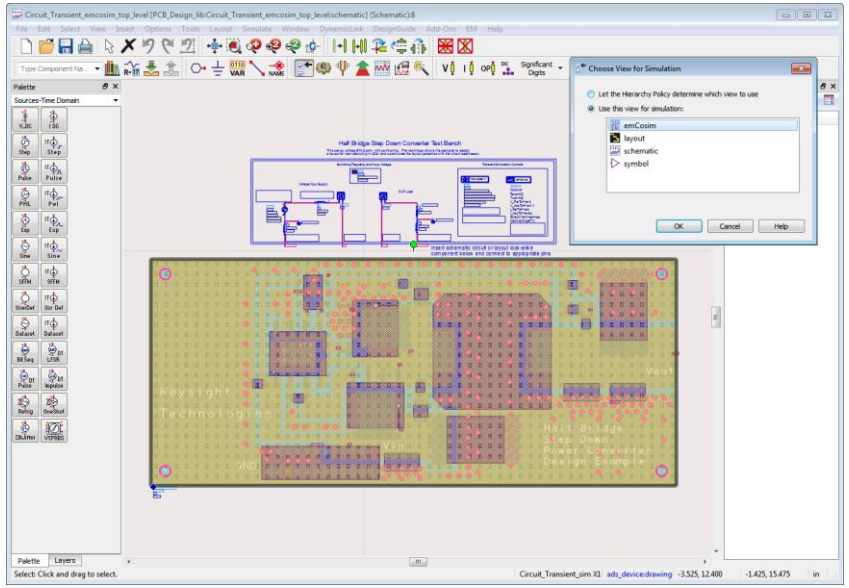
TOOLS, TECHNIQUES, POST PROCESSING

Tools – Time for a Demo?

USING ADS FOR EM CO-SIMULATION



Layout and schematic are tied together



- EM technologies can be applied to the layout
- Method of Moments EM provides the best balance of speed and accuracy for planar designs

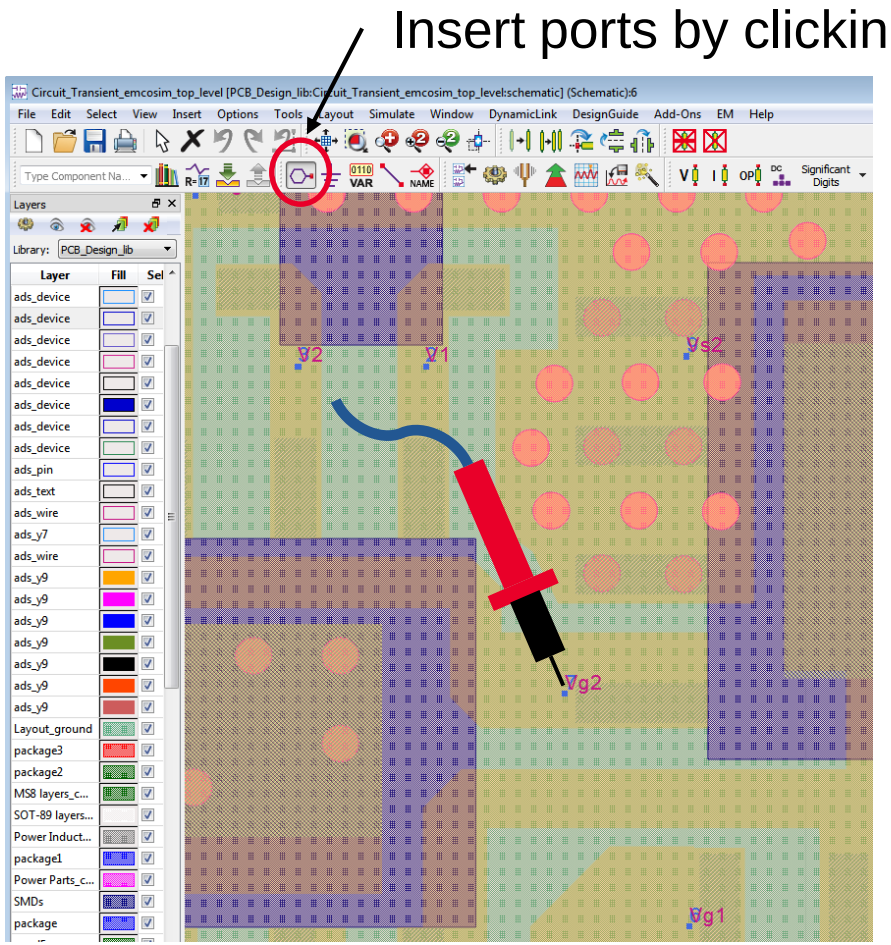
- Simulation can be switched between a schematic and EM co-sim view
- EM is utilized with transient or harmonic balance circuit simulation

** EM Co-simulation is covered in detail as a separate topic*

Probing areas of Interest

PROBES ARE EASILY PLACED IN THE LAYOUT

- Probes can be placed at any critical voltage node (like FET gate, drain, gate driver inputs, gnd, etc.)
- Probes can also be placed along a trace plane at different spots to gain di/dt insights

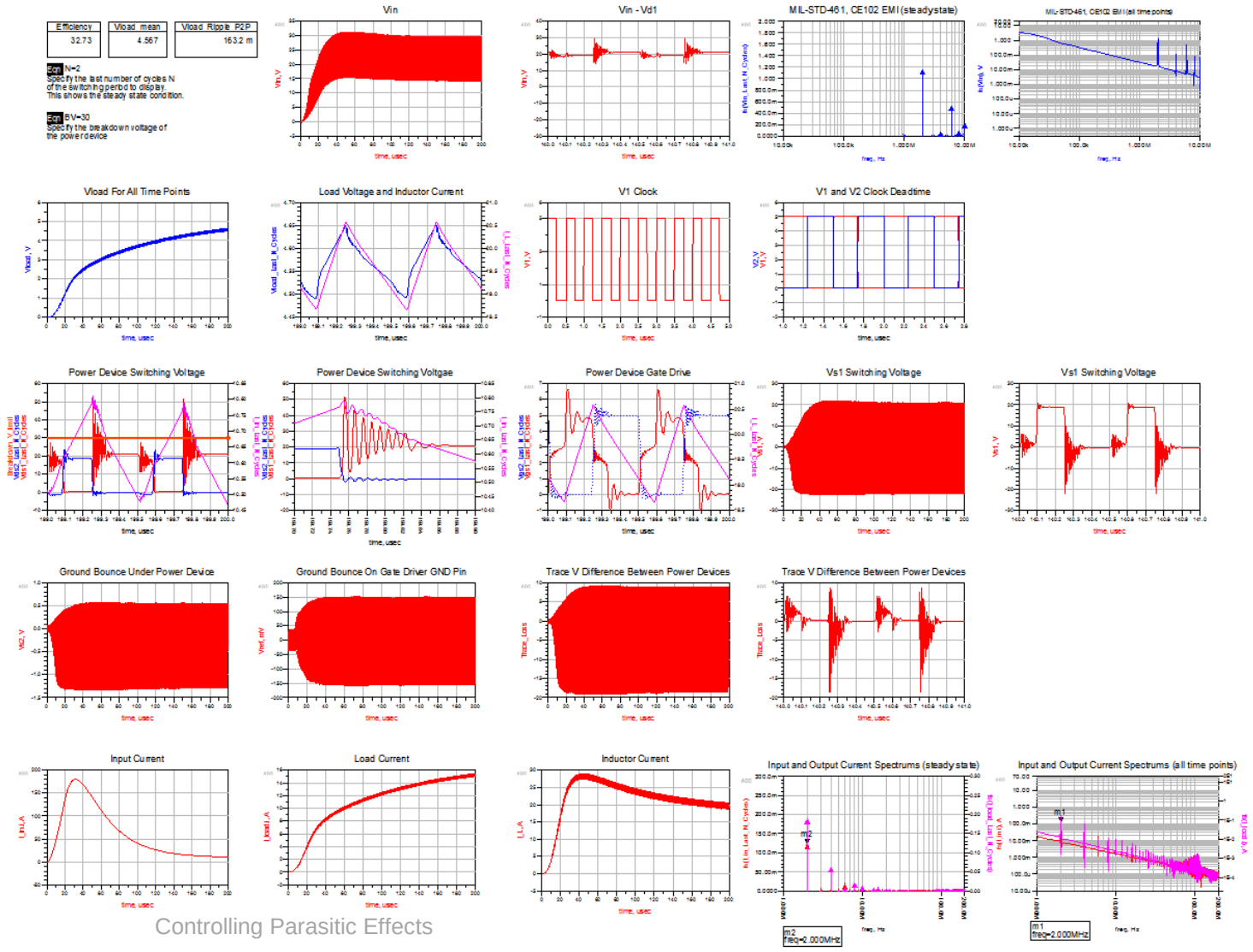


Post Processing in ADS

DATA DISPLAY IS A POWERFUL TOOL

Multiple measurements can be conveniently displayed at once.

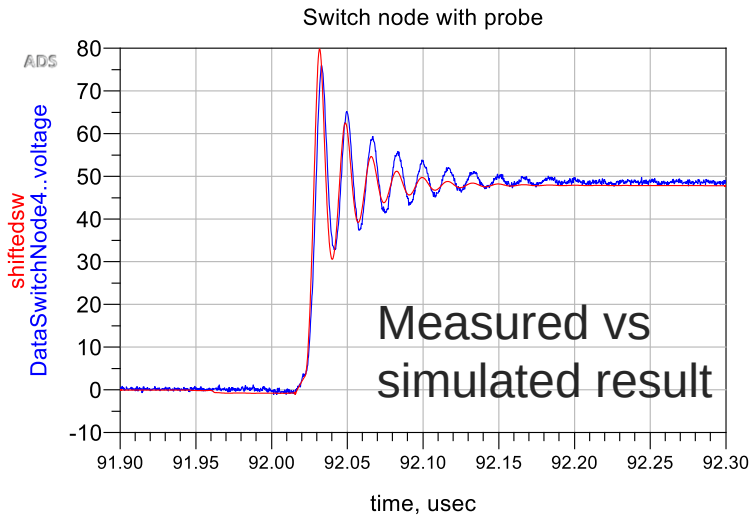
This can include: switching waveforms, ground bounce, EMI, di/dt trace drop etc.

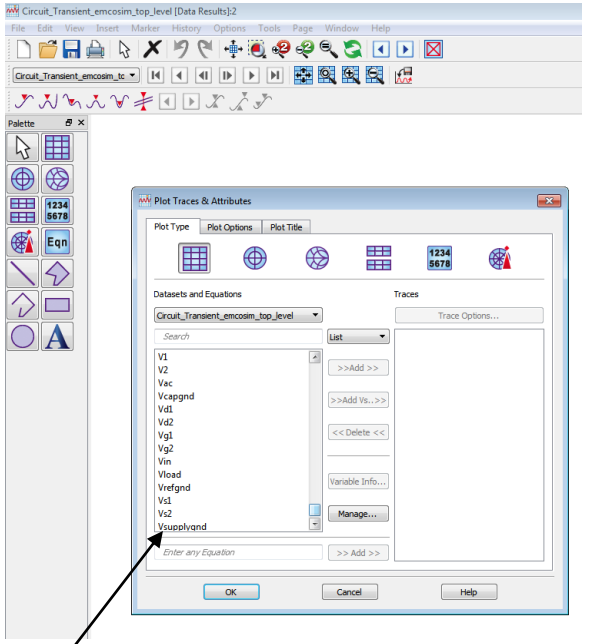


Post Processing Flexibility

CUSTOM MEASUREMENTS

- ADS provides flexibility to measure just about anything
  - Embedded measurements
  - Individual measurement of layout probe points
  - Custom scripted measurements
  - Measured vs simulated results



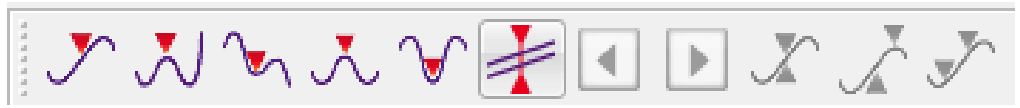



```
Eqn Tstart_Last_N_Cycles=max(time)-N/Clock_freq[0]
Eqn Tstart_index=find_index(time,Tstart_Last_N_Cycles)
Eqn Tstop_index=sweep_size(time)-1
Eqn Vload_Last_N_Cycles=Vload[Tstart_index::Tstop_index]
Eqn Vload_Last_N_Cycles_interp=interp(Vload_Last_N_Cycles)
Eqn Vload_Ripple_P2P=max(Vload_Last_N_Cycles)-min(Vload_Last_N_Cycles)
Eqn Vload_mean=mean(Vload_Last_N_Cycles)
Eqn I_load_Last_N_Cycles=I_load.i[Tstart_index::Tstop_index]
Eqn I_load_Last_N_Cycles_interp=interp(I_load_Last_N_Cycles)
Eqn Pload_Last_N_Cycles=mean(Vload_Last_N_Cycles_interp*I_load_Last_N_Cycles_interp)
Eqn Trace_Loss=Vs1-Vd2
Eqn Vgs1_Last_N_Cycles=Vg1[Tstart_index::Tstop_index]-Vs1[Tstart_index::Tstop_index]
Eqn Vgs2_Last_N_Cycles=Vg2[Tstart_index::Tstop_index]-Vs2[Tstart_index::Tstop_index]
Eqn L_Last_N_Cycles=L1.R7.i[Tstart_index::Tstop_index]
Eqn Vds1_Last_N_Cycles=Vin[Tstart_index::Tstop_index]-Vs1[Tstart_index::Tstop_index]
Eqn Vds2_Last_N_Cycles=Vd2[Tstart_index::Tstop_index]-Vs2[Tstart_index::Tstop_index]
Eqn L=R7.i
Eqn I_in_Last_N_Cycles=I_in.i[Tstart_index::Tstop_index]
Eqn I_in_Last_N_Cycles_interp=interp(I_in_Last_N_Cycles)
Eqn Vin_Last_N_Cycles=Vin[Tstart_index::Tstop_index]
Eqn Vin_Last_N_Cycles_interp=interp(Vin_Last_N_Cycles)
Eqn Pin_Last_N_Cycles=mean(Vin_Last_N_Cycles_interp*I_in_Last_N_Cycles_interp)

Eqn Efficiency=100*Pload_Last_N_Cycles/Pin_Last_N_Cycles

The interp() function with default parameters is used on several waveforms.
This gives data that is uniformly-spaced in the time domain, which is necessary
for obtaining an accurate mean calculation when the waveform is "spikey."
```

Custom scripted measurements

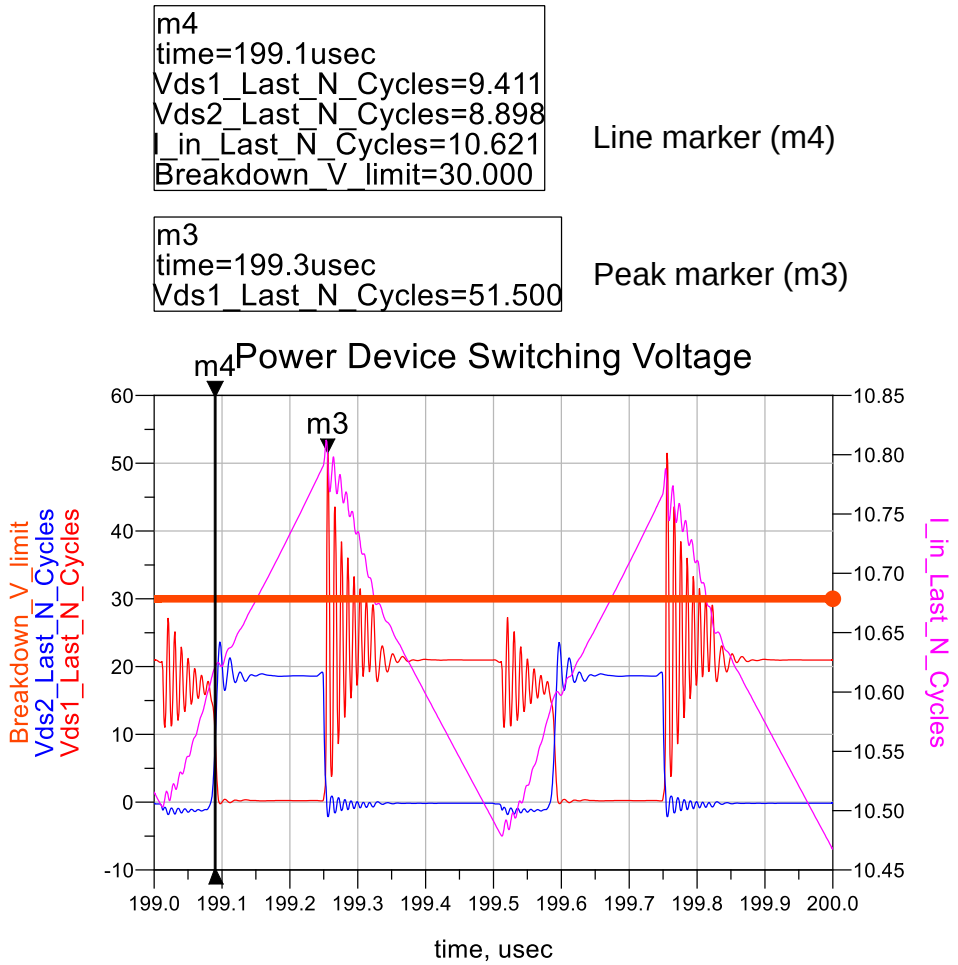
Measurement Precision

USING DATA DISPLAY MARKERS



Marker palette

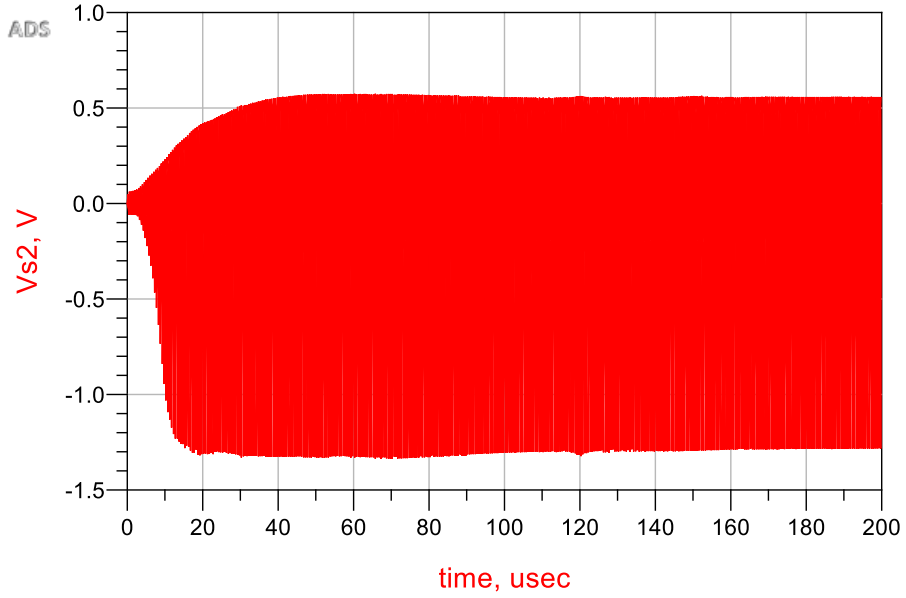
- Markers make it easier to measure data
- Markers are inserted to measure points of interest
- Markers can be used to measure the period of ringing, rise times, or differential timing



Troubleshooting Using ADS

GROUND BOUNCE EXAMPLES

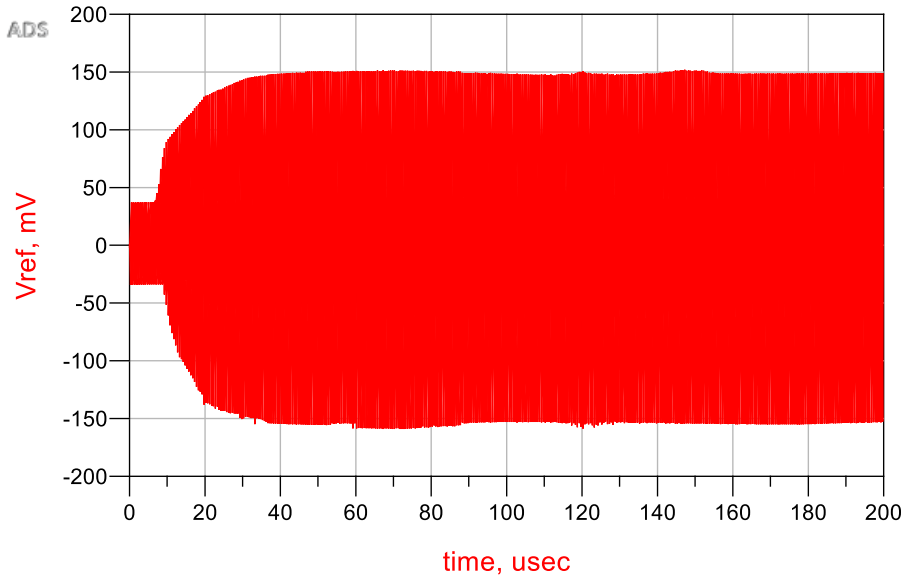
Ground Bounce Under Power Device



Ground bounce reduces converter efficiency, produces common mode noise, and degrades noise immunity.

This performance is good

Ground Bounce On Gate Driver GND Pin

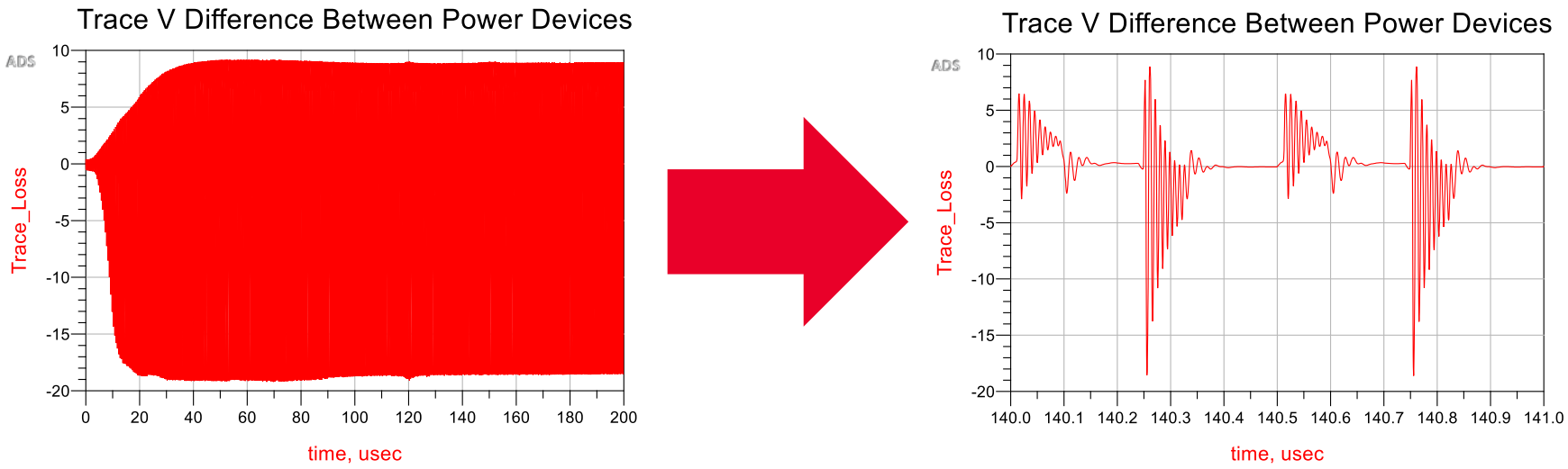


Ground bounce near a voltage reference or gate driver can degrade noise performance.

This performance is good

Troubleshooting Using ADS

dI/dT EXAMPLE – VOLTAGE DROP ACROSS A TRACE

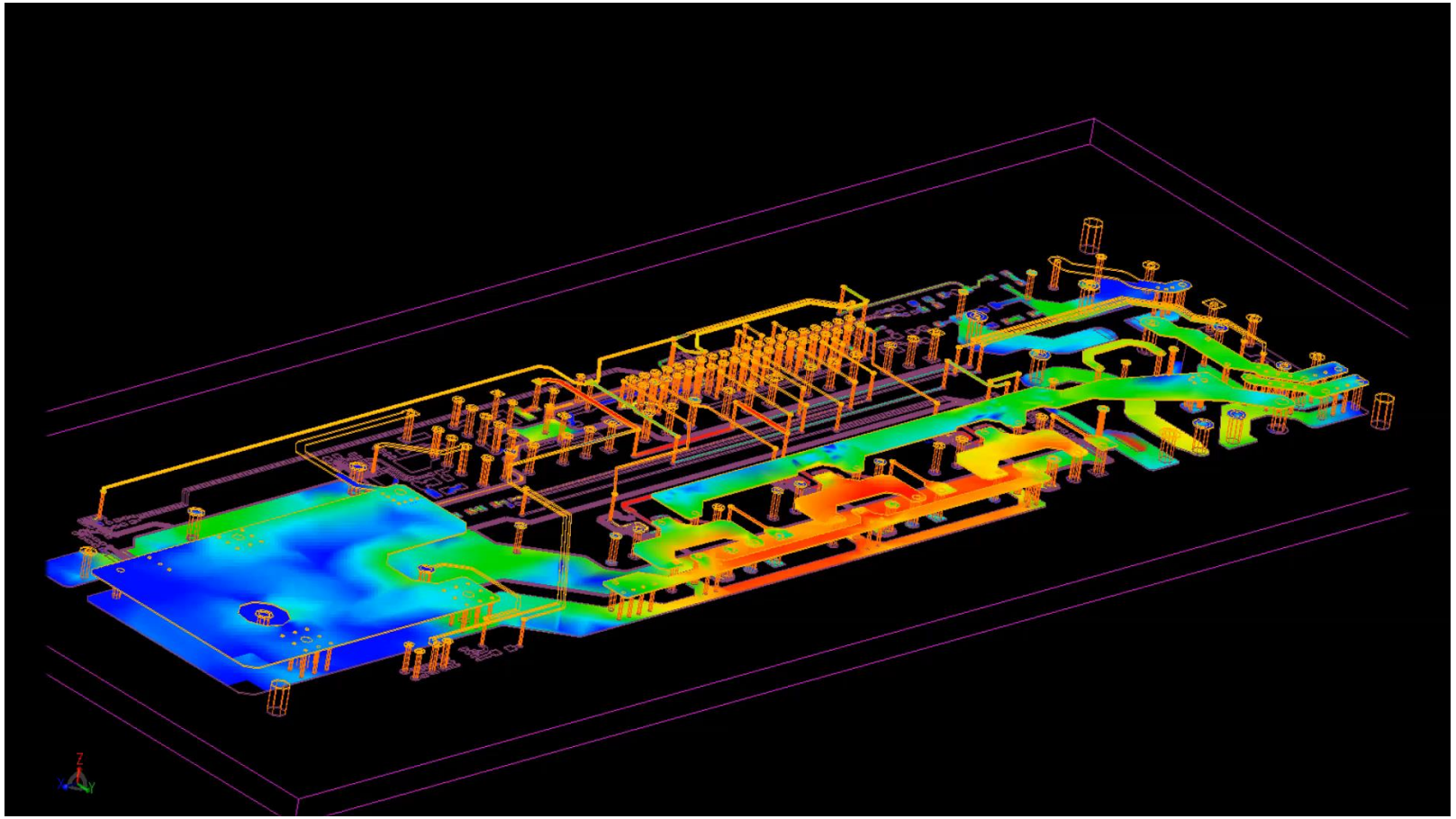


Probes placed along traces can be subtracted from each other to gain insights

- Where high current loops drive L di/dt effects
- Impact on switching efficiency

Troubleshooting Using ADS

EM EXCITATION EXAMPLE



- EM excitation provides current or voltage density to troubleshoot “hot spots”
- Visualization can be manipulated to provide different views

Conclusions

- Parasitic effects degrade performance and can cause failure
  - All physical implementations include parasitics and their impact may not be seen with a schematic-only simulation
    - Spiking, noise, ringing, oscillations, false triggering, etc.
- Every ground point on a physical design is different!
    - Ground differences reduces noise immunity - a reliability concern
- Modern EDA tools and high speed design techniques can be used to verify, troubleshoot, and optimize a design