IBIS AMI Modeling Solution

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Application Engineer/ Keysight Technologies

Agenda

- **WHY we need IBIS AMI?**
- WHAT is IBIS AMI?
- HOW to model IBIS AMI?
- Examples
- Summary

WHY we need IBIS AMI?

HSD Design Challenge

- So many standards are existing…
  - PCIe gen3/4, USB3.2, SAS, SATA, HDMI 2.1, Display Port and 100GbE PAM4…
  - DDR5 equalization
- Signal verification at RX input is not sufficient
  - RX input signal is improved by CTLE/DFE and CDR
- Data Rate is increasing, over10Gpbs is common even in consumer products
  - Xtalk , VIA design …

→ **Simulation is the best way**

→ **Model is needed**

WHY we need IBIS AMI?

Modeling Challenge

- Chip Vender
  - Quantity of products, updating rapidly
  - High cost and long period of hardware test board
  - **High requirements** for modeling engineer: need knowledge of circuit design, signal processing, signal integrity as well as scripting
  - Need to guarantee accuracy of each model
  - Vendors with **NO** experience in AMI modeling are spending 6-12 months to come up with **first**-generation models

- Chip User
  - **Higher design difficulty** requires HSD engineer to test channel performance with consideration of real chip behavior during design flow
  - Have to wait a **LONG** time before accurate AMI models are released

WHY we need IBIS AMI?

SerDes Models

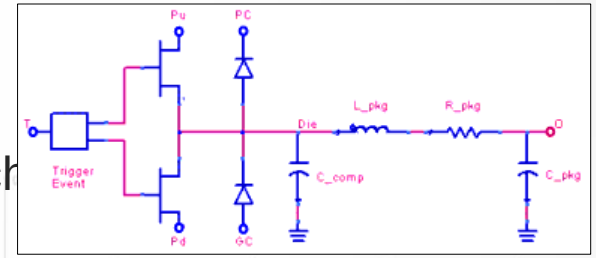
- Traditional Models
  - SPICE Model：include transistor level structure and specific processing tech
    - Include too much valuable info
    - slow simulation speed, especially for increasing complexity
  - IBIS Model：Define V-I and V-t curve of TX/RX
    - Cannot include complex equalization algorithm

IBIS AMI Model

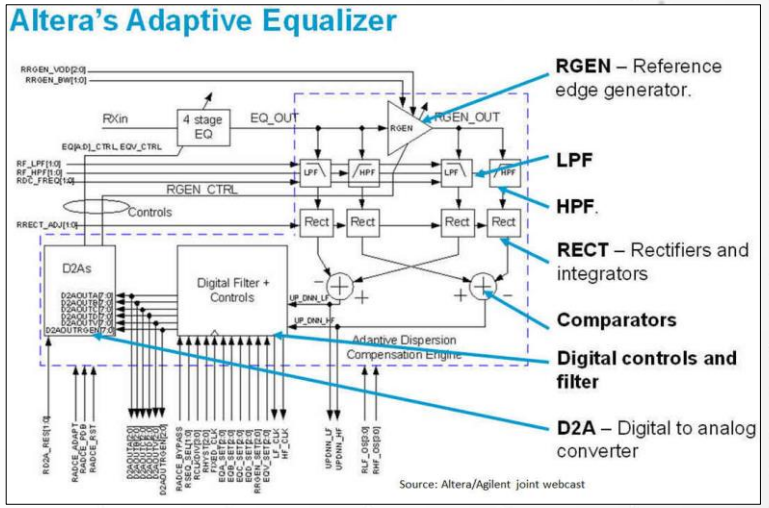
Defined since IBIS 5.0

- Note: IBIS 开放论坛制定IBIS相关的协议标准
- http://ibis.org/

Sub-gigabit/s yesterday



Multigigabit/s today



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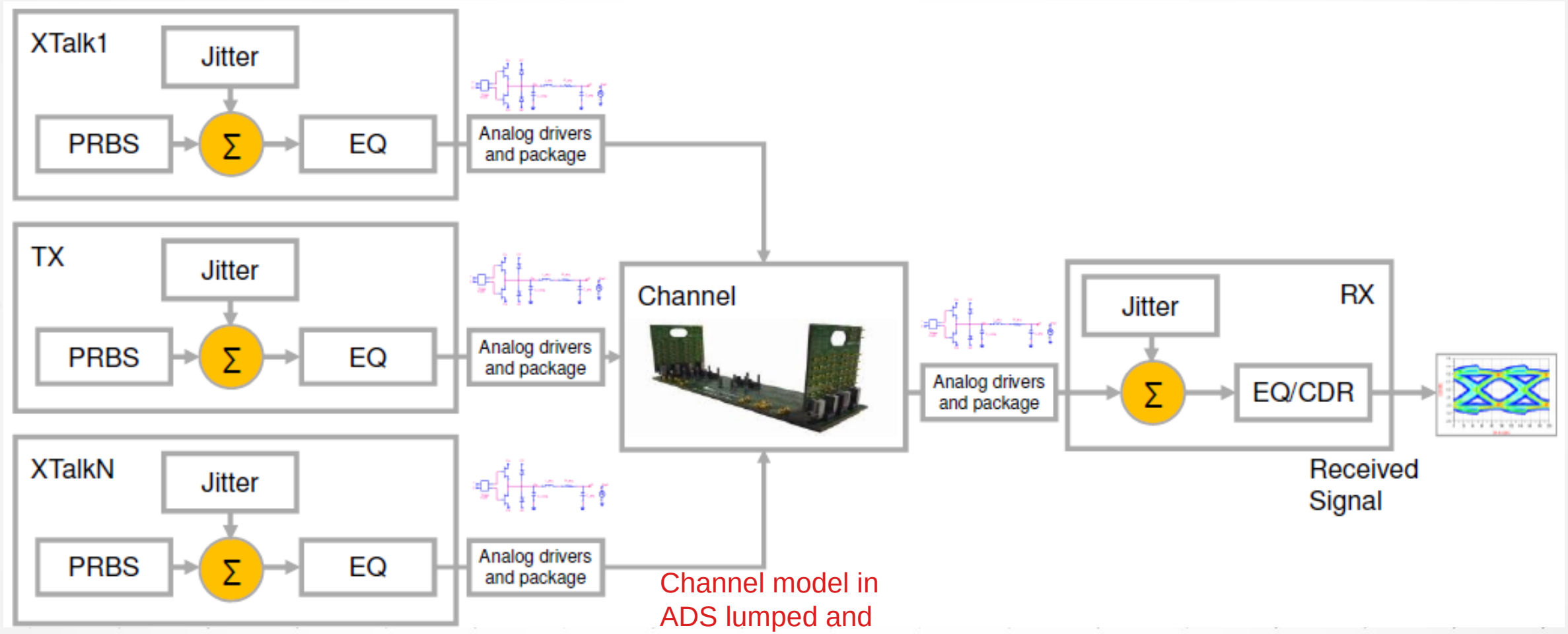
WHAT is IBIS AMI?



Tx *.ami and *.dll files

*.ibs files

Channel model in ADS lumped and distributed components

*.ibs files

Rx *.ami and *.dll files

WHAT is IBIS AMI Model?

- **.ibs** file：a model for digital buffer devices including Model, Pin, Package (Pin Parasitic), EBD, etc.. ：
  - Define **Tx** behavior except complex equalization by : Output voltage, Resistor, Switching Edge, Parasitic…
  - Define **Rx** behavior except complex equalization by : Input Resistor, Parasitic…

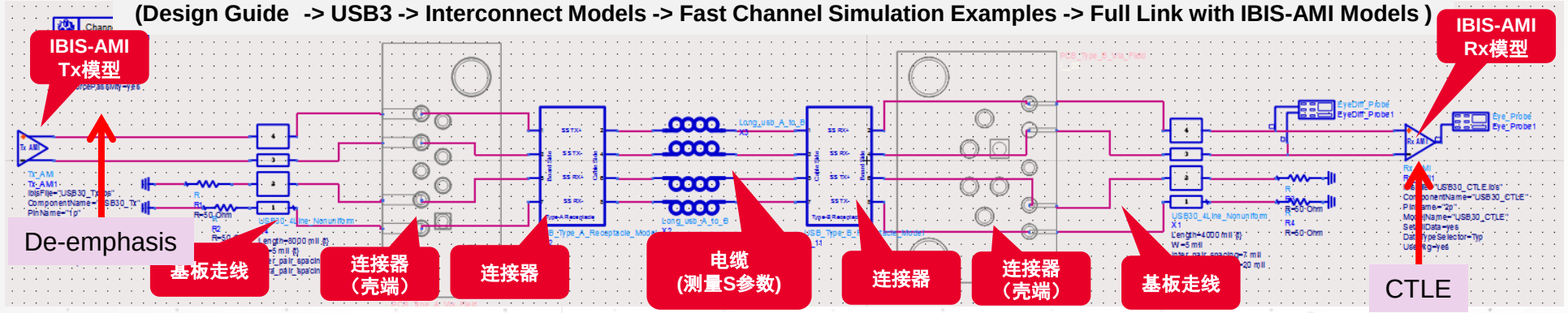
- **.ami** file：
  - [Reserved_Parameters]
    - Init_Returns_Impluse
    - GetWave_Exists
    - Tx_Jitter, Rx_Clock_PDF, etc.
  - [Model_Specific] to pass editable parameters (e.g. for EQ) to EDA tool

- **.dll /so** file (Windows/Linux)：Complied algorithmic file

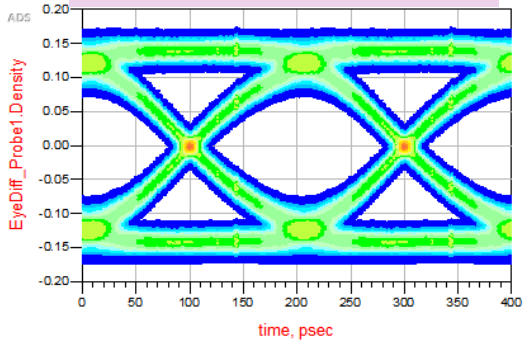
IBIS AMI Simulation Example

ADS USB3.0通道仿真

(Design Guide -> USB3 -> Interconnect Models -> Fast Channel Simulation Examples -> Full Link with IBIS-AMI Models)

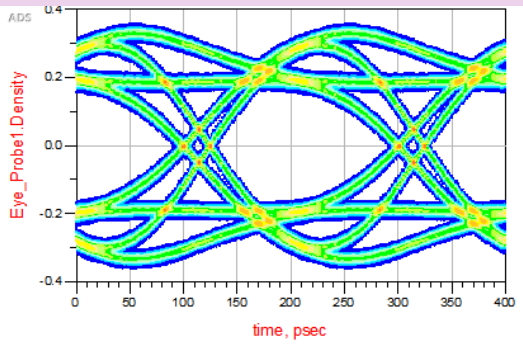


RX CTLE应用前(RX输入)



measurement	...iff_Probe1.Summary
Level1	0.120
Level0	-0.123
Height	0.131
Width	1.610E-10

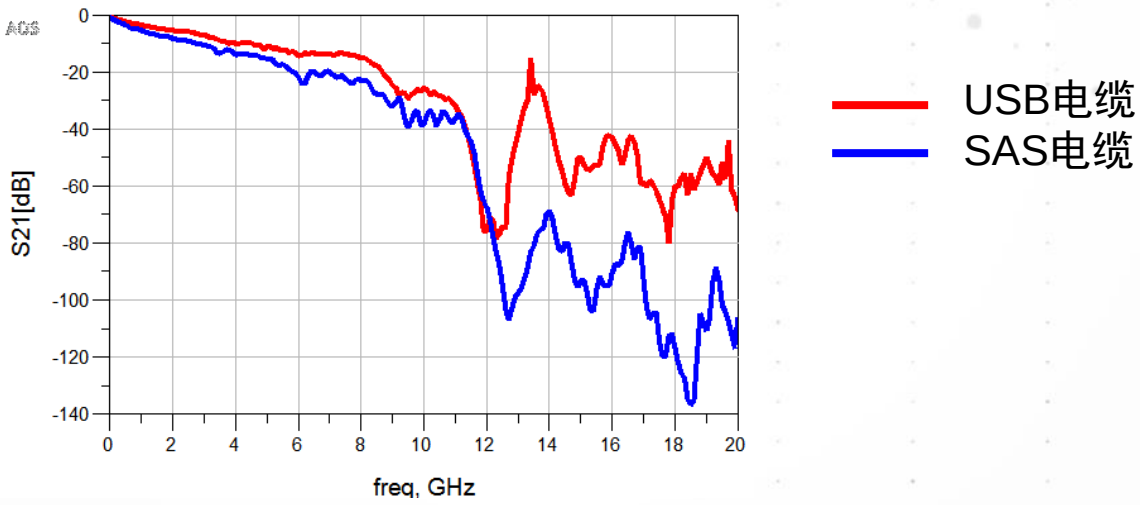
RX CTLE应用后(RX IBIS-AMI模型输出)



measurement	Eye_Probe1.Summary
Level1	0.239
Level0	-0.243
Height	0.276
Width	1.620E-10

Frequency response compensation of Channel

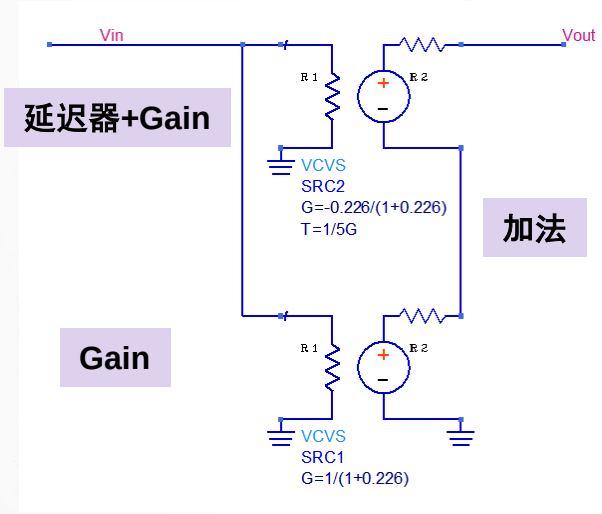
- Signal quality degrade by channel loss at high frequency region
- To compensate that, apply DeEmphasis in TX and CTLE in RX



TX Equalizer

De-Emphasis

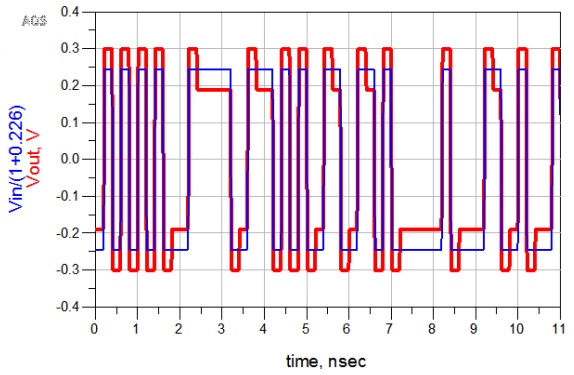
- Boost signal strength around high frequency range
- Can be modeled by delay + Gain

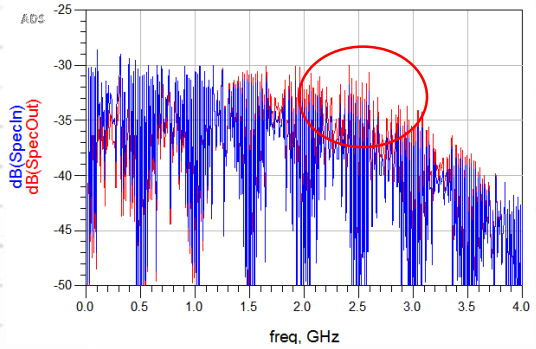


延迟器+Gain

加法

Gain





De-Emphasis后

De-Emphasis前

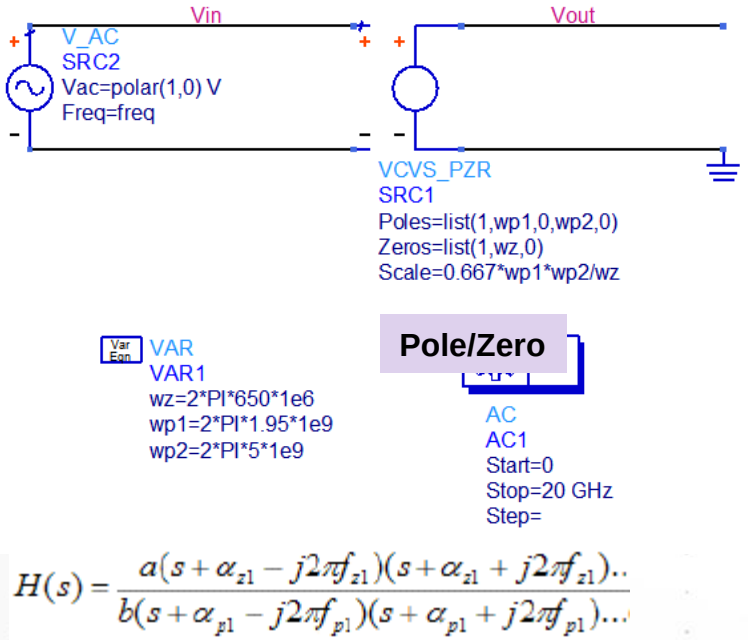
高频分量得到增强

RX Equalizer

CTLE

- CTLE(Continuous Time Linear Equalizer) is AMP with Analog Filter
- CTLE can be modeled by transfer function (Poles/Zeros)

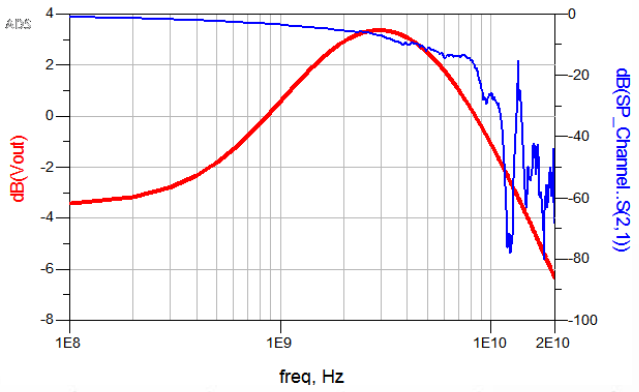
Design Guide -> USB3 -> Interconnect Models -> Receiver Equalizer -> CTLE Equalizer Simulation



$$H(s)=\frac{a(s+\alpha_{z1}-j2\pi f_{z1})(s+\alpha_{z1}+j2\pi f_{z1})..}{b(s+\alpha_{p1}-j2\pi f_{p1})(s+\alpha_{p1}+j2\pi f_{p1})...}$$

$$\text{Poles}=\text{list}(b,\alpha_{p1},f_{p1},\ldots,\alpha_{pm},f_{pm})$$

$$\text{Zeros}=\text{list}(a,\alpha_{z1},f_{z1},\ldots,\alpha_{zn},f_{zn})$$



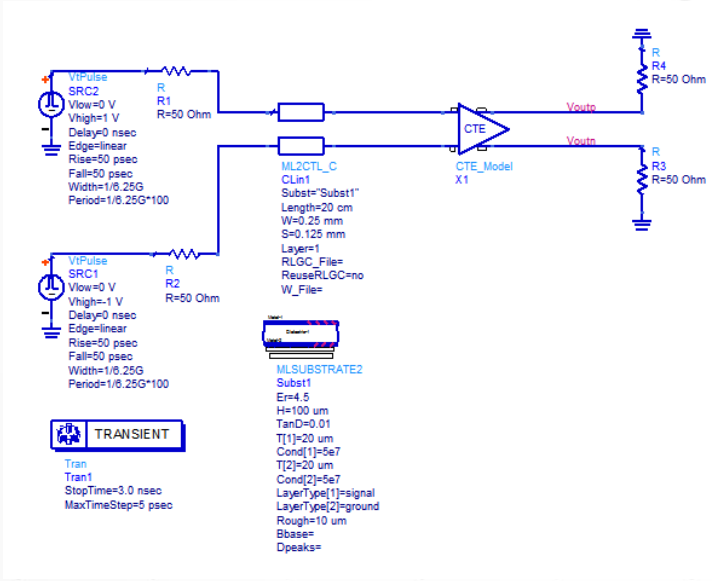
CTLE传递函数
USB电缆频率特性

高频分量得到增强

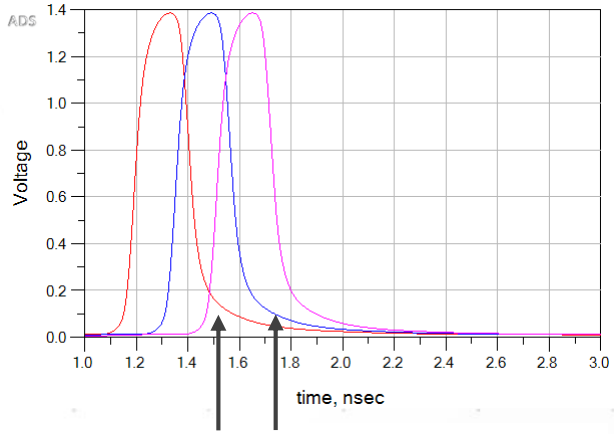
Remove ISI

DFE

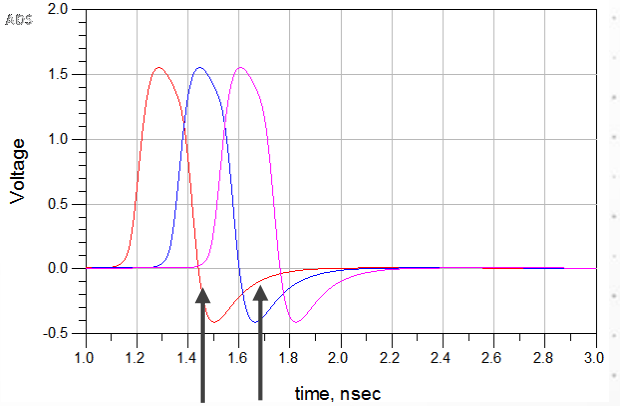
- DFE remove ISIs which are still remaining in output signal of CTLE



CTLE input

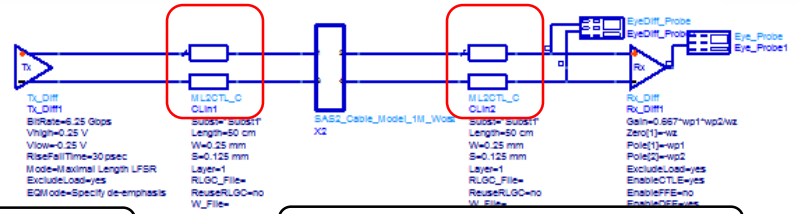


CTLE output



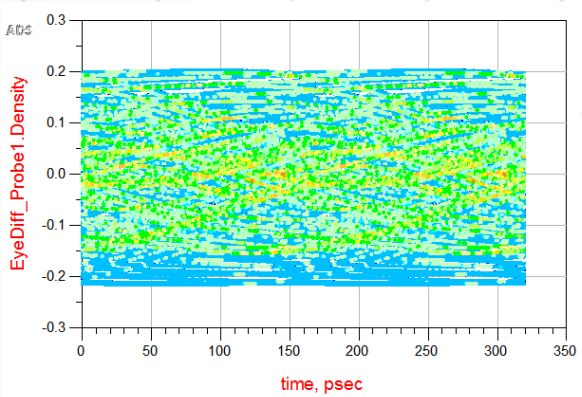
ADS TX/RX model

SIMULATION WITH CHANNEL



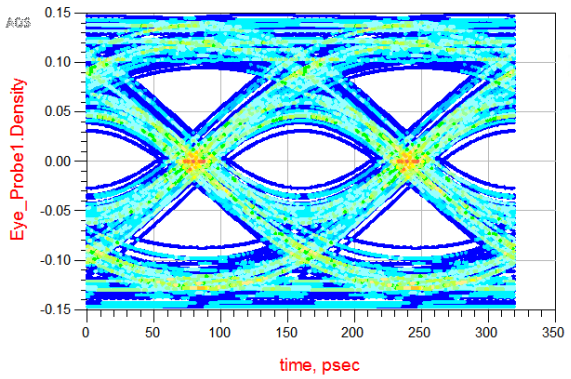
20cm -> 50cm

RX input



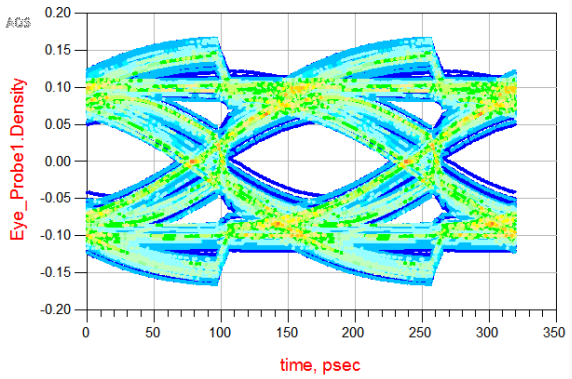
measurement	...Diff_Probe1.Summary
Level1	0.000
Level0	0.000
Height	0.000
Width	0.000

CTLE=ON/DFE=OFF



measurement	Eye_Probe1.Summary
Level1	0.090
Level0	-0.089
Height	0.052
Width	1.016E-10

CTLE=ON/DFE=ON



measurement	Eye_Probe1.Summary
Level1	0.089
Level0	-0.089
Height	0.082
Width	1.136E-10

Eye width is 10% improved

IBIS AMI Modeling Challenge

- Various Knowledge
  - Circuit Knowledge
  - High speed design simulation ability
  - Scripting ability
- Long development period
  - Period for the first time modeling requires 6~12 months
- High modeling accuracy
  - Repeated verification and testing are quired before model release

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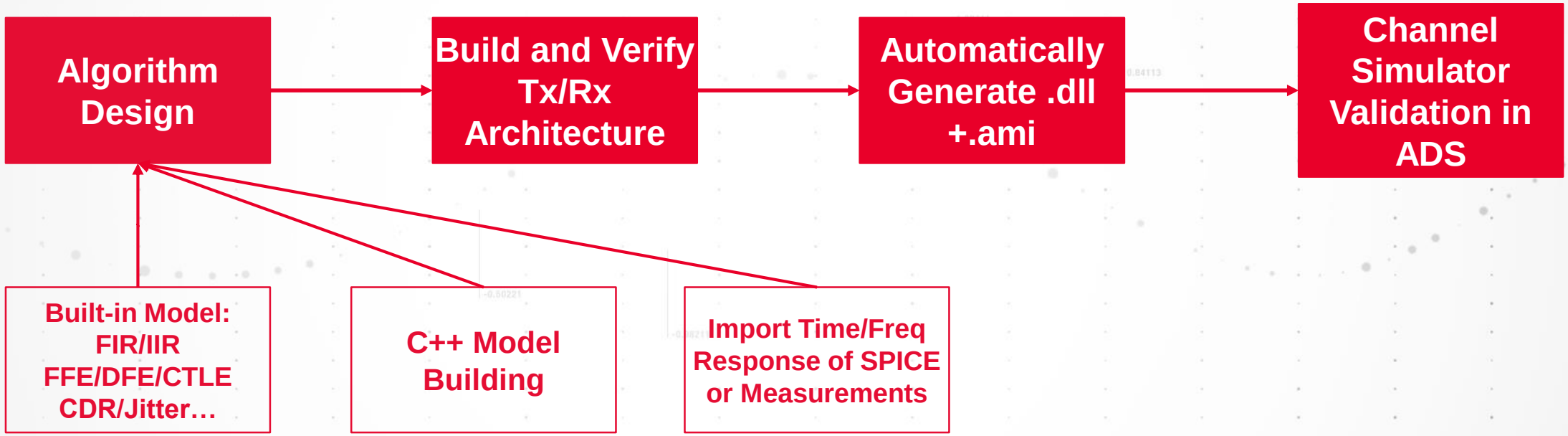
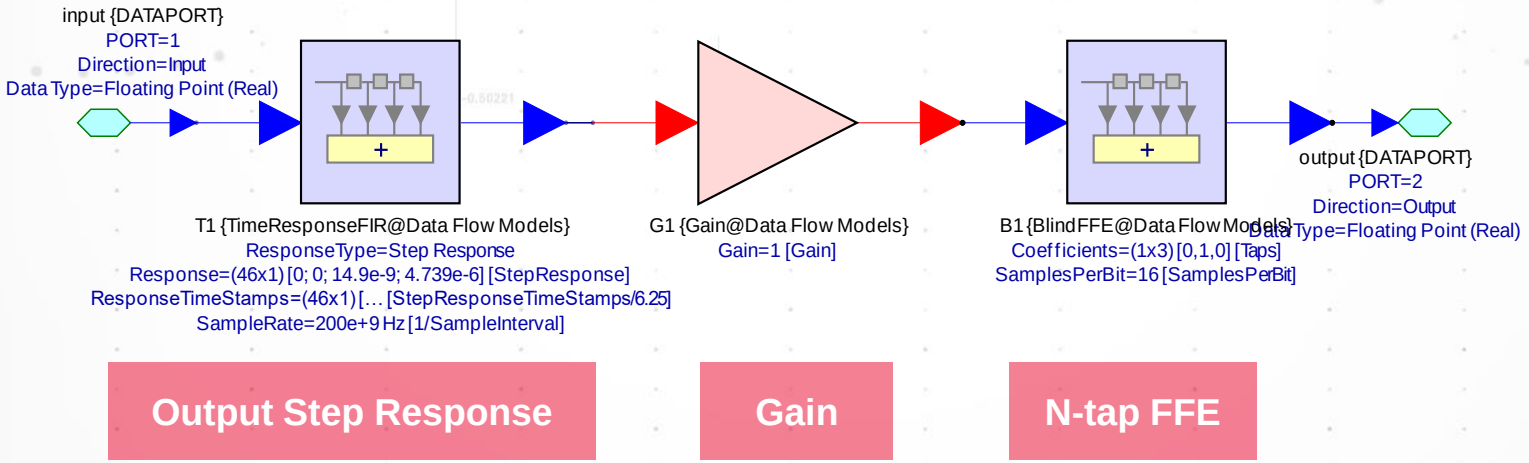
SystemVue IBIS AMI Modeling Flow



IBIS AMI Modeling Flow

Transmitter - Architecture

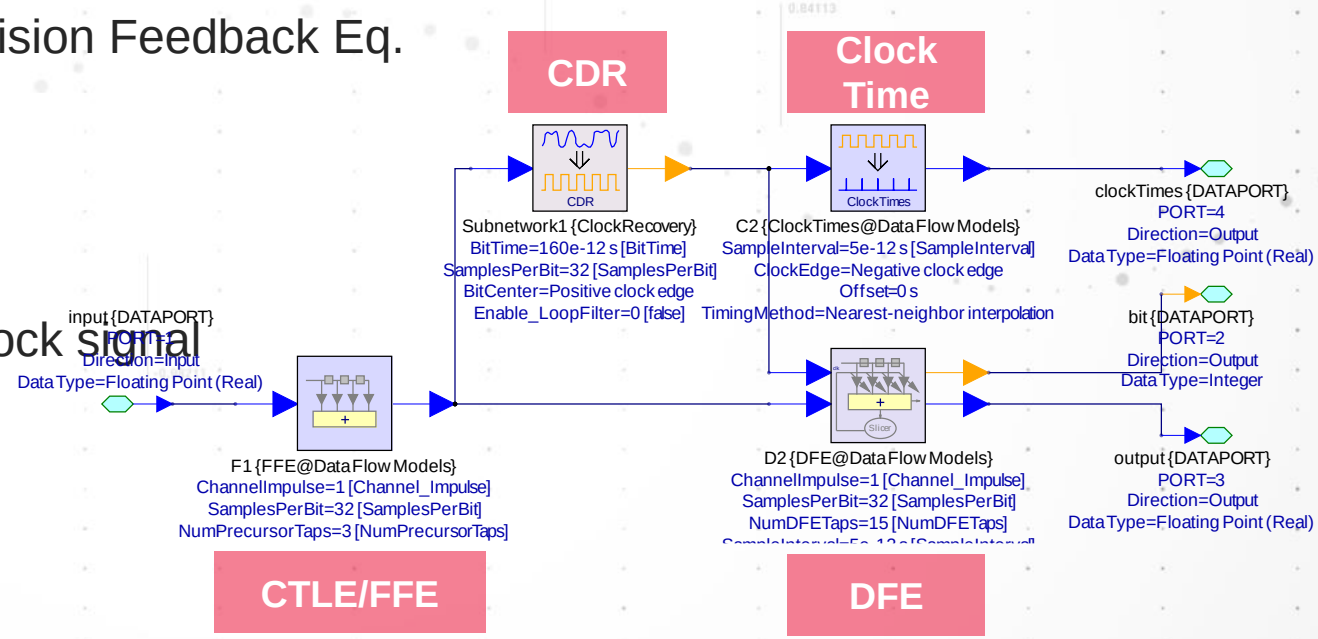
- **Step 1-1**. Transmitter:
  - Output Step/Impulse Response (TimeResponseFIR)
  - Gain (Gain)
  - Equalizer（FFE/CLTE）(BlindFFE/SDomainIIR/…)
    - Can be complex and customized equalization blocks or Import response of equalizer instead



IBIS AMI Modeling Flow

Receiver - Architecture

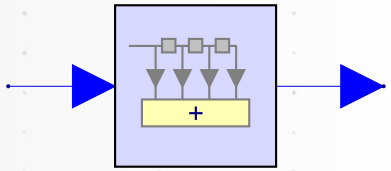
- **Step 1-2**. Receiver:
  - CTLE (SDomainIIR): Continuous Time Linear Equalizer of or FFE (FFE) Feed Forward Equalizer
  - DFE (BlindDFE or Adaptive DFE): Decision Feedback Eq.
  - CDR (CDR): Clock Data Recovery
    - Phase Detector, PLL, VCO
  - Clock Time : Extract clock time from clock signal



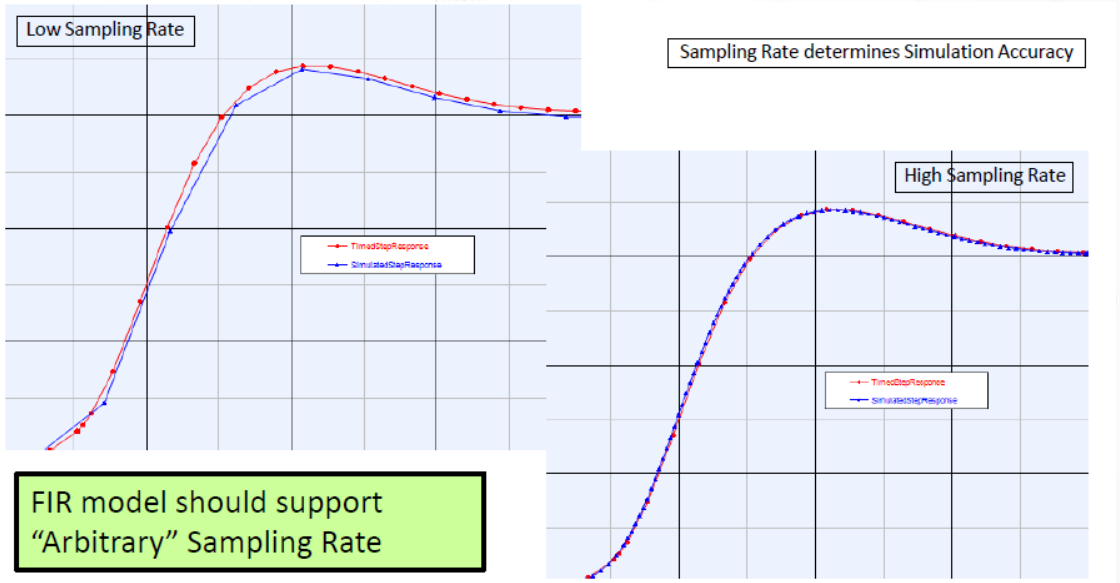
IBIS AMI Modeling Flow

Optional: Simulated or Measured DATA

- **Step 2-1**. Time/Freq. Response of circuit or equalizer: Import measurement or SPICE data
  - Use TimeResponseFIR Model to import HSPICE data or measurement data



T1 {TimeResponseFIR@Data Flow Models}
ResponseType=Step Response
Response=(46x1) [0; 0; 14.9e-9; 4.739e-6] [StepResponse]
ResponseTimeStamps=(46x1) [… [StepResponseTimeStamps/6.25]
SampleRate=200e+9 Hz [1/SampleInterval]

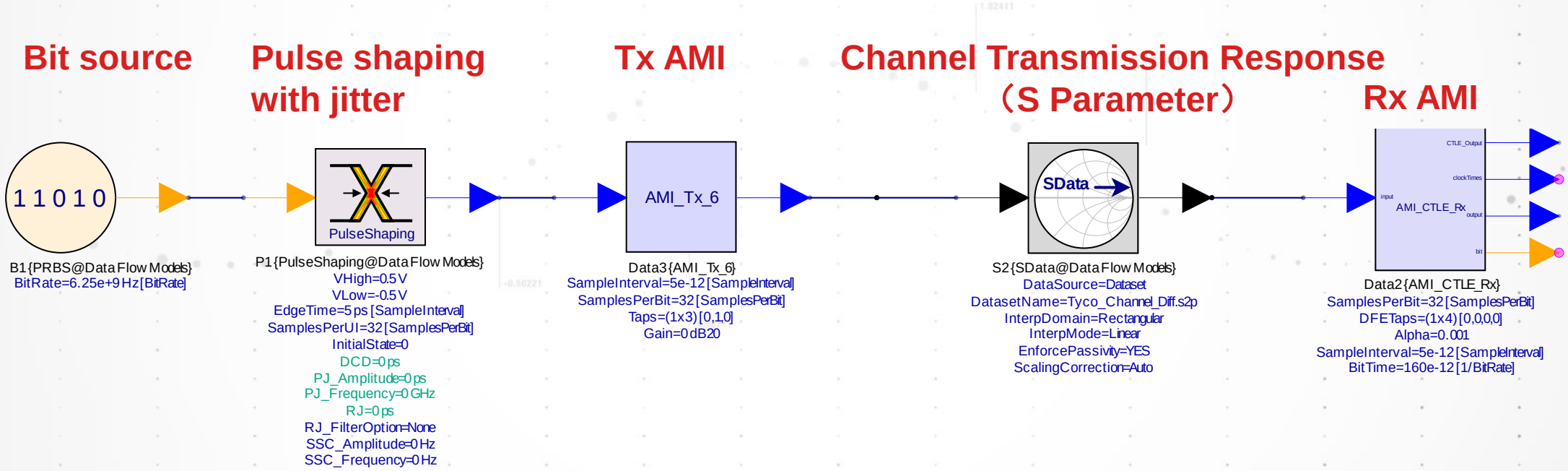


- **Step 2-2**. customized algorithm: import existing code
  - Challenges: Sometimes built-in model does not meet all IBIS AMI modeling requirement
  - Solution: User can import C++ code for modeling

IBIS AMI Modeling Flow

Algorithm Verification

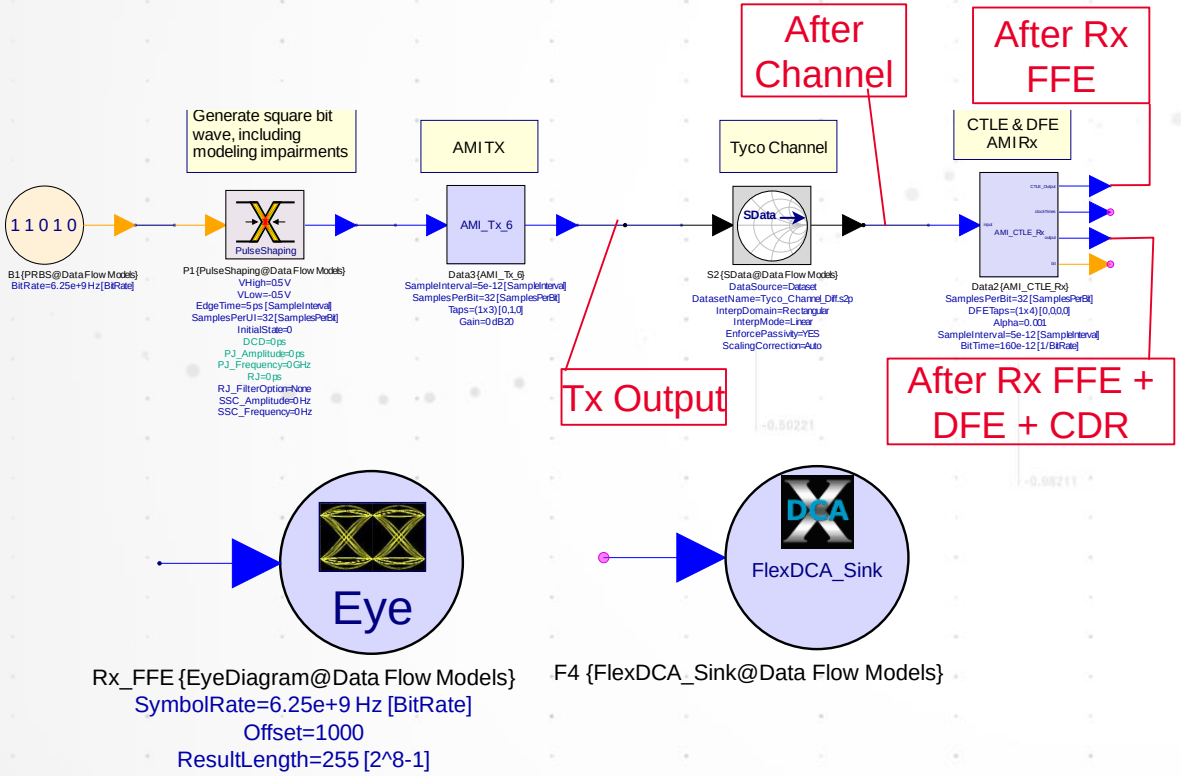
- **Step 3-1**. Verify Algorithm



IBIS AMI Modeling Flow

Algorithm Verification

- **Step 3-2**. Verify Algorithm: Use built-in model EyeDiagram or Keysight FlexDCA



IBIS AMI Modeling Flow

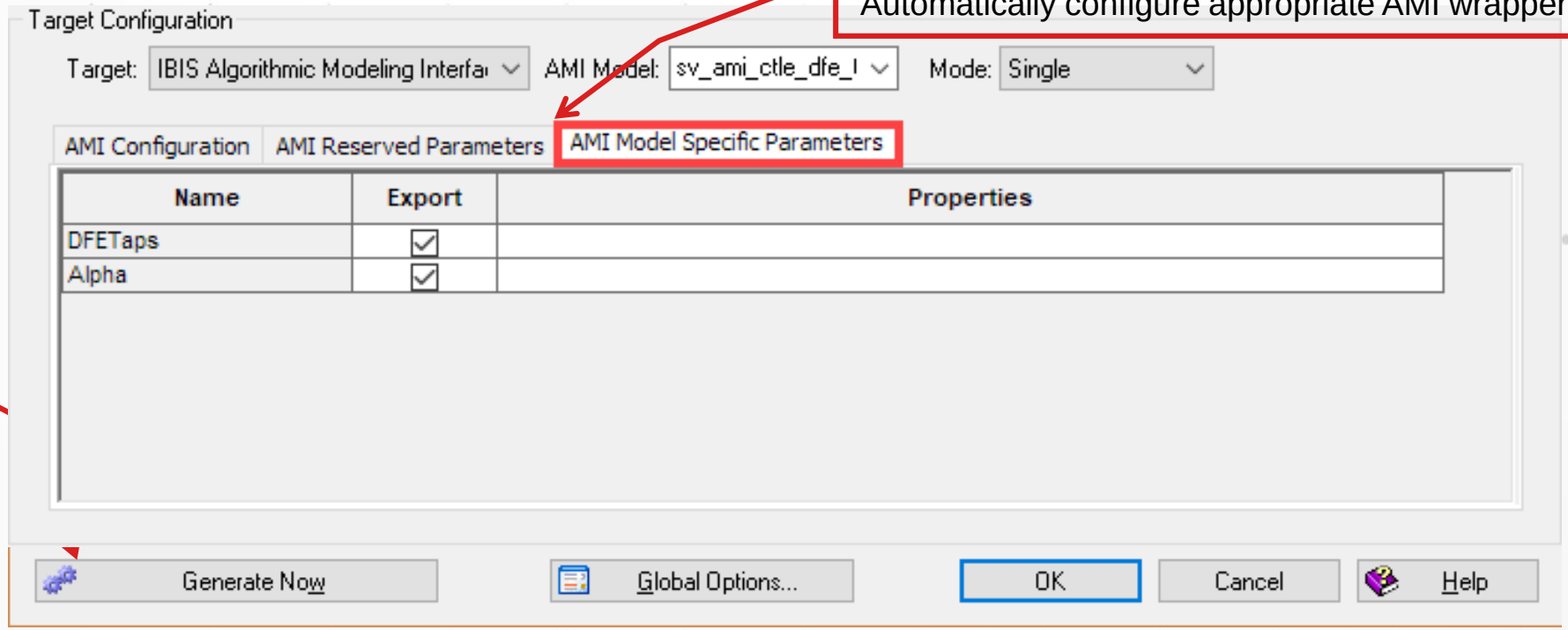
Custom Equalization – Code Generation

SystemVue

- **Step 4**.automatically generating code：（No need for manual compiling）

Define Reserved and Model Specific Parameters → Automatically configure appropriate AMI wrapper

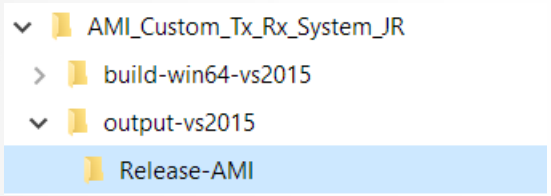
One-Click AMI Code Generation

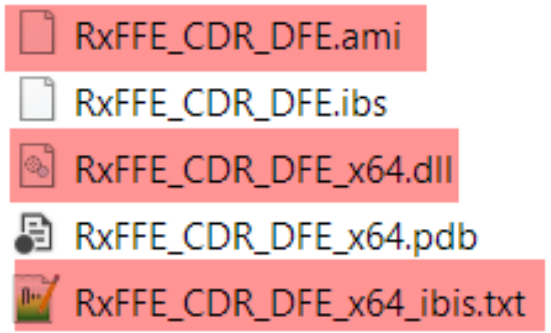


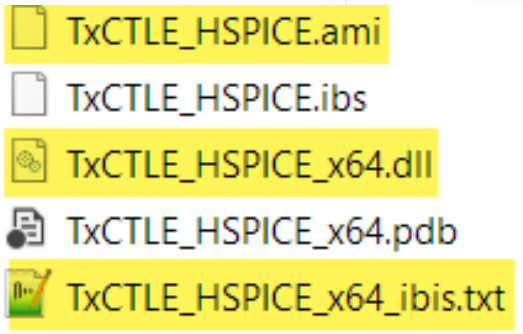
IBIS AMI Modeling Flow

Model Validation

- **Step 5**. Check IBIS AMI Model：Connect corresponding files for IBIS AMI model
  - Among generated files，**.ami** and **.dll** files work together with original .ibs
  - Key command lines are required to be extracted from **ibis.txt**： Find [Algorithmic Model] lines in ibis.txt files of Tx and Rx , copy the 'Executable …' line to the same position in original .ibs files。







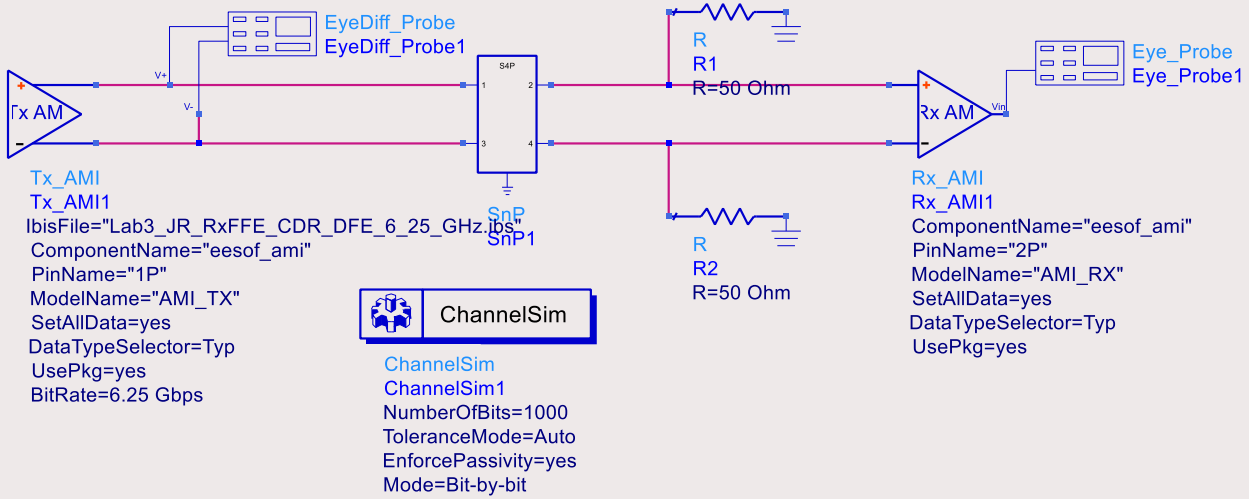

```
53  [Algorithmic Model]
54  Executable Windows_cl19.00.24215.1_64 TxCTLE_HSPICE_x64.dll TxCTLE_HSPICE.ami
55  [End Algorithmic Model]
96  [Algorithmic Model]
97  Executable Windows_cl19.00.24215.1_64 RxFFE_CDR_DFE_x64.dll RxFFE_CDR_DFE.ami
98  [End Algorithmic Model]
```

IBIS AMI Modeling Flow

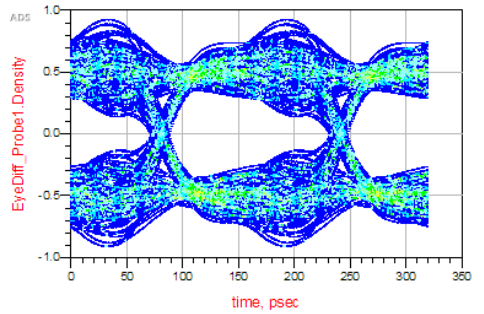
Model Validation

Advanced Design System

- **Step 6**. Verify IBIS AMI Model：Use ADS Channel Simulator to analyze channel performance through eye diagram or other measurements.

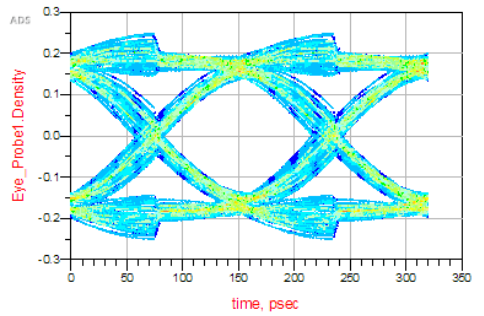


Tx

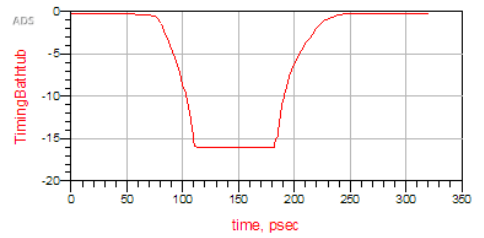


measurement	...Probe1.Summary
Level1	0.509
Level0	-0.509
Height	0.508
Width	1.480E-10

Rx



measurement	...be1.Summary
Level1	0.164
Level0	-0.164
Height	0.238
Width	1.320E-10



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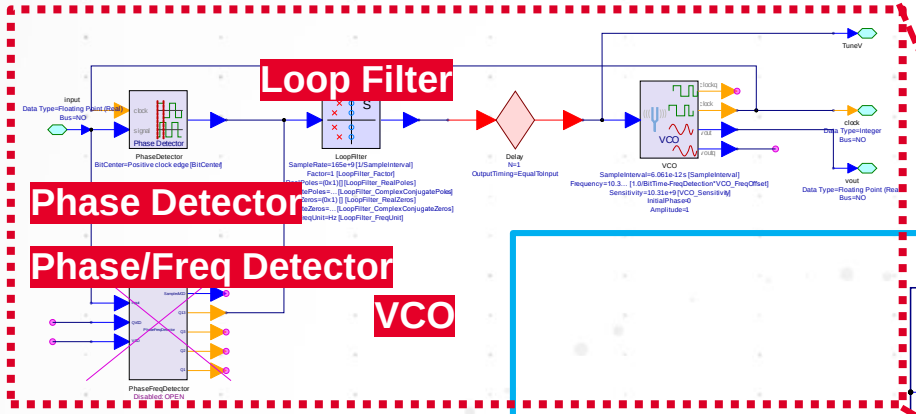
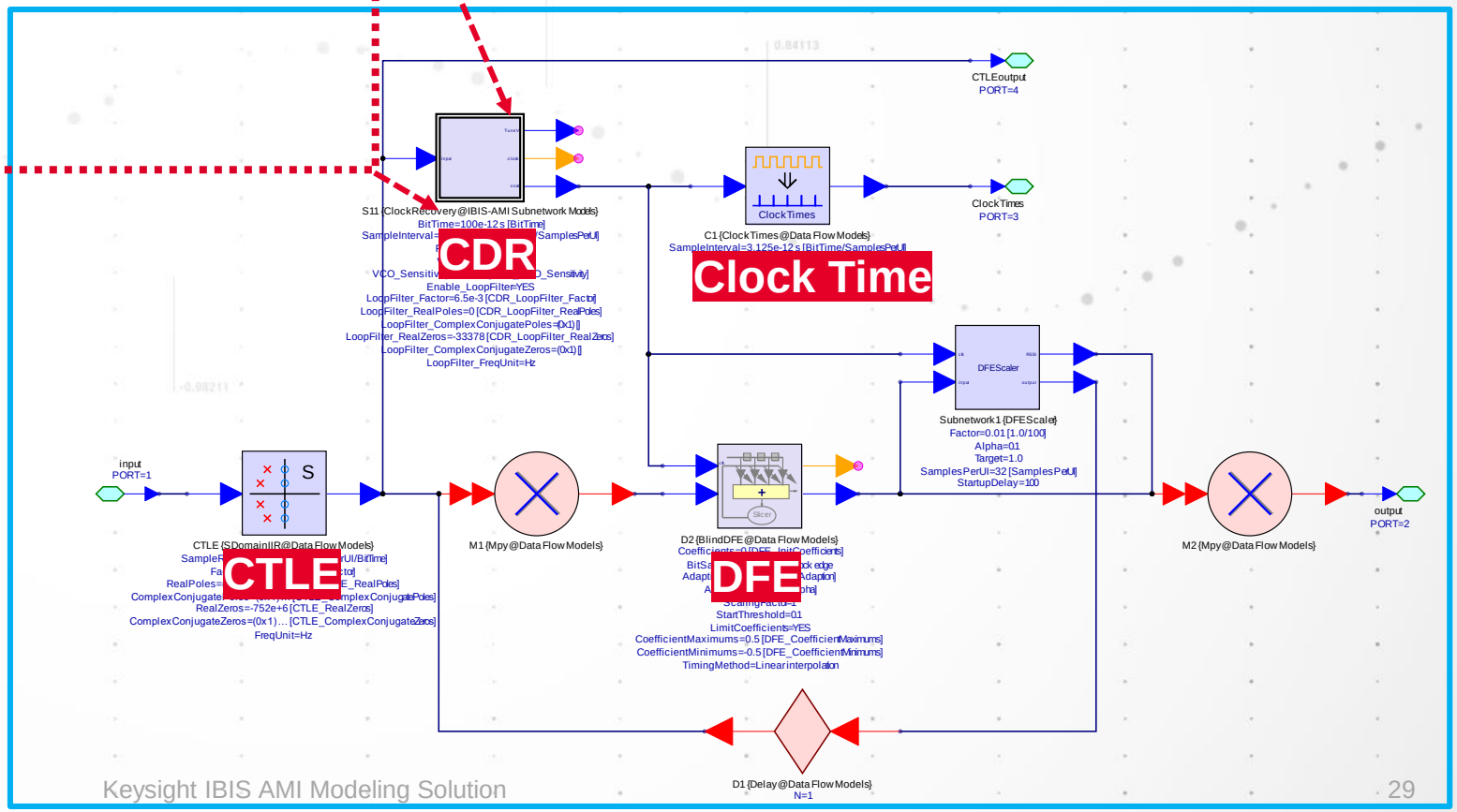
Example 1: USB 3.1

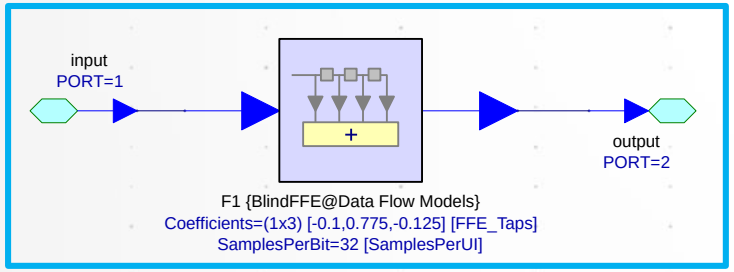
Transceiver of USB 3.1 Gen2, 10 Gbps



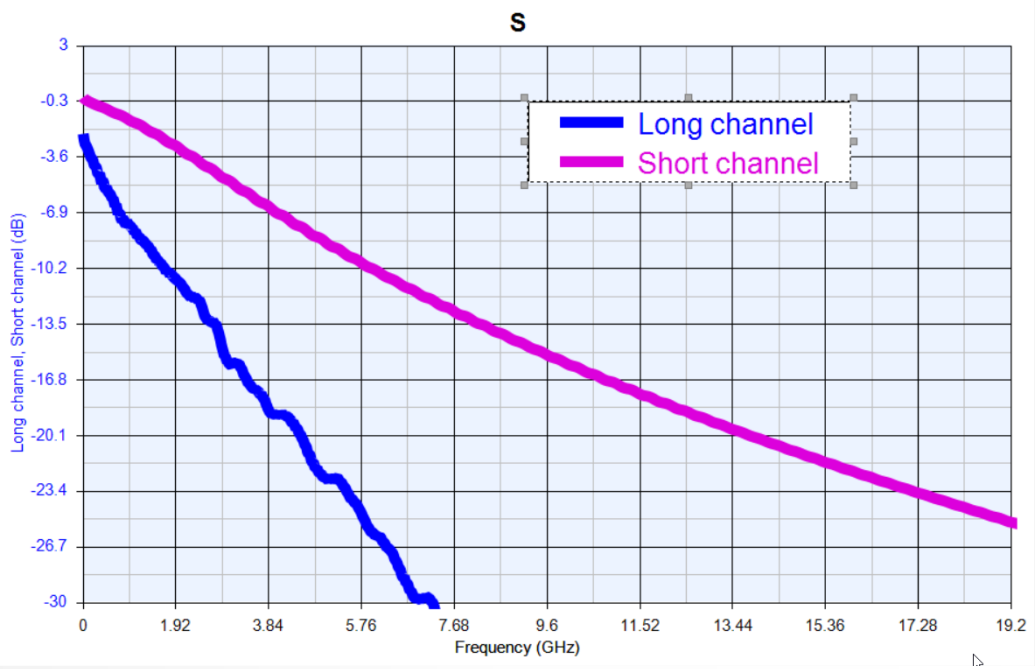
Receiver (CTLE + DFE + CDR)



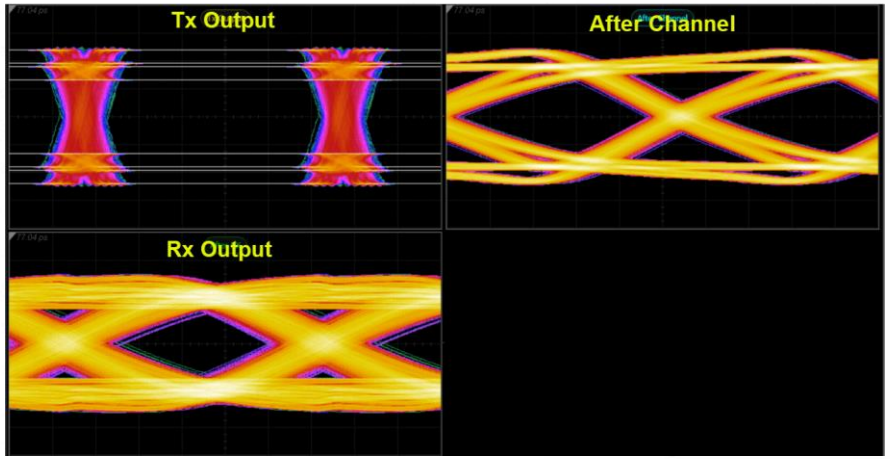
Transmitter (Feed Forward Eq)



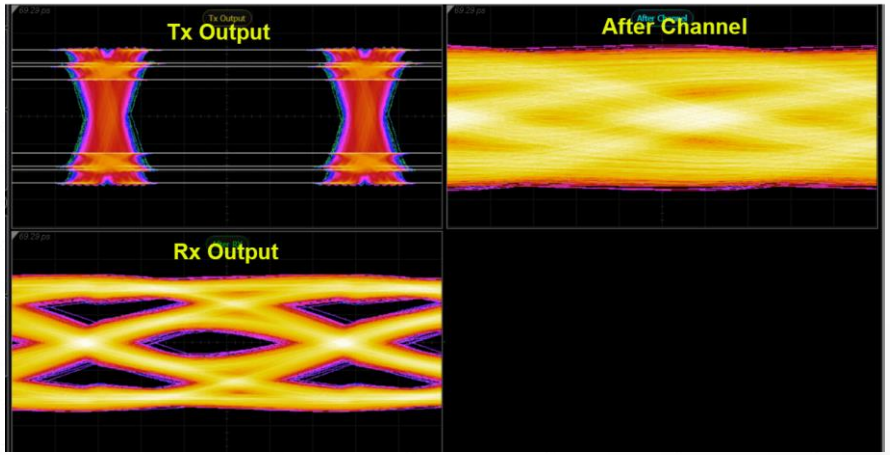
Example 1: USB 3.1



Short Channel



Long Channel



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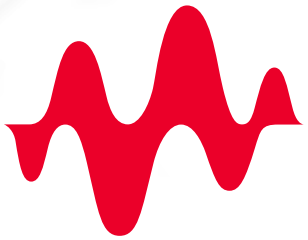
Summary

- IBIS-AMI model can remove barrier to simulation
  - Simulation with real TX signal
    - PCIe gen3/4, USB3.2, SAS, SATA, HDMI 2.1, Display Port and 100GbE PAM4
  - Equalized by CTLE/DFE in RX model
  - More accurate modeling by importing time/freq. response
  - To decide repeater use or not
- Channel Simulation by ADS provides an efficient chip-to-chip link simulation including real channel.

Appendix: Learning Resource

- ADS小秘訣 http://www.keysight.com/find/ads_tips
  - 新工程師必讀課程 - IBIS AMI 建模
    https://community.keysight.com/thread/36876



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Thank you