MIPI C-PHY
Solving Simulation Challenges

Application Engineer	***OCT 2019***
Nash TU	

MIPI Member Meeting North America #50

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Today's Typical C-PHY Simulation Challenges

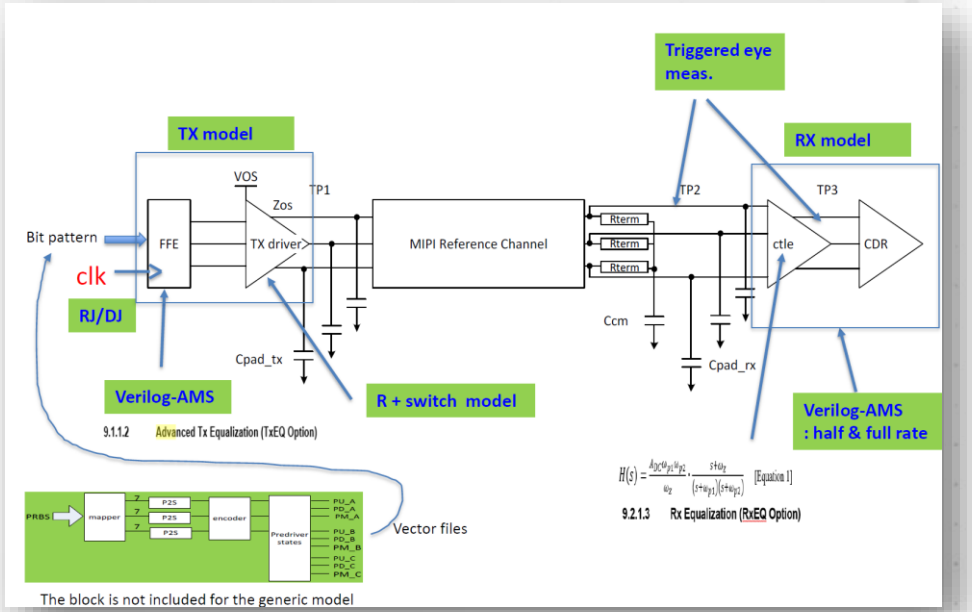
HIGHLIGHTS

- Complicated transmitter and receiver modeling process including equalizations
  - ➢ Need simple transmitter and receiver models
- No single platform solution but using multiple tools such as Verilog-A, meaning lots of customization required
  - ➢ Need just simple one platform solution without much customization
- Limited jitter analysis
  - ➢ Need full support of RJ, PJ and DCD
- SPICE-alike simulations result in long simulation time and limit number of bits that can be simulated
  - ➢ Need channel simulation technology for faster simulation with millions of bits
- Non-triggered eye plot
  - ➢ Need triggered eye plot to support MIPI C-PHY specification

Today's and New C-PHY Generic Model Architecture

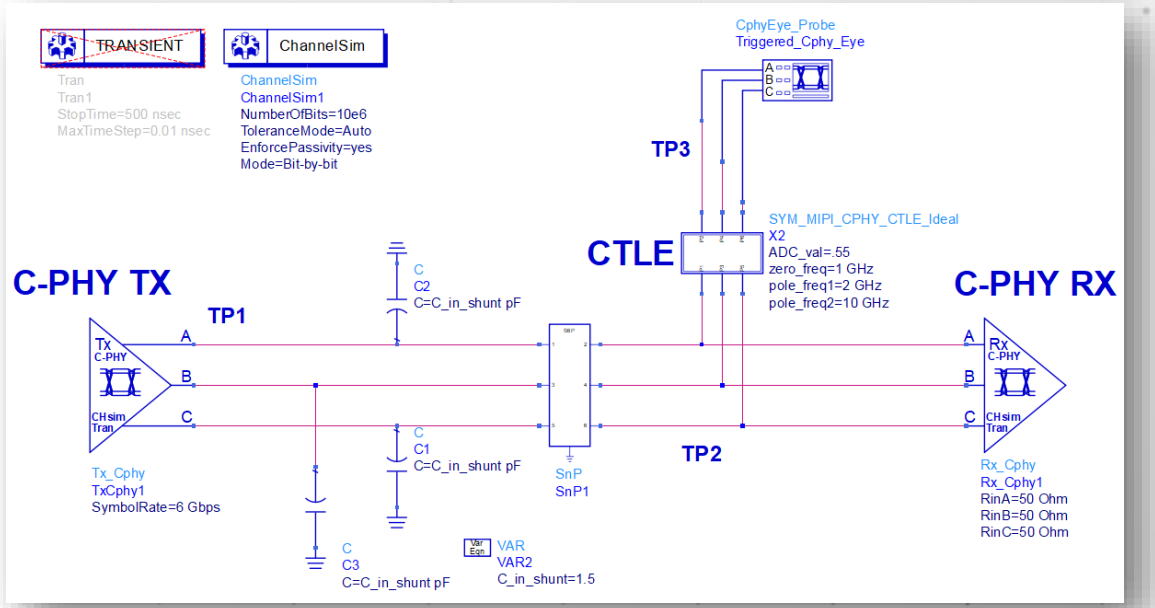
SIMPLER AND EASIER

- Dedicated C-PHY transmitter, receiver, and eye probe with triggered eye
- Supports both transient and channel simulation technologies
- Supports TX equalization and jitter models such as RJ, PJ, and clock DCD



Today

Note: Courtesy of Qualcomm

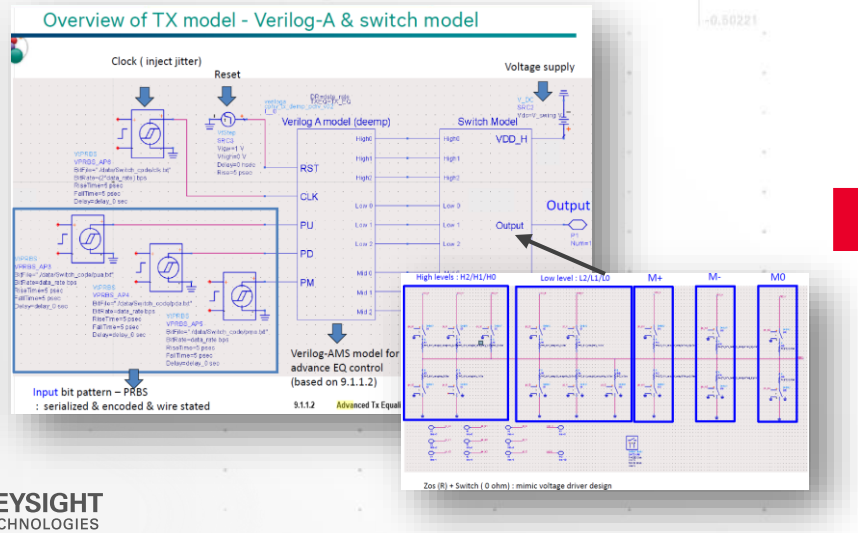


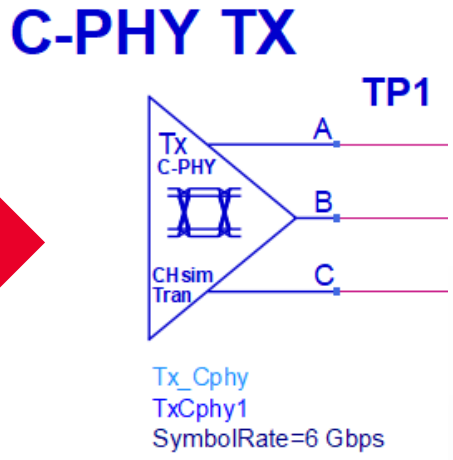
New

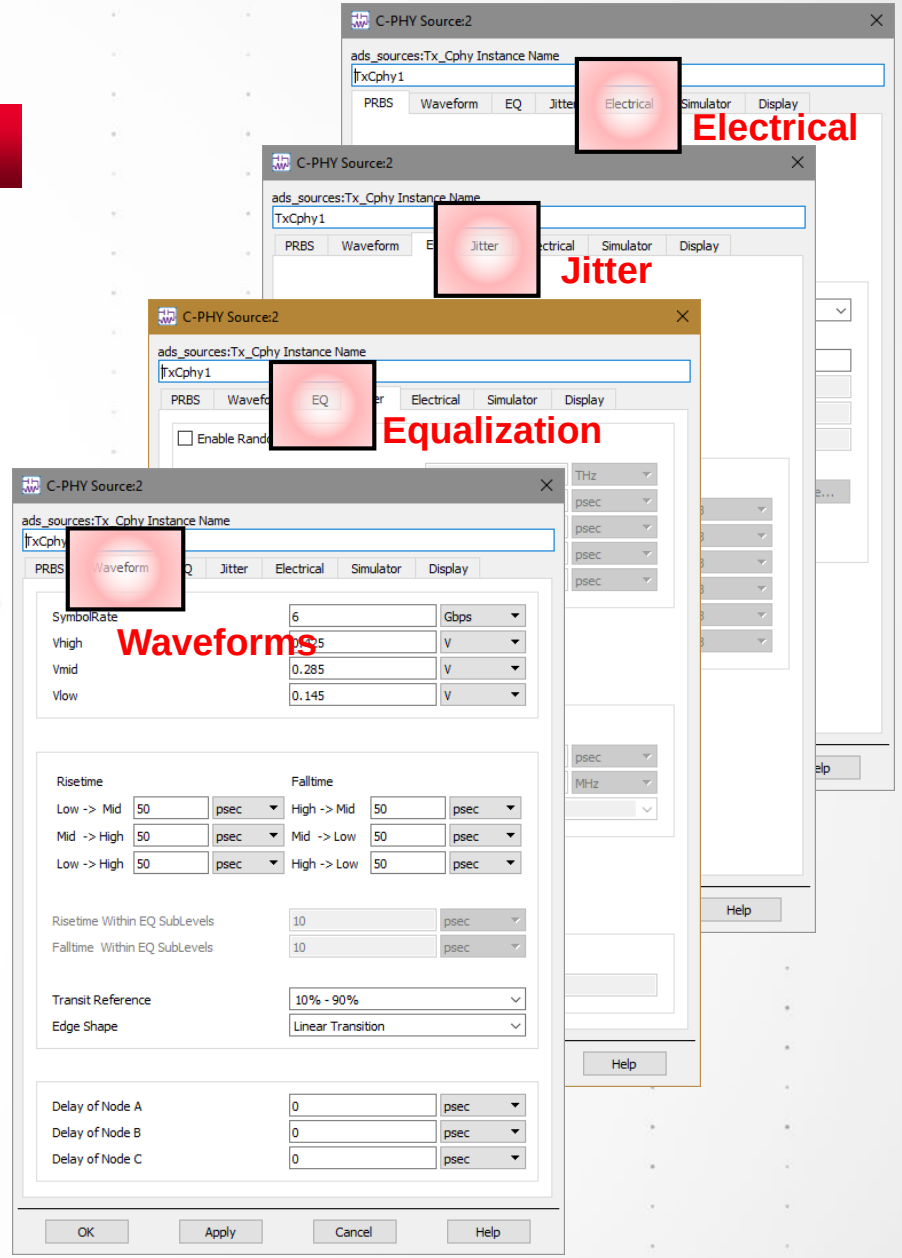
Details on C-PHY Transmitter (TX)

COMPLETE C-PHY SIGNAL SOURCE

- Tab organized special C-PHY source
  - PRBS : Maximal length LFSR, User defined LFSR, etc
  - Waveform : Vhigh, Vmid, Vlow, rise/fall time, edge shape, etc
  - Equalization : TxEQ
  - Jitter : Random, periodic jitter and clock DCD (Duty Cycle Distortion)
  - Electrical : Rout per node and level
  - Simulator : Auto, Transient and Channel simulator







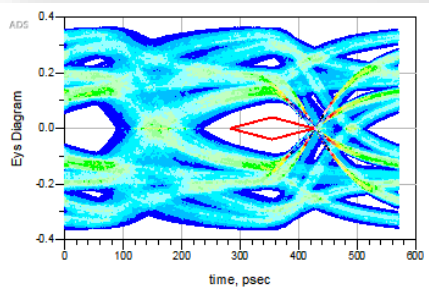
Test Case: No TX_EQ

3.5GSPS, 60 Z_IN, STANDARD CHANELL

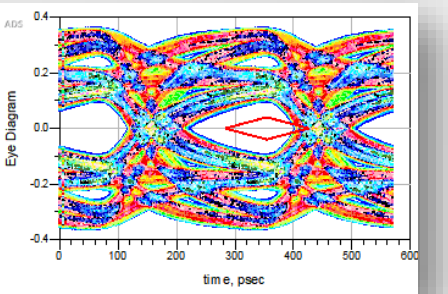
- TX Source
  - Symbol rate = 3.5Gsps
  - Waveforms
    - Vhigh = 425 mV
    - Vmid = 212.5 mV
    - Vlow = 0 V
    - Rise time/Fall time = 25ps, symmetric
- Still enough margin…

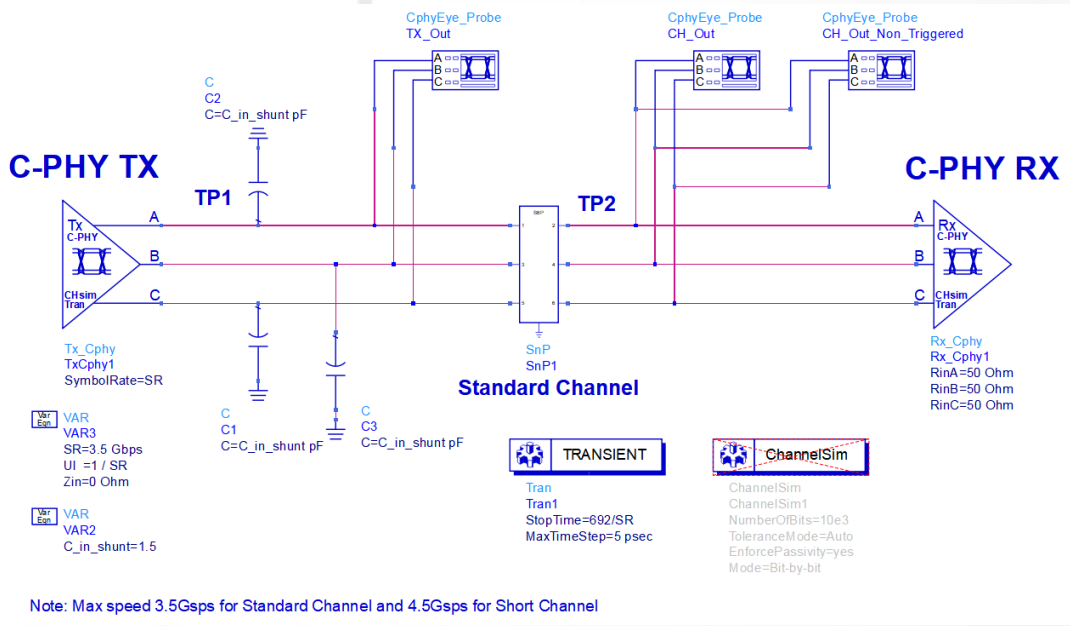
measurement	...Q.CH_Out.Summary
EyeOpeningHeight	201.0 m
EyeOpeningWidth	197.1 p
AverageUIDuration	285.7 p
MaxJitterInUI	193.5 m
MinUI	806.5 m
CphyMaskViolated	0.0000

Triggered



Non-Triggered





Test Case: Adding TX_EQ

3.5GSPS, 60 Z_IN, STANDARD CHANNEL

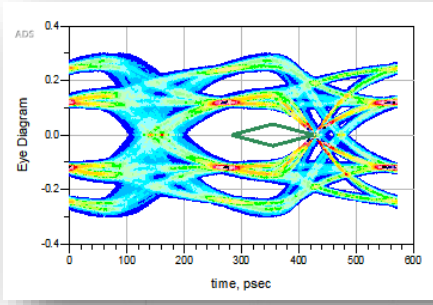
- TX Source
  - Symbol rate = 3.5Gsps
  - Waveforms
    - Vhigh = 425 mV
    - Vmid = 212.5 mV
    - Vlow = 0 V
    - Rise time/Fall time = 25ps, symmetric
  - TX Equalization

Enable Advanced TxEQ

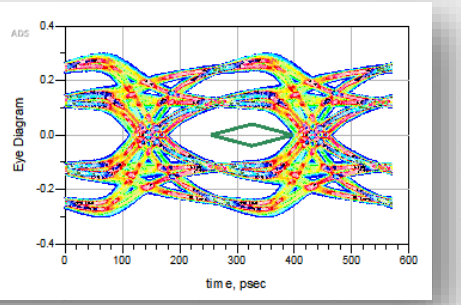
EQm1+	1.75	dB
EQm1-	1.75	dB
EQh1	1.75	dB
EQh0	3.5	dB
EQl1	1.75	dB
EQl0	3.5	dB

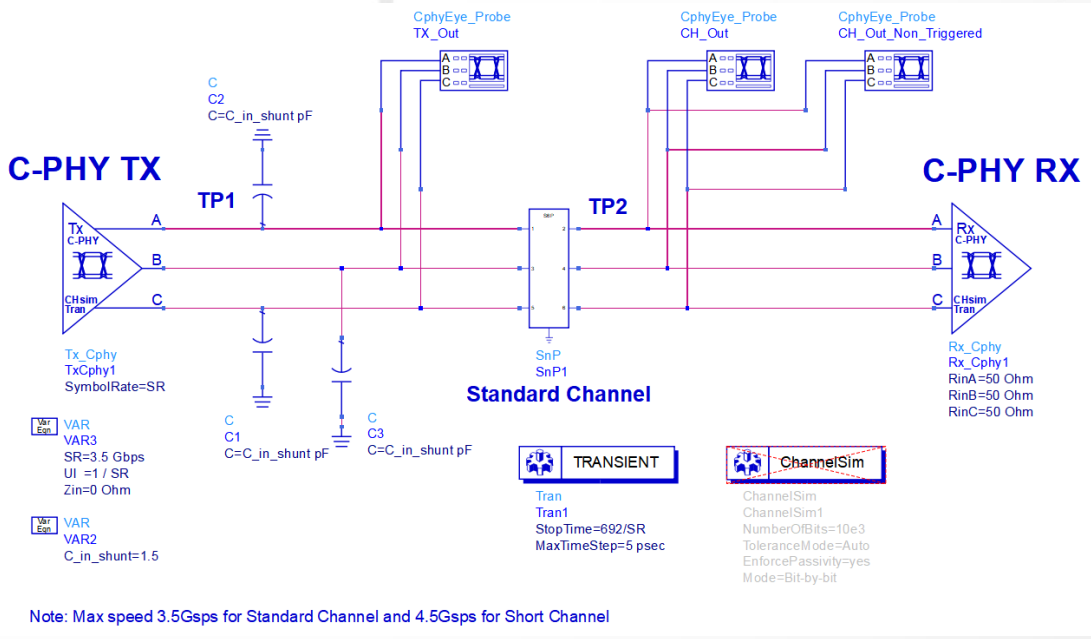
measurement	...Q.CH_Out.Summary
EyeOpeningHeight	209.0 m
EyeOpeningWidth	227.1 p
AverageUIDuration	285.7 p
MaxJitterInUI	126.1 m
MinUI	873.9 m
CphyMaskViolated	0.0000

Triggered



Non-Triggered





Note: Max speed 3.5Gsps for Standard Channel and 4.5Gsps for Short Channel

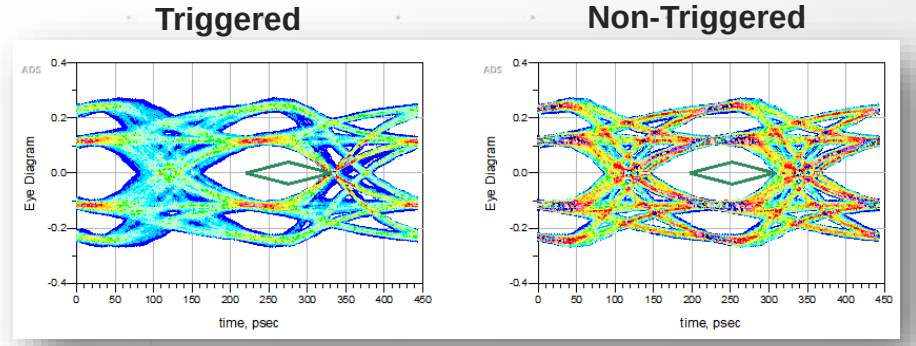
Enough Margin for Even 4.5Gsps with TQ_EX Only?

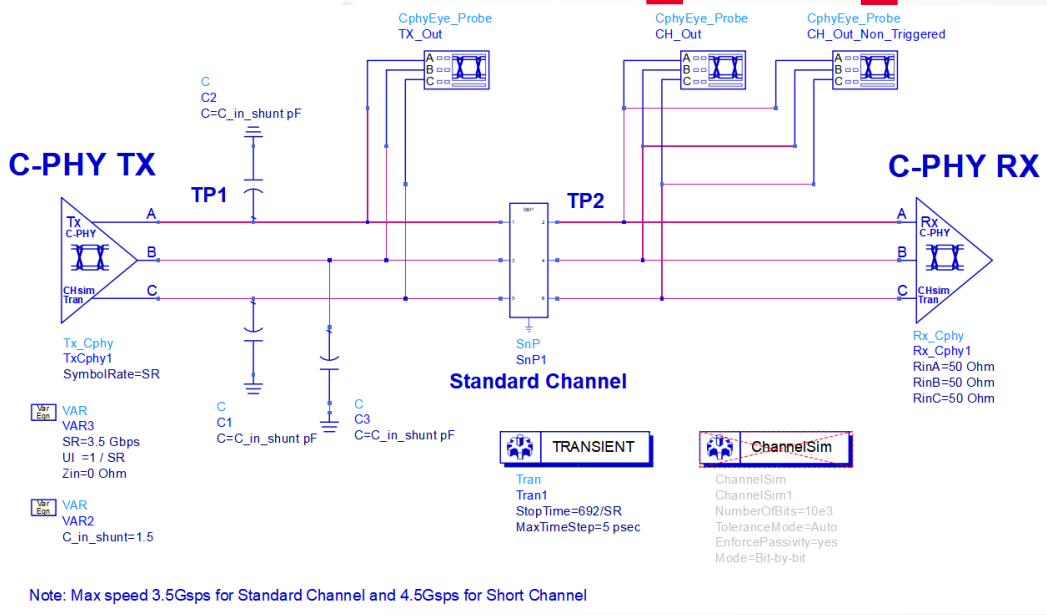
4.5GSPS, 60 Z_IN, STANDARD CHANNEL

- TX Source
  - Symbol rate = 4.5Gsps
  - Waveforms
    - Vhigh = 425 mV
    - Vmid = 212.5 mV
    - Vlow = 0 V
    - Rise time/Fall time = 25ps, symmetric
  - TX Equalization

  - Yes, it still provides good solution space

measurement	...Q..CH_Out.Summary
EyeOpeningHeight	204.0 m
EyeOpeningWidth	166.7 p
AverageUIDuration	222.2 p
MaxJitterInUI	154.4 m
MinUI	845.6 m
CphyMaskViolated	0.0000

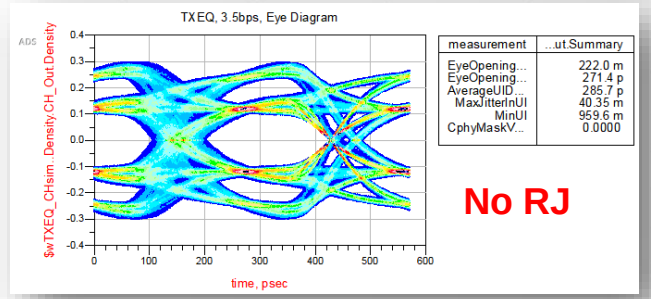


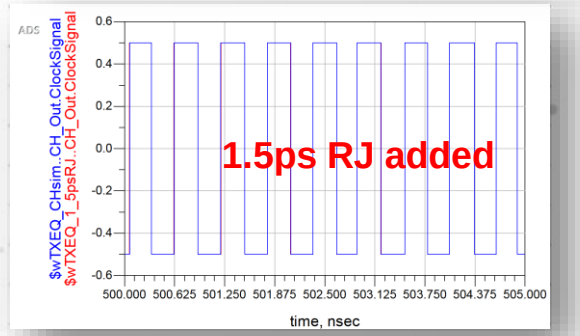


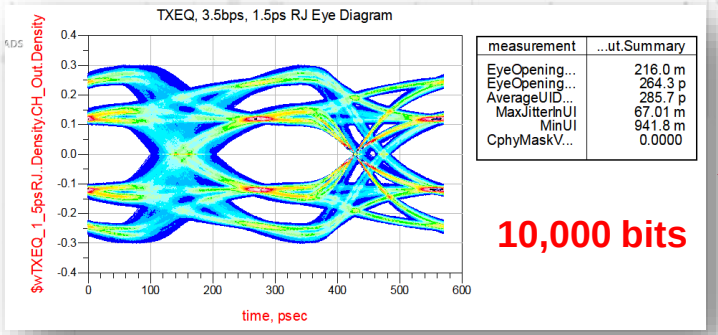
RJ (Random Jitter) Impact on Eye Diagram

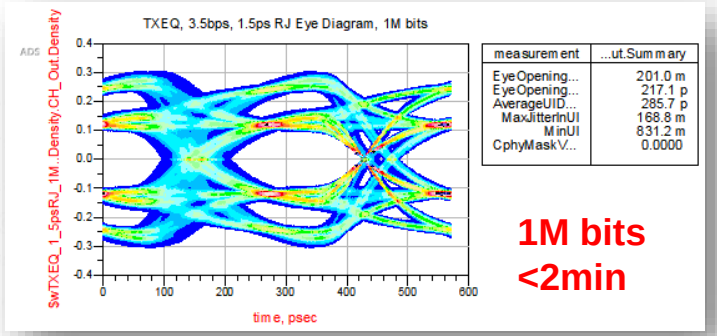
HOW MANY BITS ARE ENOUGH FOR RJ?

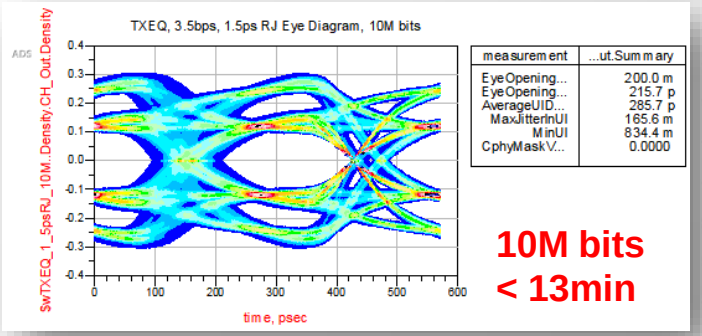
- 1.5ps RJ results in 6mV and 7.1ps eye closure with 10,000 bits
- What about running with more bits?
  - 1M bits results in significant eye closure, 19mV and 54.3ps smaller eye
  - 10M bits results in 20mV and 55.7ps smaller eye
- It is important to run with more bits to ensure the analysis accuracy
  - In this case, 1M bits are good enough









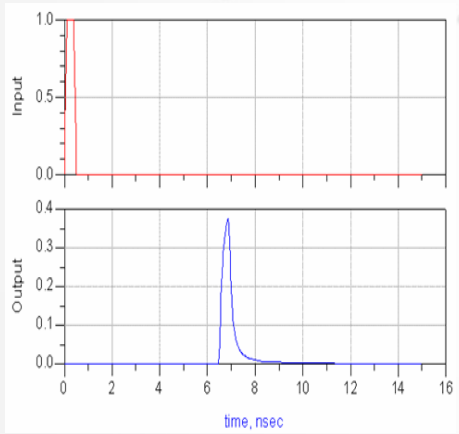


Channel Simulation Technology

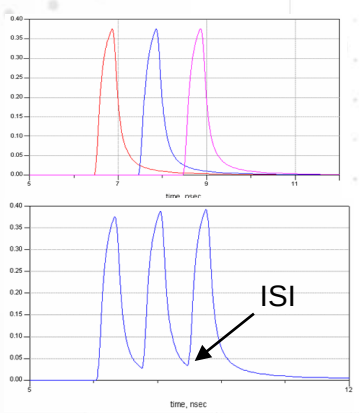
MILLIONS BITS IN MINUTES NOT DAYS!

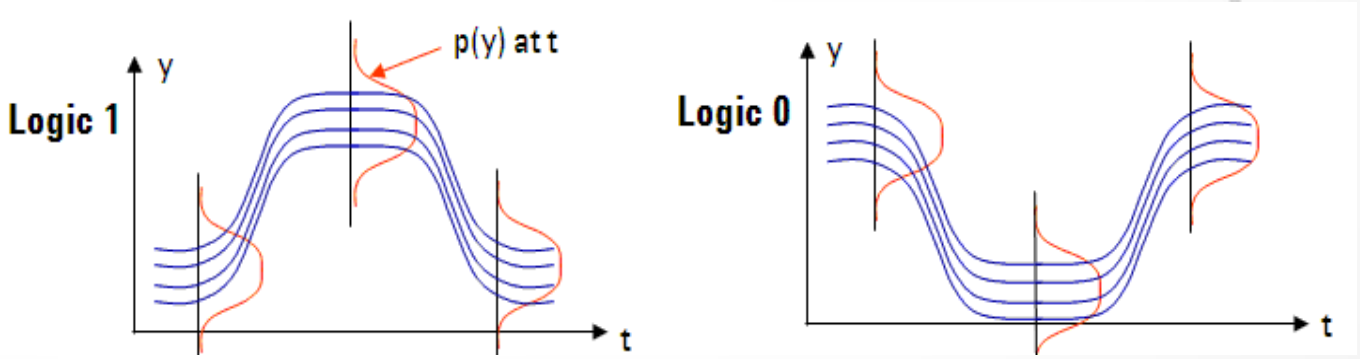
- Channel Simulation
  - The impulse response is calculated using a short, traditional transient simulation on the channel, Tx, Rx, and analog *.ibs model files
  - Bit-by-Bit mode performs superposition on an explicit bit pattern
  - Statistical mode applies statistical techniques to the stochastic properties of conceptually infinite non-repeating bit pattern, not the bit pattern itself (**C-PHY only support Bit-by-Bit mode**)

Impulse Response



Superposition



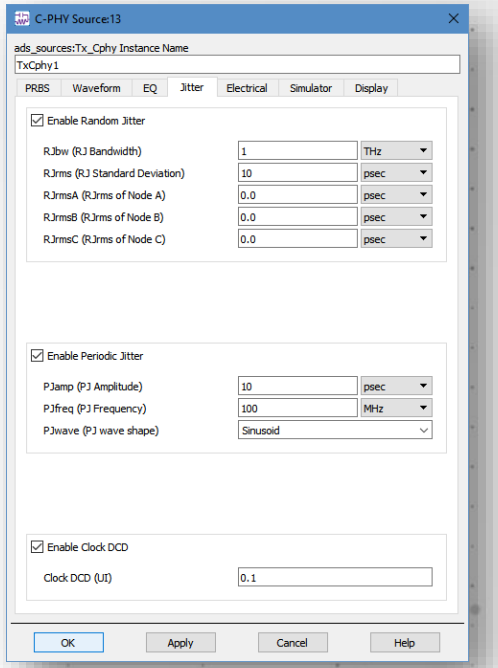


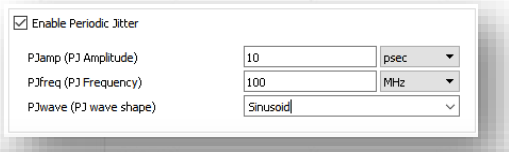
Inherently capturing the worst-case eye at any desired BER!

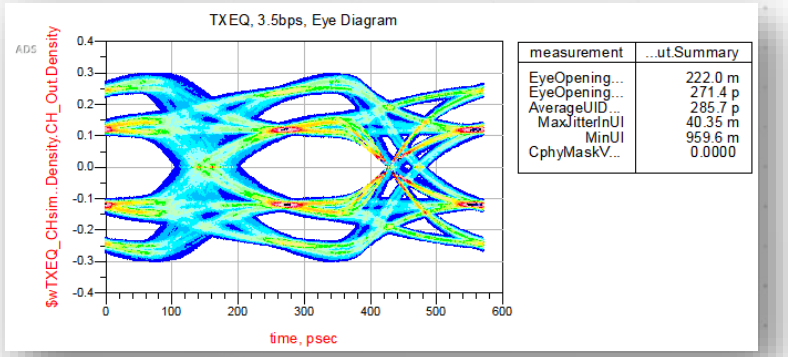
Other Jitter Impact

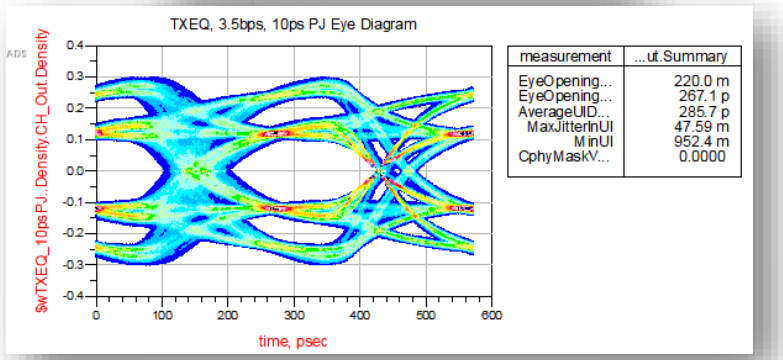
CLOCK DCD AND PERIODIC JITTER

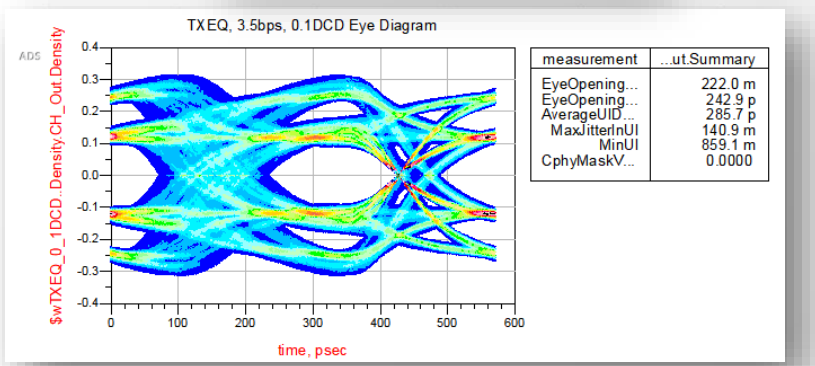
- Periodic Jitter
  - ➢10ps 100MHz PJ results in 30mV, 4.3ps eye closure
- Clock DCD (Duty Cycle Distortion) Jitter
  - ➢0.1 DCD results in 0mV and 28.5ps eye closure





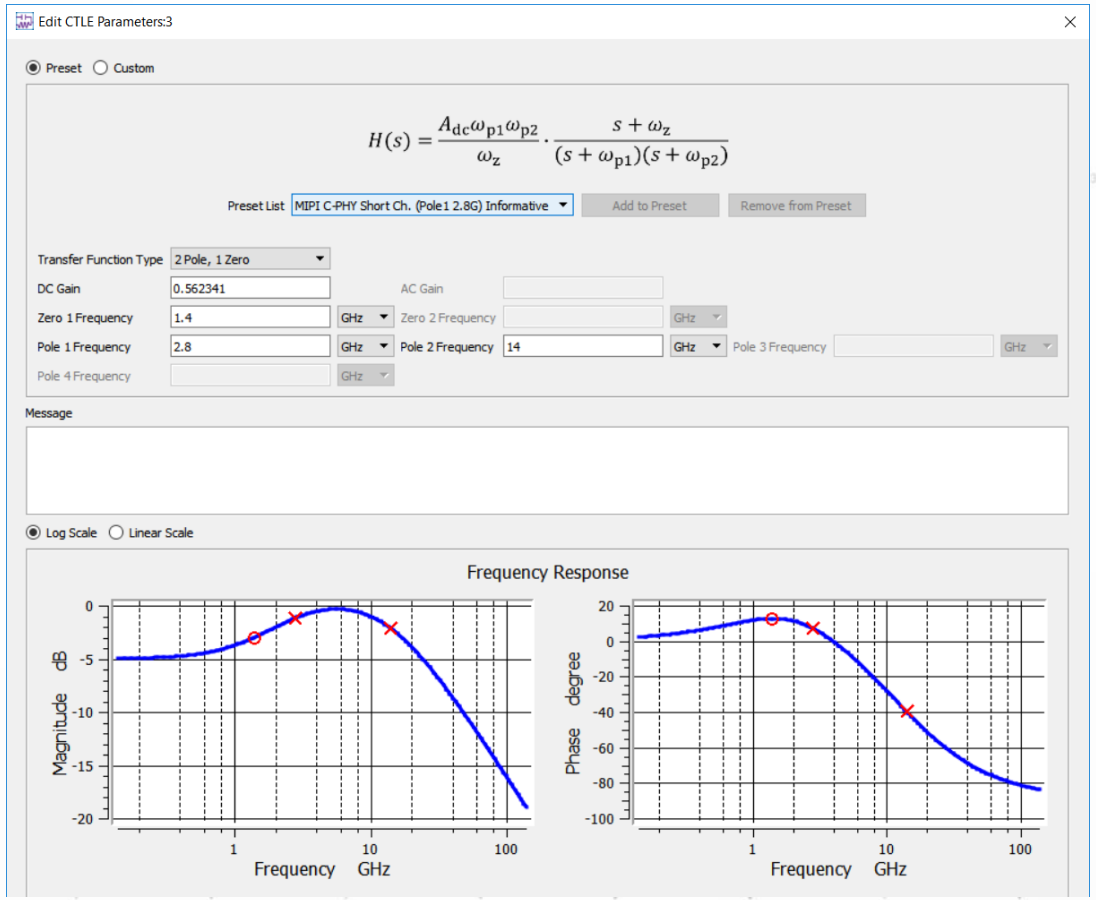


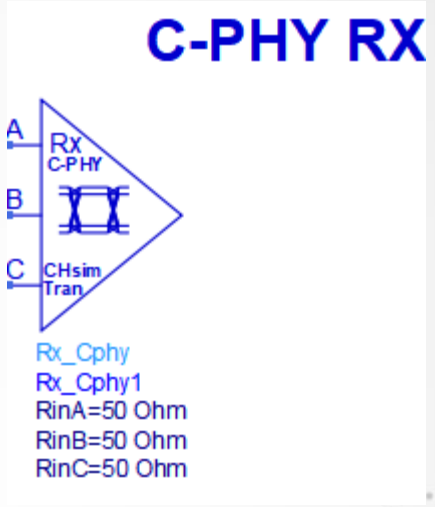




C-PHY RX (Receiver)

- RX with Equalization.





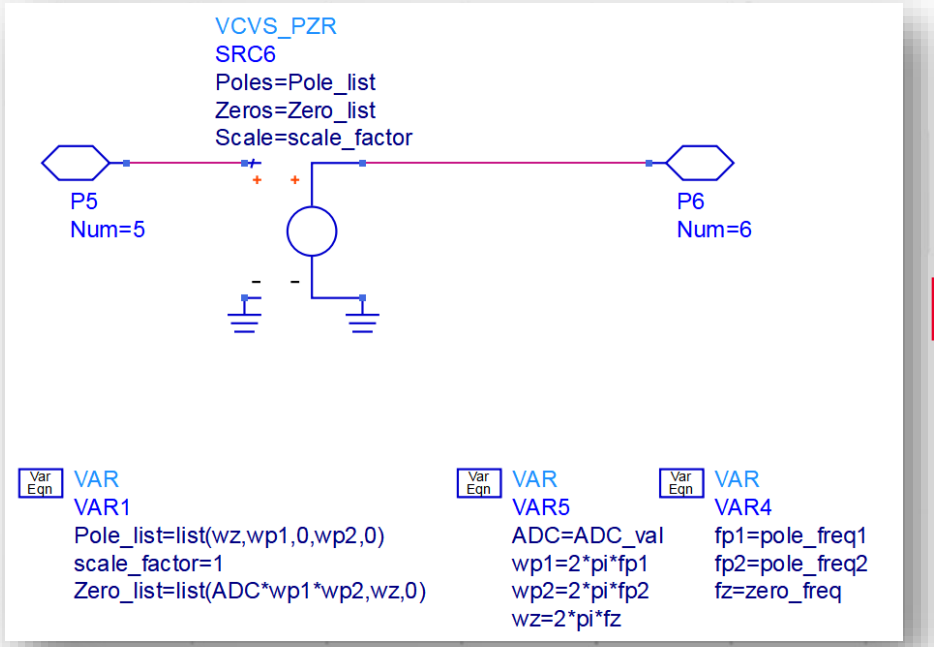
Implementing CTLE Equalization

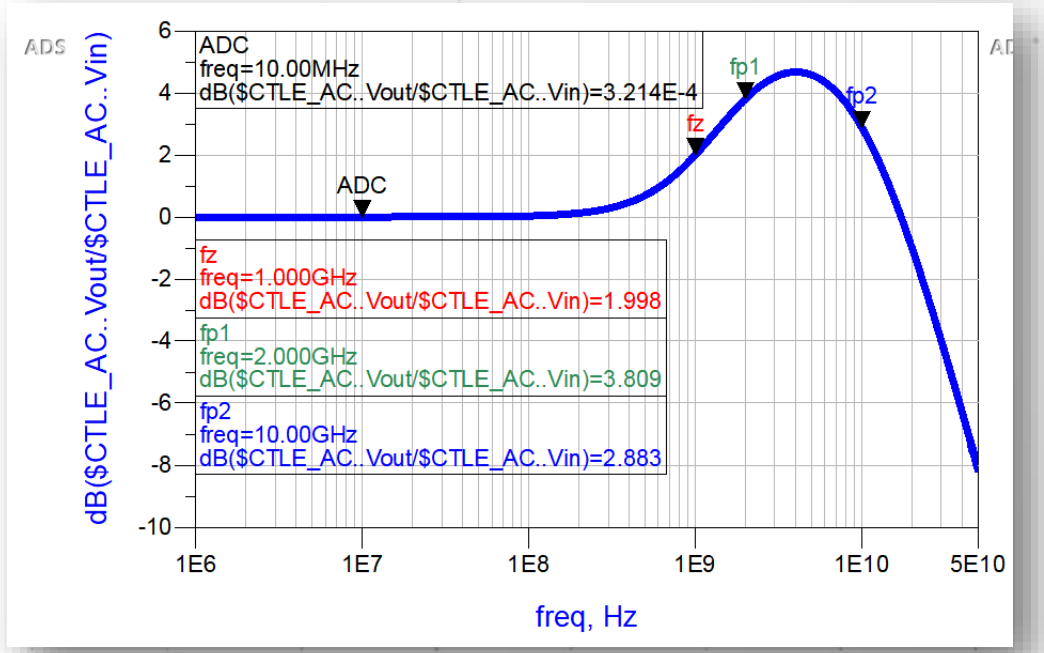
BY SIMPLE TRANSFER FUNCTION SOLUTION

- CTLE C-PHY Transfer function

$$H(s) = \frac{A_{DC}\omega_{P1}\omega_{P2}}{\omega_Z} \cdot \frac{s+\omega_Z}{(s+\omega_{P1})(s+\omega_{P2})}$$

A_{DC}	is the DC gain,
$\omega_{P1} = 2\pi f_{P1}$	f_{P1} is the first pole frequency
$\omega_{p2} = 2\pi f_{P2}$	f_{P2} is the second pole frequency
$\omega_Z = 2\pi f_Z$	f_Z is the zero frequency

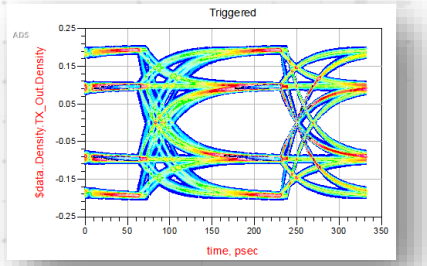


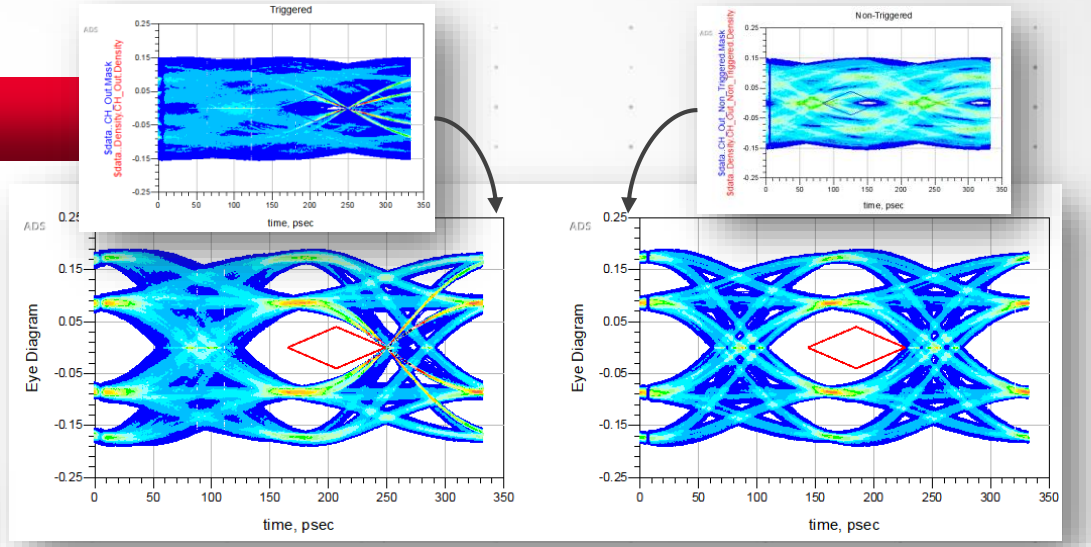


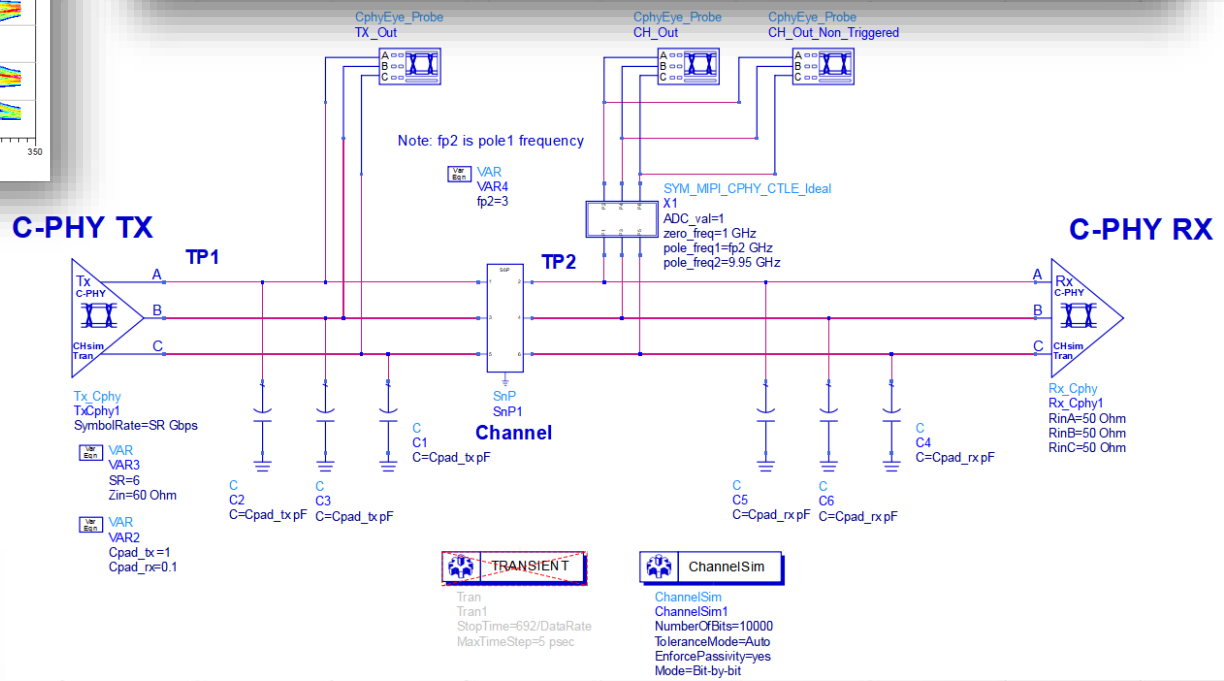
CTLE Validation Test

6GSPS WITH STANDARD CHANNEL

- Poles and zeros
  - fz = 1 GHz, fp1 = 3GHz, fp2 = 9.95GHz
- ADC set to 1
- Cpad_tx = 1pF
- Cpad_rx = 0.1pF
- Standard channel
- Eye width
  - Triggered = 120.8ps, Non-triggered = 117.5ps







measurement	$data..CH_Out.Summary
EyeOpeningHeight	147.0 m
EyeOpeningWidth	120.8 p
AverageUIDuration	166.7 p
MaxJitterInUI	184.9 m
MinUI	815.1 m
CphyMaskViolated	0.0000

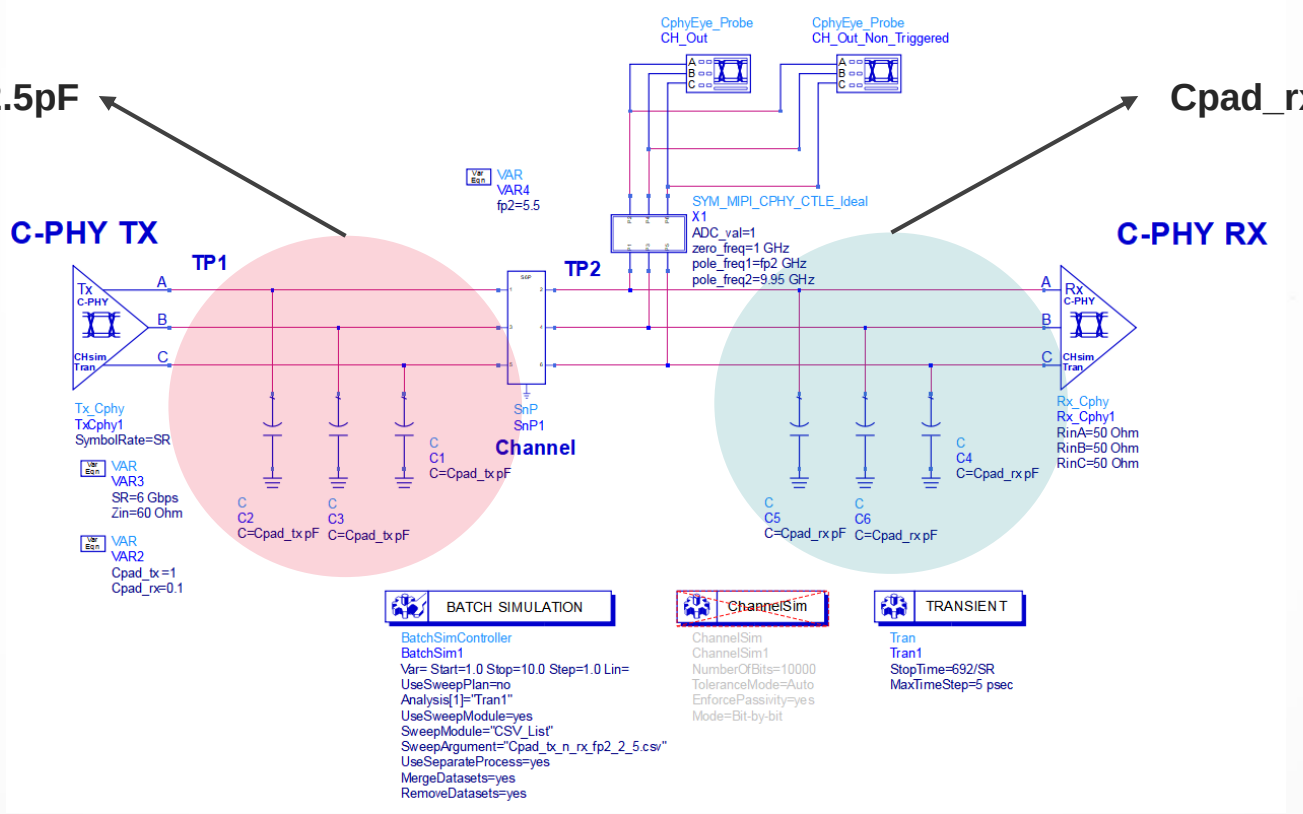
measurement	...on_Triggered.Summary
EyeOpeningHeight	149.0 m
EyeOpeningWidth	117.5 p
AverageUIDuration	166.7 p
MaxJitterInUI	184.9 m
MinUI	815.1 m
CphyMaskViolated	0.0000

Open Eye Study

CPAD_TX AND CPAD_RX WITH CTLE

Target Eye Mask

- w/o clock jitter: EW=0.65UI EH=+/-40mV
- w/ clock jitter: EW=0.5UI EH=+/-40mV

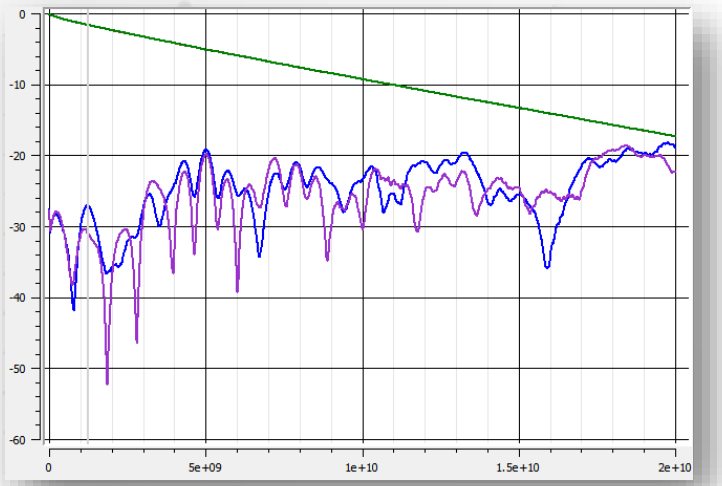


3 Channels for Tests

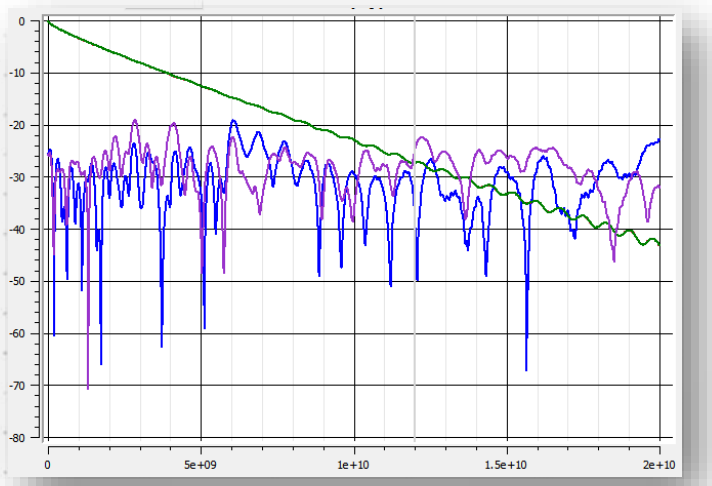
3 CHANNELS S-PARAMETER DATA

- Short channel is driven by 8Gsps signal
- Standard channel is driven by 6Gsps signal
- Long channel is driven by 4Gsps signal

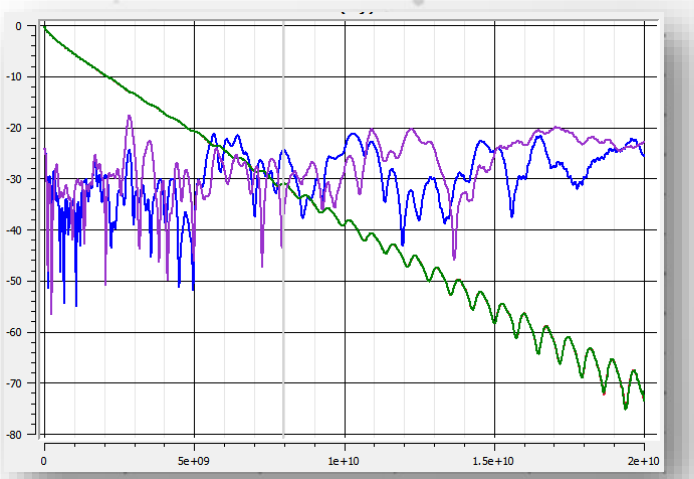
Short Channel



Standard Channel



Long Channel



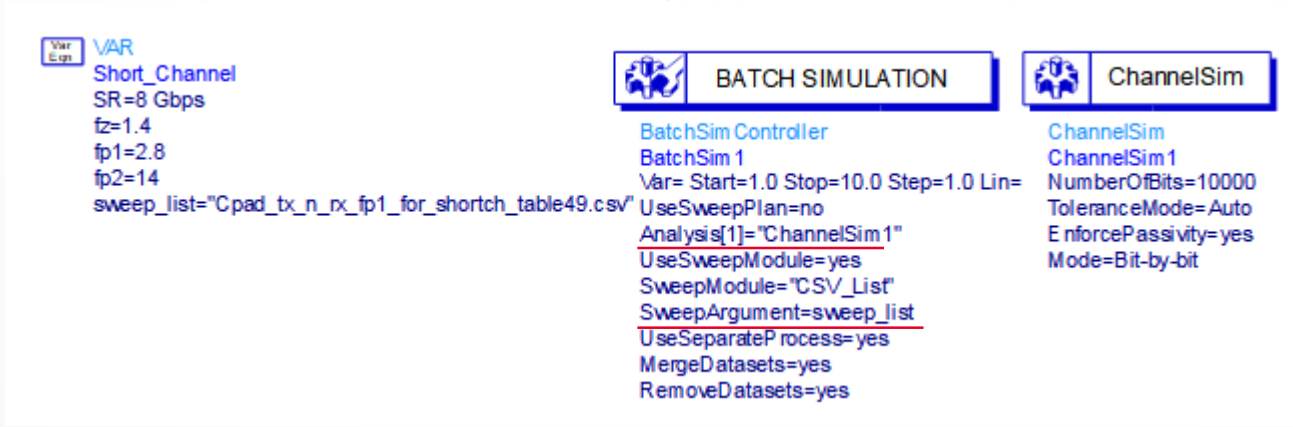
Batch Simulation

RUN FASTER AND EASIER FOR ALL COMBINATIONS

- Total 36 cases for short, standard, and 96 cases for long channels
  - Short Channel case
    - Cpad_tx : 0.5 ~ 1.5 pF, 0.5pF step size
    - Cpad_rx : 2 cases 0.5pF and 1pF
    - Pole1 frequency : 2.8,3.1,3.4,3.6,3.9, and 4.2
    - Pole2 frequency : 14GHz
    - Zero frequency : 1.4GHz

  Vhigh : 425mV
  Zin : 60ohm
  Rise/fall time : 0ps
  Signal transition : 0-100%

- Simple batch simulation setup
  - .csv file for the list of combinations



Excel .csv format

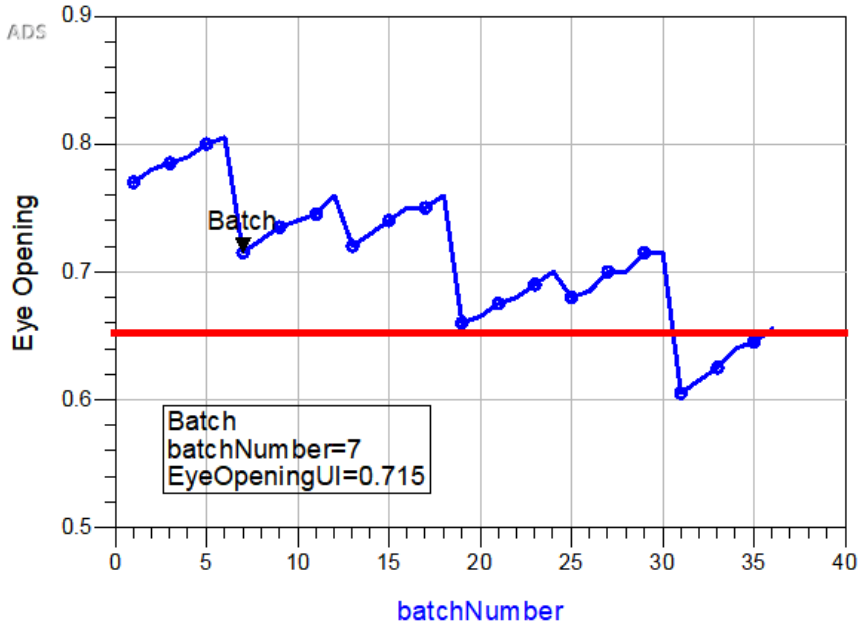
	A	B	C
1	Cpad_tx	Cpad_rx	fp1
2	0.5	0.5	2.8
3	0.5	0.5	3.1
4	0.5	0.5	3.4
5	0.5	0.5	3.6
6	0.5	0.5	3.9
7	0.5	0.5	4.2
8	0.5	1	2.8
9	0.5	1	3.1
10	0.5	1	3.4
11	0.5	1	3.6
12	0.5	1	3.9
13	0.5	1	4.2
14	1	0.5	2.8
15	1	0.5	3.1
16	1	0.5	3.4
17	1	0.5	3.6
18	1	0.5	3.9
19	1	0.5	4.2
20	1	1	2.8
21	1	1	3.1
22	1	1	3.4
23	1	1	3.6
24	1	1	3.9
25	1	1	4.2
26	1.5	0.5	2.8
27	1.5	0.5	3.1
28	1.5	0.5	3.4
29	1.5	0.5	3.6
30	1.5	0.5	3.9
31	1.5	0.5	4.2
32	1.5	1	2.8
33	1.5	1	3.1
34	1.5	1	3.4
35	1.5	1	3.6
36	1.5	1	3.9
37	1.5	1	4.2

Short Channel Case

ZERO = 1.4GHZ, POLE2 = 14GHZ, 8GBPS

- Without clock DCD

Cpad_tx	Cpad_rx	pole1	pole1/zero
...ta..Cpad_tx[Idx]	...ta..Cpad_rx[Idx]	...chData..fp1[Idx]	Rzp1
0.500	1.000	2.800	2.000



Eye Height

...Summary[Idx,0]
154.0 m

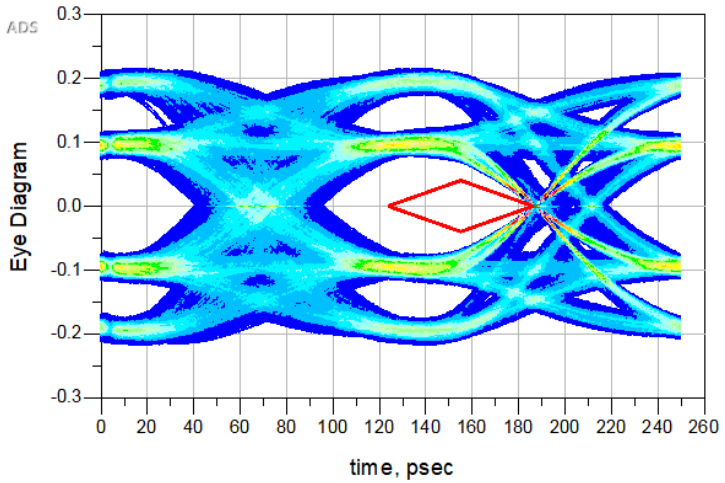
Eye Width

...Summary[Idx,1]
89.38 p

Eye Opening in UI

...eOpeningUI_Idx
0.715

Triggered



Triggered

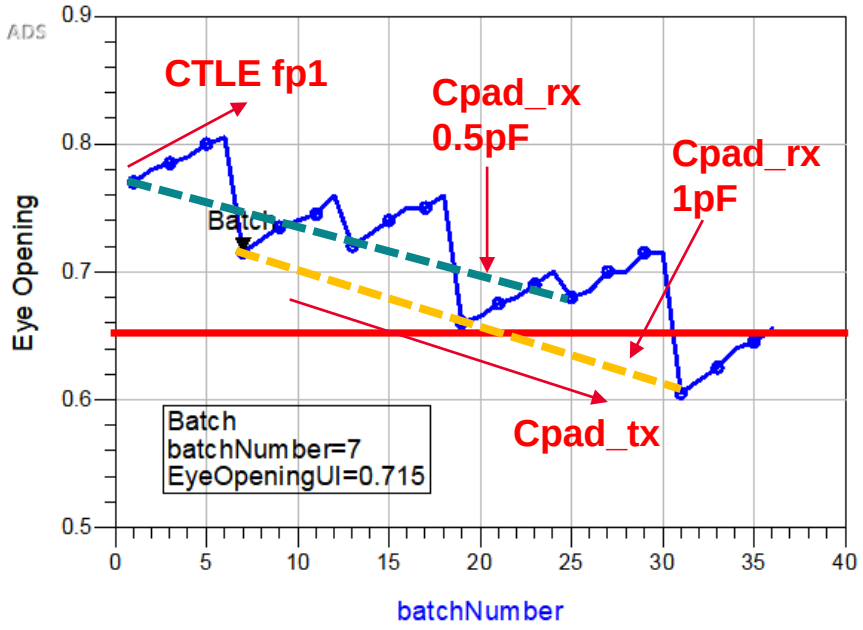
measurement	...t.Summary[Idx,::]
EyeOpeningHeight	154.0 m
EyeOpeningWidth	89.38 p
AverageUIDuration	125.0 p
MaxJitterInUI	189.5 m
MinUI	810.5 m
CphyMaskViolated	0.0000

Short Channel Case

ZERO = 1.4GHZ, POLE2 = 14GHZ, 8GBPS

- Without clock DCD

Cpad_tx	Cpad_rx	pole1	pole1/zero
...ta..Cpad_tx[Idx]	...ta..Cpad_rx[Idx]	...chData..fp1[Idx]	Rzp1
0.500	1.000	2.800	2.000



Eye Height

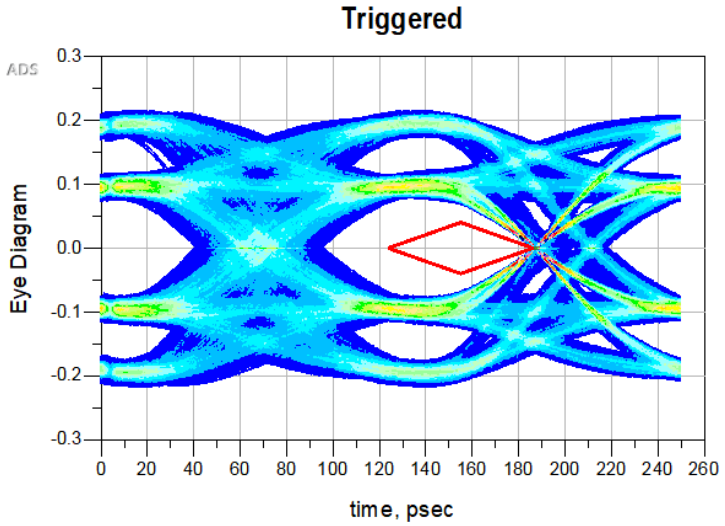
...Summary[Idx,0]
154.0 m

Eye Width

...Summary[Idx,1]
89.38 p

Eye Opening in UI

...eOpeningUI_Idx
0.715



Triggered

measurement	...t.Summary[Idx,::]
EyeOpeningHeight	154.0 m
EyeOpeningWidth	89.38 p
AverageUIDuration	125.0 p
MaxJitterInUI	189.5 m
MinUI	810.5 m
CphyMaskViolated	0.0000

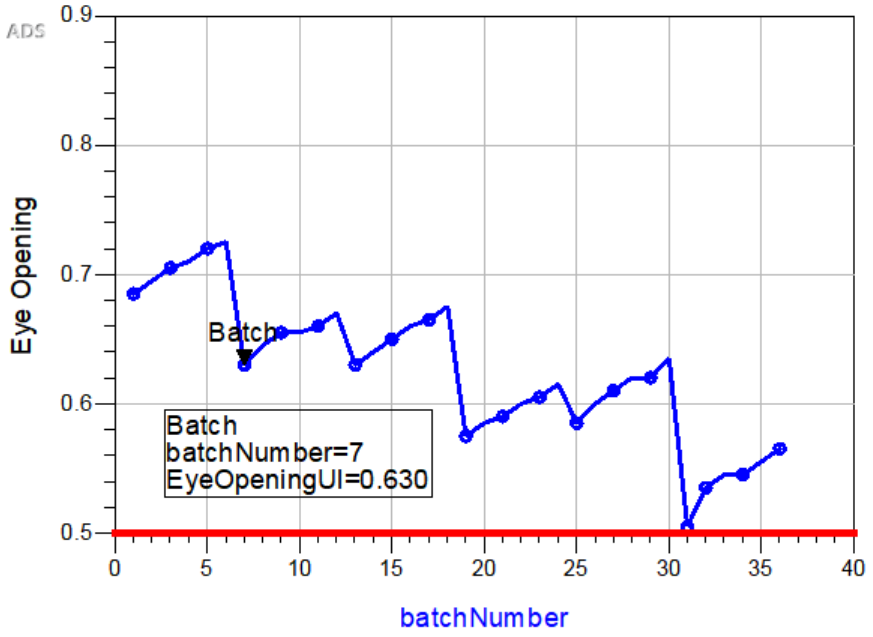
Good solution space..

Short Channel Case

ZERO = 1.4GHZ, POLE2 = 14GHZ, 8GBPS

- With 0.1 clock DCD

Cpad_tx	Cpad_rx	pole1	pole1/zero
...ta..Cpad_tx[Idx]	...ta..Cpad_rx[Idx]	...chData..fp1[Idx]	Rzp1
0.500	1.000	2.800	2.000



Eye Height

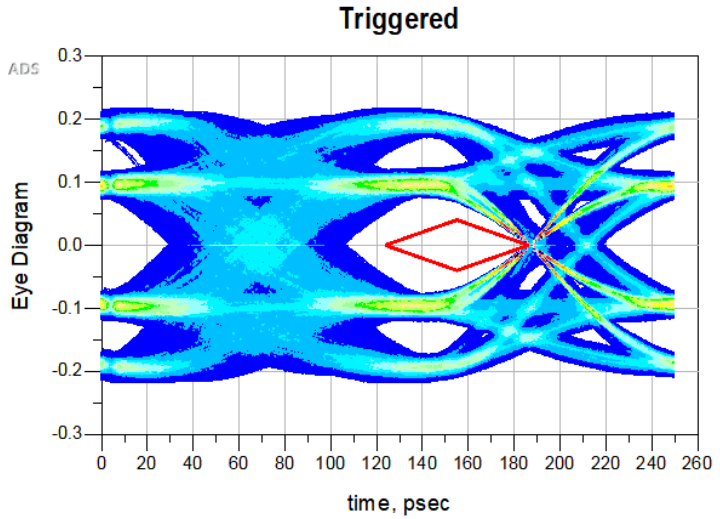
...Summary[Idx,0]
154.0 m

Eye Width

...Summary[Idx,1]
78.75 p

Eye Opening in UI

...eOpeningUI_Idx
0.630



Triggered

measurement	...t.Summary[Idx,::]
EyeOpeningHeight	154.0 m
EyeOpeningWidth	78.75 p
AverageUIDuration	125.0 p
MaxJitterInUI	284.6 m
MinUI	715.4 m
CphyMaskViolated	0.0000

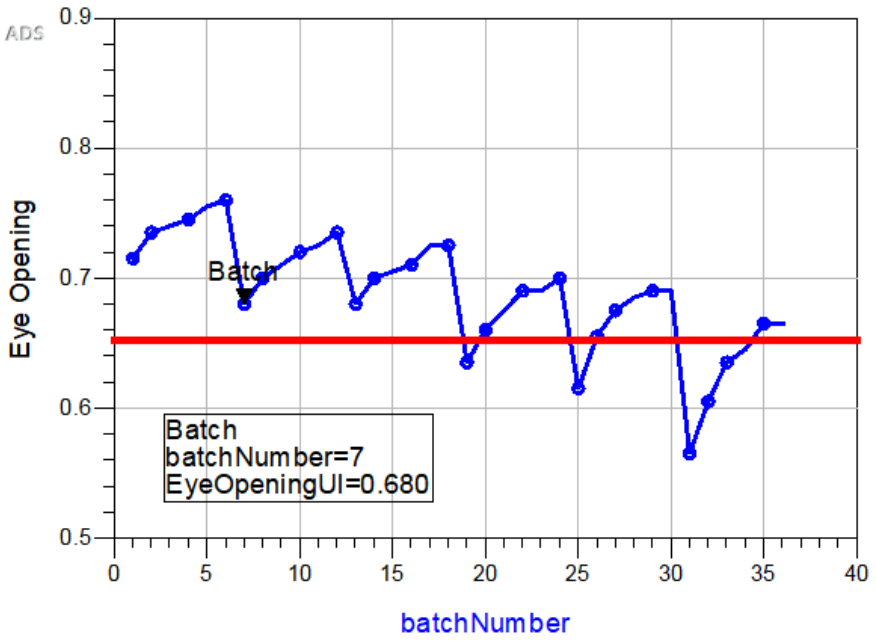
Good solution space..

Standard Channel Case

ZERO = 1GHZ, POLE2 = 10GHZ, 6GBPS

- Without clock DCD

Cpad_tx	Cpad_rx	pole1	pole1/zero
...ta..Cpad_tx[Idx]	...ta..Cpad_rx[Idx]	...chData..fp1[Idx]	Rzp1
0.500	1.000	2.000	2.000



Eye Height

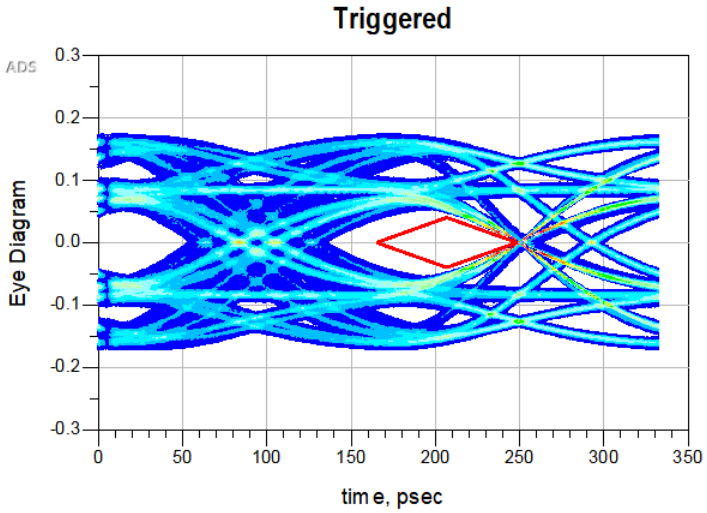
...Summary[Idx,0]
107.0 m

Eye Width

...Summary[Idx,1]
113.3 p

Eye Opening in UI

...eOpeningUI_Idx
0.680



Triggered

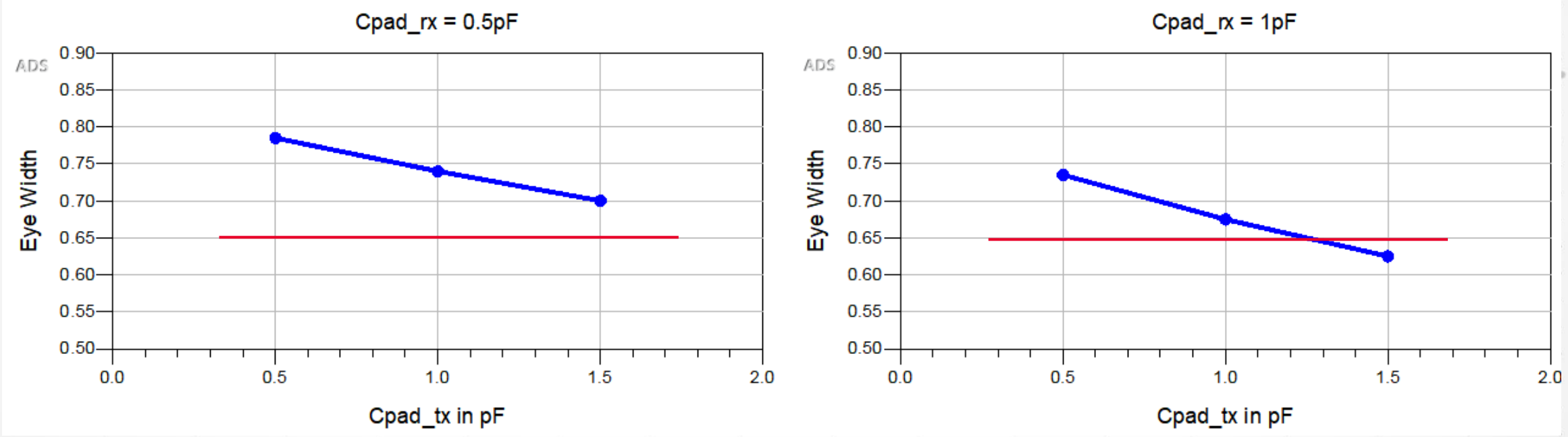
measurement	...t.Summary[Idx,::]
EyeOpeningHeight	107.0 m
EyeOpeningWidth	113.3 p
AverageUIDuration	166.7 p
MaxJitterInUI	180.5 m
MinUI	827.4 m
CphyMaskViolated	0.0000

Good solution space..

Eye Opening (UI) per Cpad_tx Value

SHORT CHANNEL, 8GSPS W/O CLOCK DCD JITTER

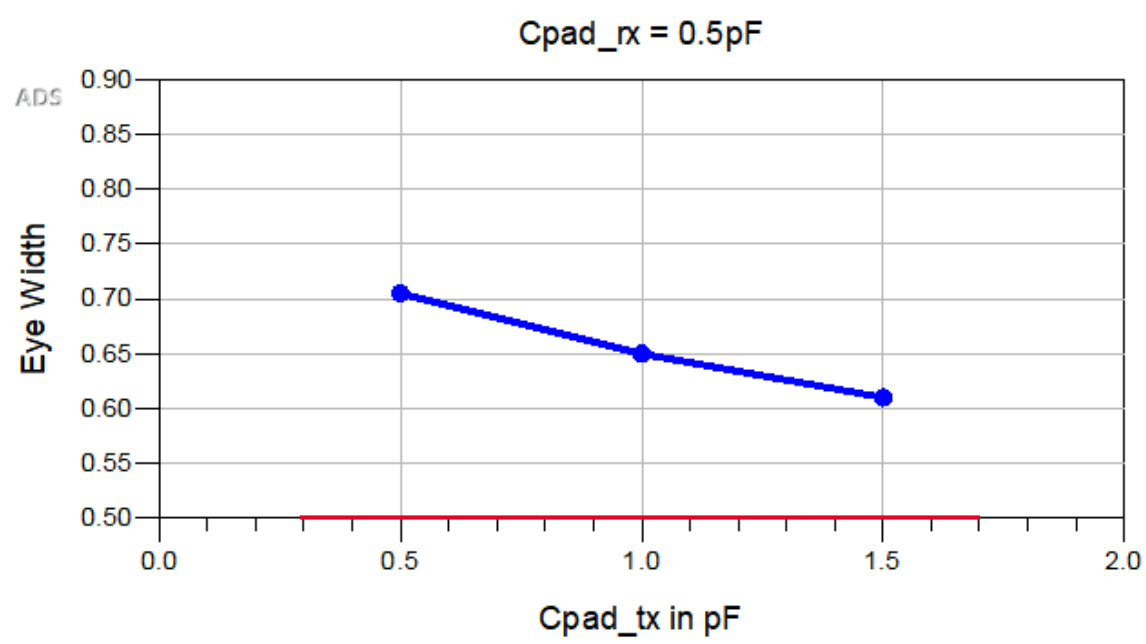
- Zero: 1.4GHz, Pole 1: **3.4GHz**, Pole 2: 14GHz

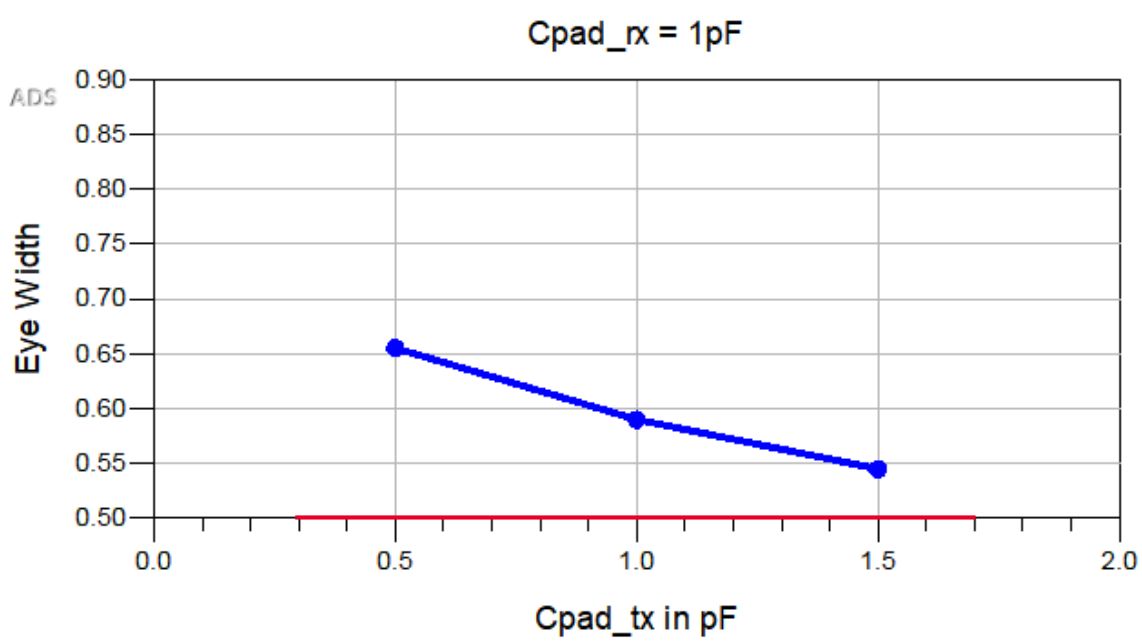


Eye Opening (UI) per Cpad_tx Value

SHORT CHANNEL, 8GSPS W 0.1 CLOCK DCD JITTER

- Zero: 1.4GHz, Pole 1: **3.4GHz**, Pole 2: 14GHz

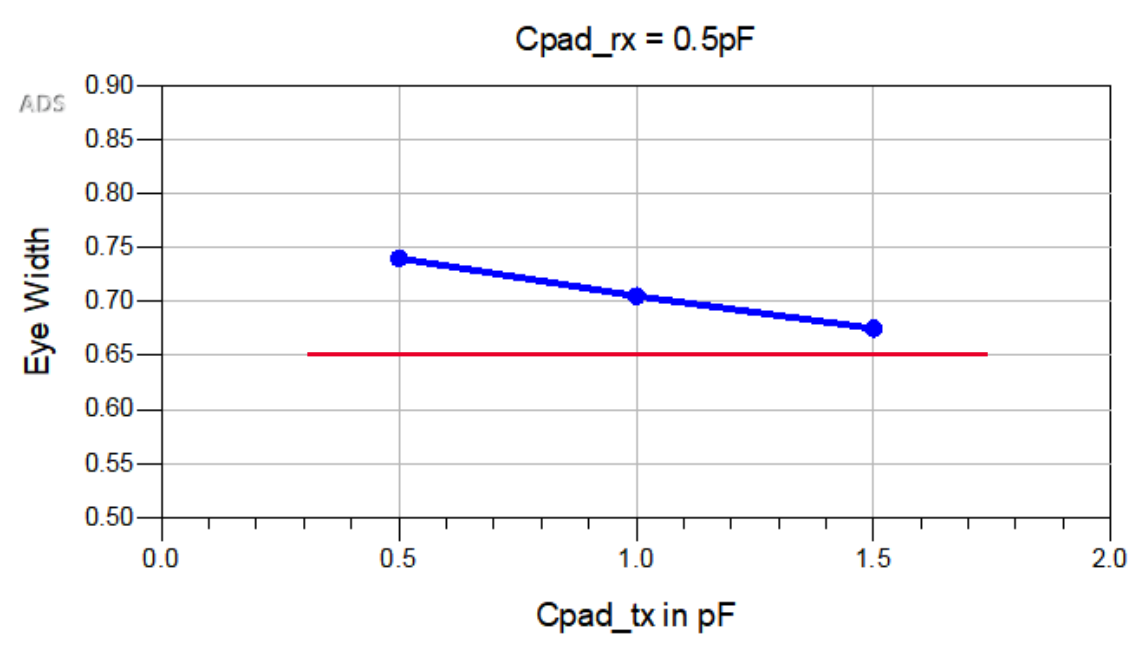


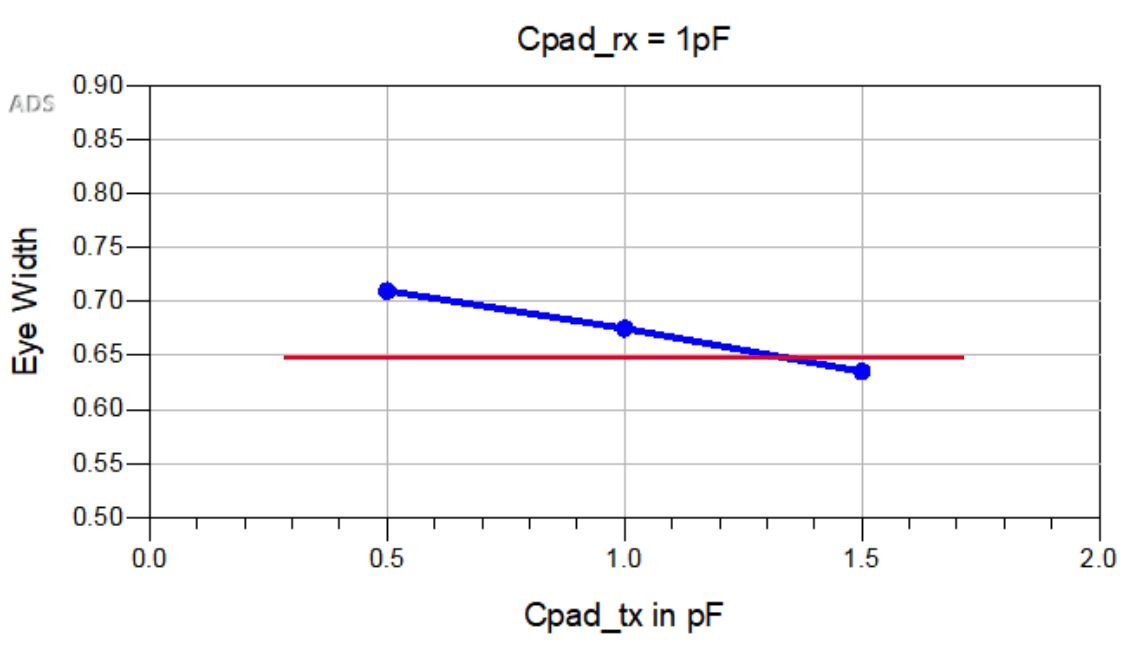


Eye Opening (UI) per Cpad_tx Value

STANDARD CHANNEL, 6GSPS W/O CLOCK DCD JITTER

- Zero: 1GHz, Pole 1: **2.4GHz**, Pole 2: 10GHz

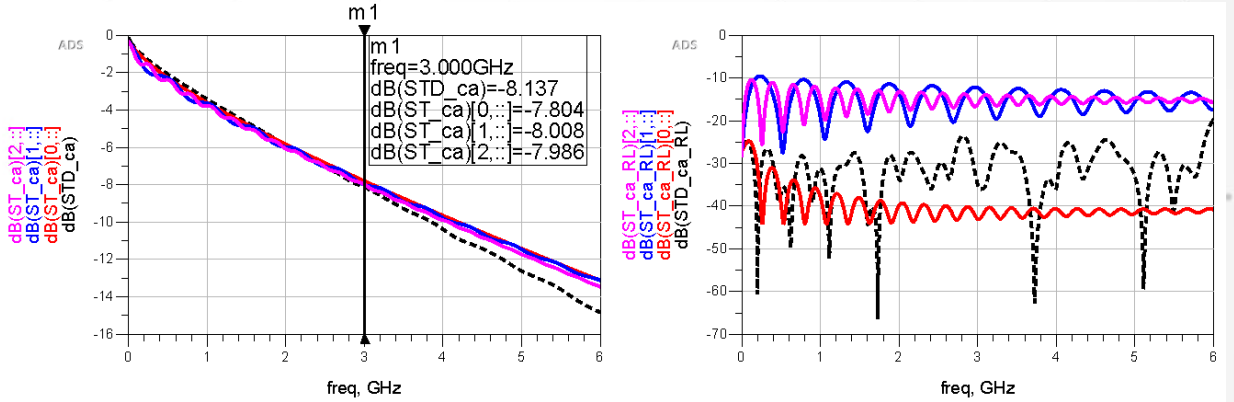




Impedance Discontinuity Study

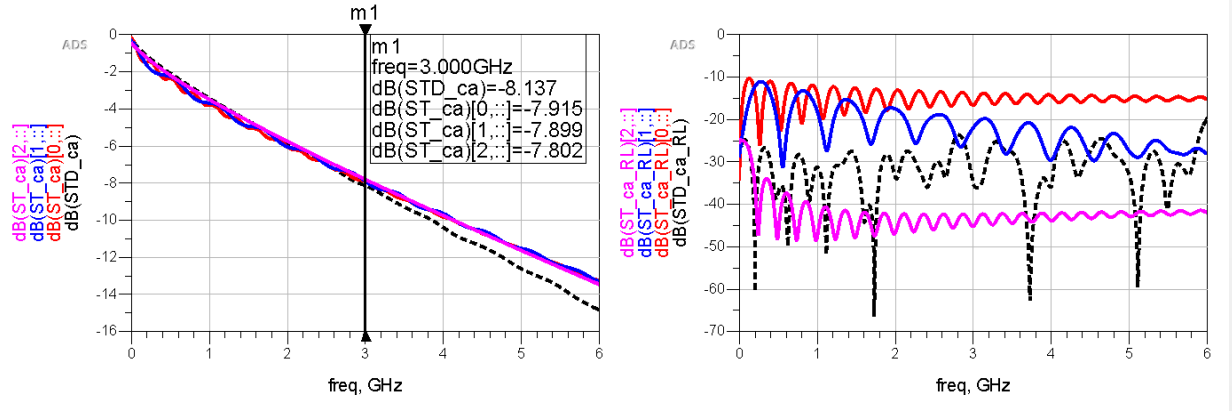
- 70ohm stripline + 100ohm microstrip

	Stripline (70Ω)	Ustrip (100Ω)
Case 1 (12.5”)	0”	12.5”
Case 2 (12”)	6”	6”
Case 3 (12”)	12”	0”



- 100ohm stripline + 70ohm microstrip

	Stripline (100Ω)	Ustrip (70Ω)
Case 1 (12.5”)	0”	12.5”
Case 2 (12.5”)	6.5”	6”
Case 3 (13”)	13”	0”



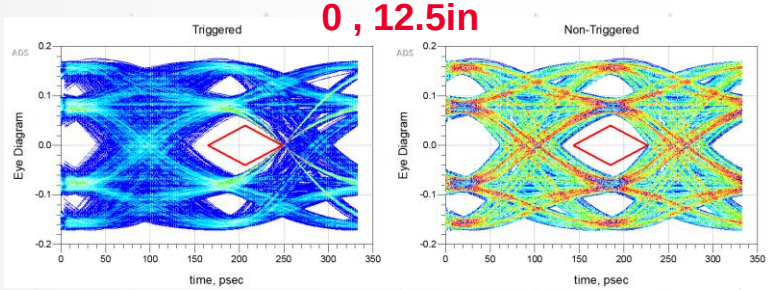
Results

GOOD MARGIN

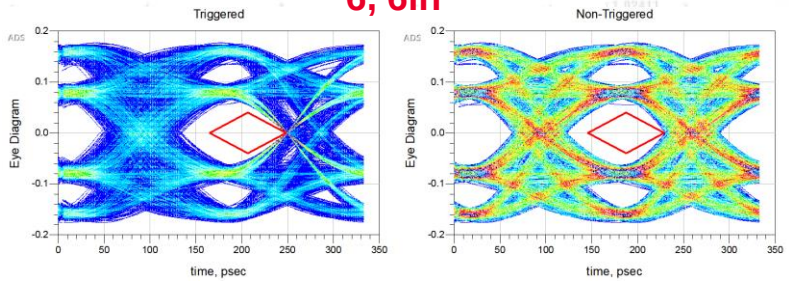
CTLE: ADC=1, zero = 1GHz, pole1 = 3GHz, pole2=9.95GHz, Cpad_tx: 2pF

- 70ohm stripline + 100ohm microstrip

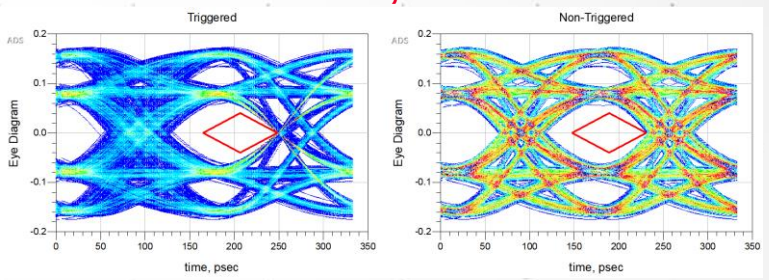
0 , 12.5in



6, 6in

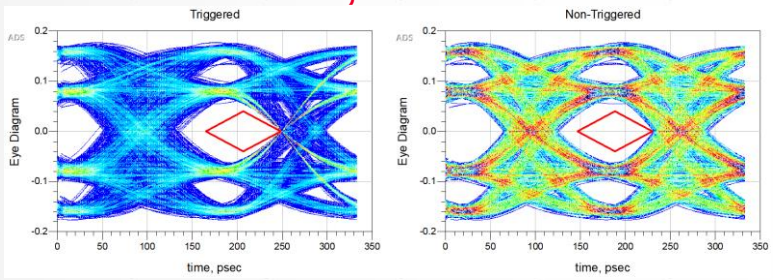


12, 0in

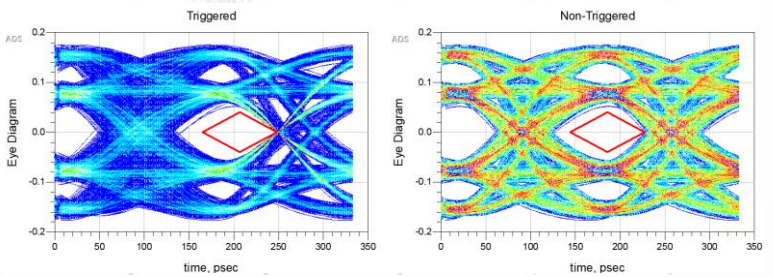


- 100ohm stripline + 70ohm microstrip

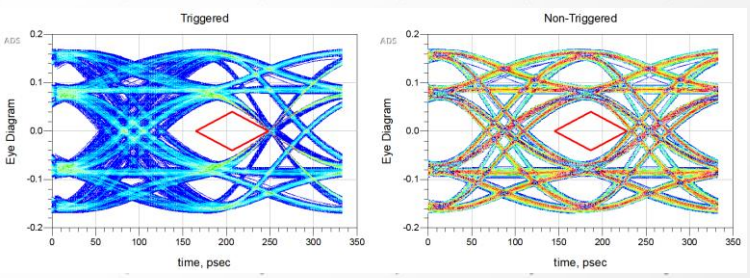
0 , 12.5in



6.5, 6in

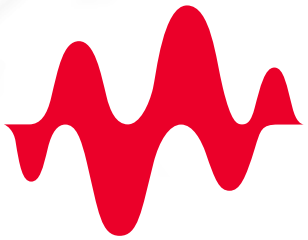


13, 0in



Summary

- With TX_EQ and CTLE RX equalizations, it is demonstrated that there is enough solution space for different channel configurations, including impedance mismatch from the channel
- The channel simulation technology empower C-PHY designers to evaluate the designs with millions of bits in minutes
- New ADS modeling and simulation environment provides an easier, faster, and complete solution for C-PHY design exploration



KEYSIGHT
TECHNOLOGIES