MIPI C-PHY Solving Simulation Challenges

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Today's Typical C-PHY Simulation Challenges

HIGHLIGHTS

- Complicated transmitter and receiver modeling process including equalizations
 - Need simple transmitter and receiver models
- No single platform solution but using multiple tools such as Verilog-A, meaning lots of customization required
 - Need just simple one platform solution without much customization
- Limited jitter analysis
 - Need full support of RJ, PJ and DCD
- SPICE-alike simulations result in long simulation time and limit number of bits that can be simulated
 - Need channel simulation technology for faster simulation with millions of bits
- Non-triggered eye plot

Need triggered eye plot to support MIPI C-PHY specification



Today's and New C-PHY Generic Model Architecture

SIMPLER AND EASIER

- Dedicated C-PHY transmitter, receiver, and eye probe with triggered eye
- Supports both transient and channel simulation technologies
- Supports TX equalization and jitter models such as RJ, PJ, and clock DCD





.

Details on C-PHY Transmitter (TX)

COMPLETE C-PHY SIGNAL SOURCE

- Tab organized special C-PHY source
 - PRBS : Maximal length LFSR, User defined LFSR, etc
 - · Waveform : Vhigh, Vmid, Vlow, rise/fall time, edge shape, etc
 - Equalization : TxEQ
 - Jitter : Random, periodic jitter and clock DCD (Duty Cycle Distortion)
 - Electrical : Rout per node and level
 - Simulator : Auto, Transient and Channel simulator



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Test Case: No TX_EQ

3.5GSPS, 60 Z_IN, STANDARD CHANELL

TX Source

- Symbol rate = 3.5Gsps
- Waveforms
 - ➤Vhigh = 425 mV
 - ➤Vmid = 212.5 mV
 - \geq VIow = 0 V
 - Rise time/Fall time = 25ps, symmetric
- Still enough margin...





Test Case: Adding TX_EQ

3.5GSPS, 60 Z_IN, STANDARD CHANNEL

• TX Source

- Symbol rate = 3.5Gsps
- Waveforms
 - Vhigh = 425 mV
 - Vmid = 212.5 mV
 - Vlow = 0 V
 - Rise time/Fall time = 25ps, symmetric

TX Equalization

🗹 Enable	e Advanced TxE0	2				
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EQI1						•
EQI0			3.5		dB	•
			÷	24		





Enough Margin for Even 4.5Gsps with TQ_EX Only?

4.5GSPS, 60 Z_IN, STANDARD CHANNEL

• TX Source

- Symbol rate = 4.5Gsps
- Waveforms
 - Vhigh = 425 mV
 - Vmid = 212.5 mV
 - Vlow = 0 V
 - Rise time/Fall time = 25ps, symmetric

TX Equalization

Enable Advanced TxEQ		
EQm1+	1.75	dB 🔻
EQm1-	1.75	dB 👻
EQh1	1.75	dB 🔻
EQh0	3.5	dB 🔻
EQI1	1.75	dB 👻
EQI0	3.5	dB 🔻

• Yes, it still provides good solution space





RJ (Random Jitter) Impact on Eye Diagram

HOW MANY BITS ARE ENOUGH FOR RJ?

- 1.5ps RJ results in 6mV and 7.1ps eye closure with 10,000 bits
- What about running with more bits?
 - 1M bits results in significant eye closure, <u>19mV and 54.3ps</u> smaller eye
 - 10M bits results in 20mV and 55.7ps smaller eye
- It is <u>important</u> to run with more bits to ensure the analysis accuracy
 - In this case, 1M bits are good enough





Channel Simulation Technology

MILLIONS BITS IN MINUTES NOT DAYS!

- Channel Simulation
 - The impulse response is calculated using a short, traditional transient simulation on the channel, Tx, Rx, and analog *.ibs model files
 - Bit-by-Bit mode performs superposition on an explicit bit pattern
 - Statistical mode applies statistical techniques to the stochastic properties of conceptually infinite non-repeating bit pattern, not the bit pattern itself (<u>C-PHY only support Bit-by-Bit mode</u>)





Other Jitter Impact

CLOCK DCD AND PERIODIC JITTER

Periodic Jitter

KEYSIGH

>10ps 100MHz PJ results in 30mV, 4.3ps eye closure

Clock DCD (Duty Cycle Distortion) Jitter
>0.1 DCD results in 0mV and 28.5ps eye closure



C Enable Periodic Jitter		
PJamp (PJ Amplitude)	10	psec
PJfreq (PJ Frequency)	100	MHz
PJwave (PJ wave shape)	Sinusoid	



Display PIES Waveform EQ Itter Betwie Random 3itter R.bw (R3 Bandwidth) I Ittr R.max (R15 tandard Deviation) 10 psec Plane Period: 3tter Plane (P1 Amplitude) 10 Plane (P1 Amplitude) 10 Plane (P1 Amplitude) 10 Plane (P2 Hamp (P1 Amplitude) 10 Plane (Dock DCD 0.1 Clock DCD (U1) 0.1 Clock DCD (U1) 0.1 Enable Clock DCD 0.1 Clock DCD (U1) 0.1 Eq. (3.5bps, 0.1DCD Eye Diagram EyeOpening 222.0 EyeOpening 222.0 EyeOpening 222.0		ada courceauTy. Coby Instance	o Nomo					
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C-PHY RX (Receiver)

• RX with Equalization.





Implementing CTLE Equalization

BY SIMPLE TRANSFER FUNCTION SOLUTION

CTLE C-PHY Transfer function is the DC gain, A_{DC} f_{P1} is the first pole frequency $\omega_{\rm P1} = 2\pi f_{\rm P1}$ $A_{DC}\omega_{P1}\omega_{P2}$. $\frac{\omega_{DC}\omega_{P1}\omega_{P2}}{\omega_{Z}} \cdot \frac{s+\omega_{Z}}{(s+\omega_{P1})(s+\omega_{P2})}$ H(s) = $\omega_{p2} = 2\pi f_{P2}$ f_{P2} is the second pole frequency $\omega_z = 2\pi f_z$ f_Z is the zero frequency VCVS PZR AC..Vin) ADC ADS SRC6 freg=10.00MHz Poles=Pole list dB(\$CTLE AC..Vout/\$CTLE AC..Vin)=3.214E-4 4– Zeros=Zero list Scale=scale factor AC..Vout/\$CTLE ADC **P5** P6 Num=5 Num=6 -2reg=1.000GHz dB(\$CTLE AC..Vout/\$CTLE AC..Vin)=1.998 rea=2.000GHz dB(\$CTLE AC. Vout/\$CTLE AC. Vin)=3.809 dB(\$CTLE -6 rea=10.00GHz dB(\$CTLE AC. Vout/\$CTLE AC. Vin)=2.883 Var VAR Var Eqn VAR Var Egn VAR VAR1 VAR5 VAR4 -10 Pole list=list(wz,wp1,0,wp2,0) ADC=ADC val fp1=pole freq1 1E6 1E7 1E8 1E9 1E10 5E10 scale factor=1 wp1=2*pi*fp1 fp2=pole freq2 Zero list=list(ADC*wp1*wp2,wz,0) wp2=2*pi*fp2 fz=zero freq freq, Hz wz=2*pi*fz **KEYSIGH1**

CTLE Validation Test

6GSPS WITH STANDARD CHANNEL

- Poles and zeros
 - fz = 1 GHz, fp1 = 3GHz, fp2 = 9.95GHz
- ADC set to 1
- Cpad_tx = 1pF
- Cpad_rx = 0.1pF
- Standard channel
- Eye width

ECHNOLOGIES

• Triggered = 120.8ps, Non-triggered = 117.5ps

riggered

time nee





Open Eye Study

CPAD_TX AND CPAD_RX WITH CTLE

Target Eye Mask

- w/o clock jitter: EW=0.65UI EH=+/-40mV
- w/ clock jitter: EW=0.5UI EH=+/-40mV





3 Channels for Tests

3 CHANNELS S-PARAMETER DATA

- Short channel is driven by 8Gsps signal
- Standard channel is driven by 6Gsps signal
- Long channel is driven by 4Gsps signal





Long Channel



Batch Simulation

RUN FASTER AND EASIER FOR ALL COMBINATIONS

Total 36 cases for short, standard, and 96 cases for long channels

Cpad tx n rx fp1 for shortch table49.

Analysis[1 UseSweep SweepMo

SweepArgument=sweep list

MergeDatasets=ve

- Short Channel case
 - Cpad_tx : 0.5 ~ 1.5 pF, 0.5pF step size
 - Cpad_rx : 2 cases 0.5pF and 1pF
 - Pole1 frequency : 2.8,3.1,3.4,3.6,3.9, and 4.2

Short_Channel SR=8 Gbps fz=1.4 fp1=2.8 fp2=14

sweep list='

- Pole2 frequency : 14GHz
- Zero frequency : 1.4GHz
- Simple batch simulation setup
 - .csv file for the list of combinations

Vhigh: 425mV		
Zin : 60ohm		
Rise/fall time : 0ps		
Signal transition : 0-1	100	%

TCH SIMULATION		ChannelSim
Controller =1.0 Stop=10.0 Step=1.0 Lin Plan=no ="ChannelSim1" Module=yes fule="CSV_List"	Cha Cha I= Num Tole Enfo Mod	nnelSim nnelSim1 IberOfBits=10000 ranceMode=Auto orcePassivity=yes e=Bit-by-bit

	Α	В	С
1	Cpad_tx	Cpad_rx	fp1
2	0.5	0.5	2.8
3	0.5	0.5	3.1
4	0.5	0.5	3.4
5	0.5	0.5	3.6
6	0.5	0.5	3.9
7	0.5	0.5	4.2
8	0.5	1	2.8
9	0.5	1	3.1
10	0.5	1	3.4
11	0.5	1	3.6
12	0.5	1	3.9
13	0.5	1	4.2
14	1	0.5	2.8
15	1	0.5	3.1
16	1	0.5	3.4
17	1	0.5	3.6
18	1	0.5	3.9
19	1	0.5	4.2
20	1	1	2.8
21	1	1	3.1
22	1	1	3.4
23	1	1	3.6
24	1	1	3.9
25	1	1	4.2
26	1.5	0.5	2.8
27	1.5	0.5	3.1
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34	1.5	1	3.4
35	1.5	1	3.6
36	1.5	1	3.9
37	1.5	1	4.2

16

Excel .csv format



Short Channel Case

ZERO = 1.4GHZ, POLE2 = 14GHZ, 8GBPS

Without clock DCD





Short Channel Case

ZERO = 1.4GHZ, POLE2 = 14GHZ, 8GBPS

Without clock DCD





Short Channel Case

ZERO = 1.4GHZ, POLE2 = 14GHZ, 8GBPS

• With 0.1 clock DCD

KEYSIGHT TECHNOLOGIES



Triggered

154.0 m 78.75 p 125.0 p

284.6 m

715.4 m

0.0000

Standard Channel Case

ZERO = 1GHZ, POLE2 = 10GHZ, 6GBPS

Without clock DCD

ECHNOLOGIES



Eye Opening (UI) per Cpad_tx Value

SHORT CHANNEL, 8GSPS W/O CLOCK DCD JITTER

Cpad_rx = 0.5pF

• Zero: 1.4GHz, Pole 1: <u>3.4GHz</u>, Pole 2: 14GHz





Eye Opening (UI) per Cpad_tx Value

SHORT CHANNEL, 8GSPS W 0.1 CLOCK DCD JITTER

• Zero: 1.4GHz, Pole 1: <u>3.4GHz</u>, Pole 2: 14GHz





Eye Opening (UI) per Cpad_tx Value

STANDARD CHANNEL, 6GSPS W/O CLOCK DCD JITTER

• Zero: 1GHz, Pole 1: 2.4GHz, Pole 2: 10GHz





Impedance Discontinuity Study

• 70ohm stripline + 100ohm microstrip

	Stripline (70Ω)	Ustrip (100Ω)
Case 1 (12.5")	0"	12.5"
Case 2 (12")	6"	6"
Case 3 (12")	12"	0"
		20 C



• 100ohm stripline + 70ohm microstrip

	Stripline (100Ω)	Ustrip (70Ω)
Case 1 (12.5")	0"	12.5"
Case 2 (12.5")	6.5"	6"
Case 3 (13")	13"	0"
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	(c)





Results

GOOD MARGIN

CTLE: ADC=1, zero = 1GHz, pole1 = 3GHz, pole2=9.95GHz, Cpad_tx: 2pF

• 70ohm stripline + 100ohm microstrip



• 100ohm stripline + 70ohm microstrip





Summary

- With TX_EQ and CTLE RX equalizations, it is demonstrated that there is enough solution space for different channel configurations, including impedance mismatch from the channel
- The channel simulation technology empower C-PHY designers to evaluate the designs with millions of bits in minutes
- New ADS modeling and simulation environment provides an easier, faster, and complete solution for C-PHY design exploration



KEYSIGHT TECHNOLOGIES