



A Power Amplifier Design Based on Wavetek Process Design Kits

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Sponsor:  **KEYSIGHT**
TECHNOLOGIES

What Can We Do for Customers...?

As a pure foundry provider, what can we do for our customer...?

Agenda

- Introduction of Wavetek (WTK)
- Overview of WTK process design kit
- Example of power amplifier design
 - General considerations on power amplifier design
 - Final stage and power cell design
 - Complete power amplifier design
- Summary

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INTRODUCTION OF WAVETEK (WTK) ○

Process Map

HBT

SH2

High Beta 120 for Excellent Linearity

SH1

High Beta 125 for Excellent Linearity

HBT1/2

High Linearity 3G/LTE/WiFi

HBT3

Medium Linearity GSM/GPRS/EDGE

HBT5

High Ruggedness PA

HBT6

Small Cell [12V operation]

pHEMT

ED25

LNA/PA/Infrastructure/
RF switch

ED15-00

mmWave/LNA/5G Cellular

ED15-01

5G Cellular/mmWave

PA25

Power pHEMT [8V]

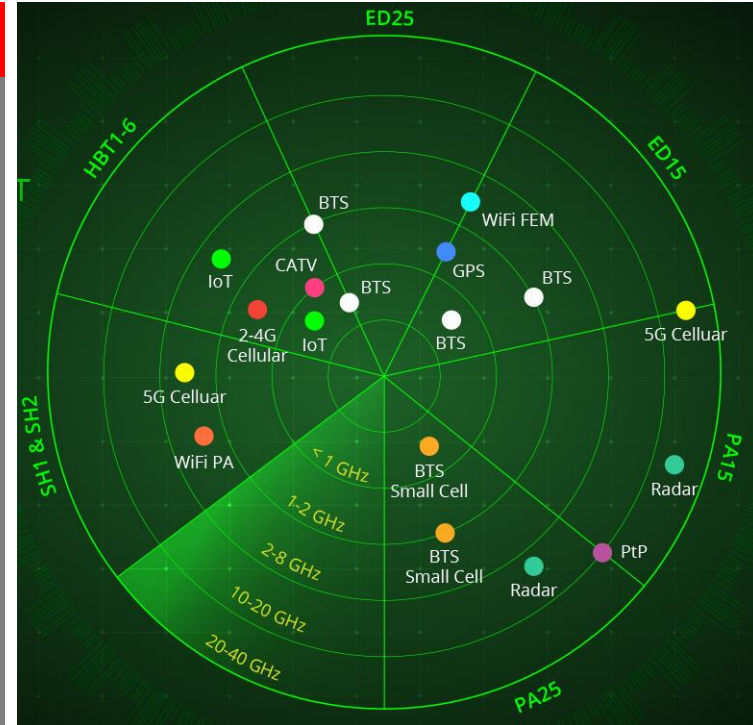
Others

IPD1

Polyimide

IPD2

Air-bridge



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OVERVIEW OF WTK PROCESS DESIGN KIT

Keysight Advance Design System (ADS)

A large graphic with a dark background and a red and grey diagonal split. It features the text "PATHWAVE Advanced Design System Premier High-Frequency and High Speed Design Platform (2020)" and "ADS 2020 is Released!". The Keysight Technologies logo and copyright information are at the bottom.

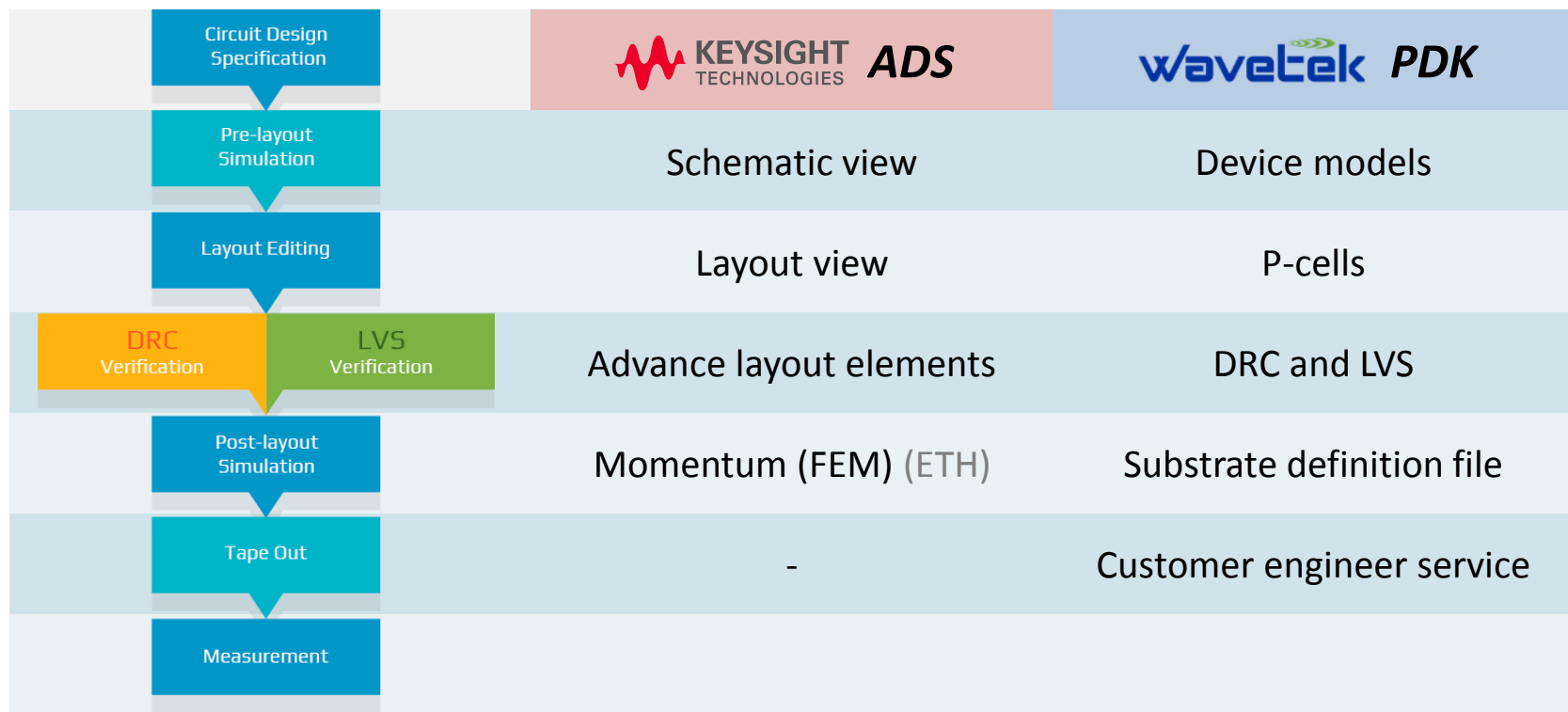
PATHWAVE
Advanced
Design System
Premier High-Frequency and
High Speed Design Platform (2020)

ADS 2020 is Released!

 KEYSIGHT
TECHNOLOGIES

© Keysight Technologies 1983-2019

One Stop RF Circuit Design Flow



Components in Schematic Library

The screenshot shows a schematic library window titled 'cell_1 [SH2_Demo_lib] cell_1.schem'. The interface includes a menu bar (File, Edit, Select, View, Insert), a toolbar with various icons, and a 'Parts' panel on the left. The main area displays a grid of components from the 'WTK_SH2_KIT' library. Five numbered callouts (1-5) point to specific categories:

- 1 Netlist Include Kit**: Points to the 'INCLUDE' component.
- 2 Active Devices**: Points to 'HBT' and 'Diode' components.
- 3 Passive Component**: Points to 'Resistor' and 'Inductor' components.
- 4 Traces**: Points to 'Microstrip lines' and 'Backside via.' components.
- 5 Others**: Points to 'ESD devices' and 'Customized components'.

At the bottom of the window, it says 'Select: Click and drag to select.'

SH2
wavetek
WTK_SH2_Include
Include
Version=TPM_VOP2_01
SH2_TEMP=25

Components in Layout Library

1 Active Devices

- HBT
- Diode

2 Passive Component

- Resistor
- Inductor
- Capacitor

3 Traces

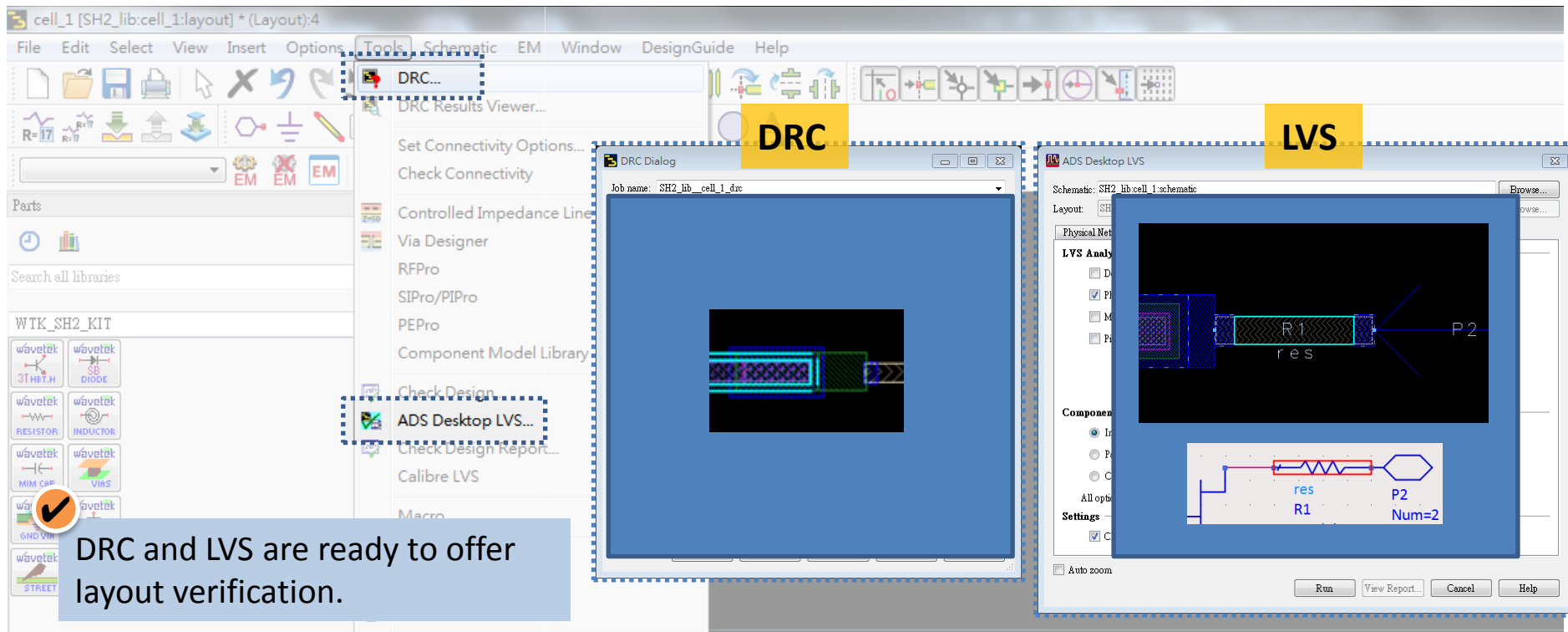
- Microstrip lines
- Backside via.
- Via
- Standard pad.

4 Others

- Dicing streets
- Text layouts

I LOVE
WAVETEK

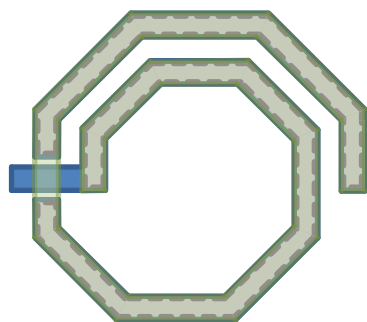
DRC / LVS (Layout Verification Tools)



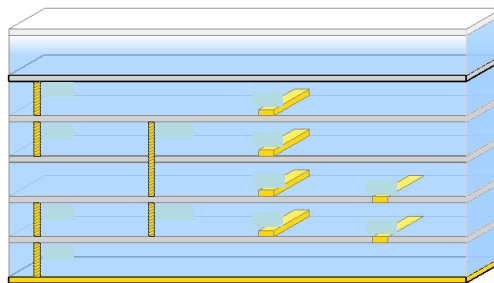
The screenshot displays a PCB design software interface with the following elements:

- Main Window:** Shows a layout file named "cell_1 [SH2_lib:cell_1:layout] * (Layout):4". The menu bar includes File, Edit, Select, View, Insert, Options, Tools, Schematic, EM, Window, DesignGuide, and Help. The Tools menu is open, highlighting "DRC..." and "ADS Desktop LVS...".
- Left Panel:** Contains a "Parts" list with a search bar and a library of components from WTK_SH2_KIT, including resistors, inductors, and capacitors.
- DRC Dialog:** A window titled "DRC Dialog" with "Job name: SH2_lib_cell_1_drc". It displays a 3D visualization of a PCB layout with a red and blue highlighted area.
- LVS Dialog:** A window titled "ADS Desktop LVS" showing a schematic diagram with a resistor labeled "R1 res" and a port labeled "P2". Below the schematic is a component model diagram with labels "res", "R1", and "P2 Num=2".
- Annotations:** Yellow boxes labeled "DRC" and "LVS" are placed over their respective dialog windows. A blue callout box at the bottom left contains the text: "DRC and LVS are ready to offer layout verification."

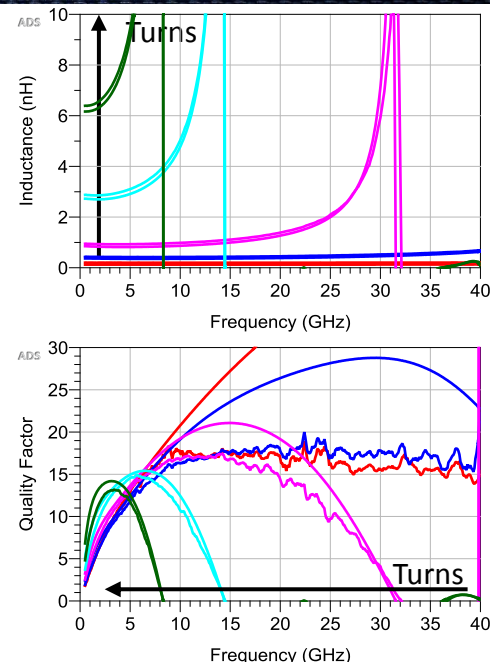
EM-Simulation on Momentum



Layout pattern



Substrate definition files



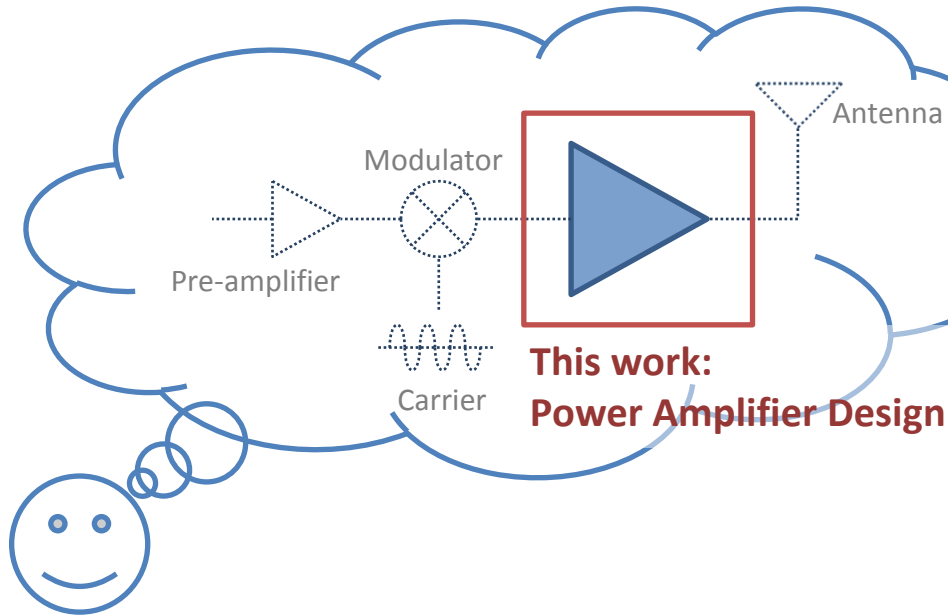
Measured (solid line) and simulated (dash line) inductance and quality factor with different turns.

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EXAMPLE OF POWER AMPLIFIER DESIGN

A Power Amplifier Design



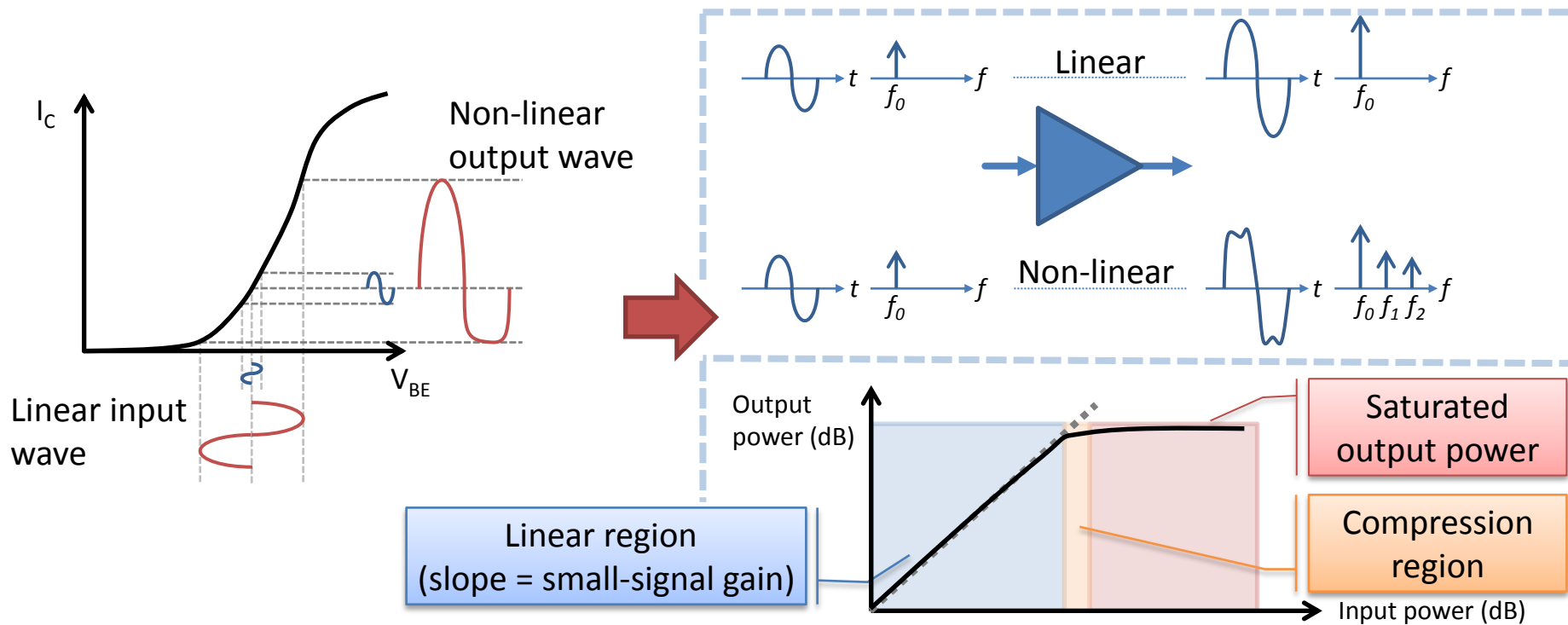
Considerations in power amplifier design

- **Linearity:** IP3, AM-AM/-PM conversion, ACLR...
- **Thermal:** electro-thermal interaction, thermal coupling effect

Performance of power amplifier design

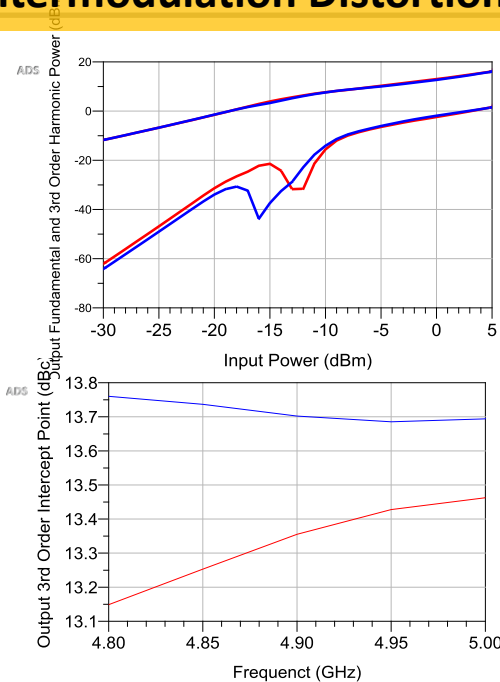
- Return loss
- Gain
- P_{1dB}
- IP3
- ...

Non-Linear Effect

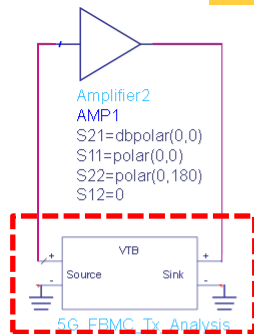


Modulation Issue

Intermodulation Distortion



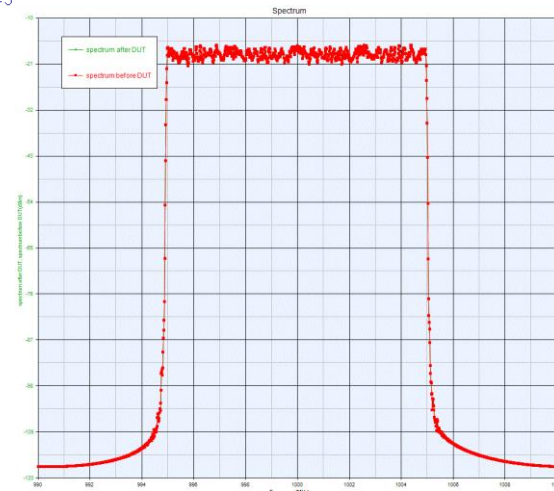
Verification Test Bench (VTB)



ENVELOPE

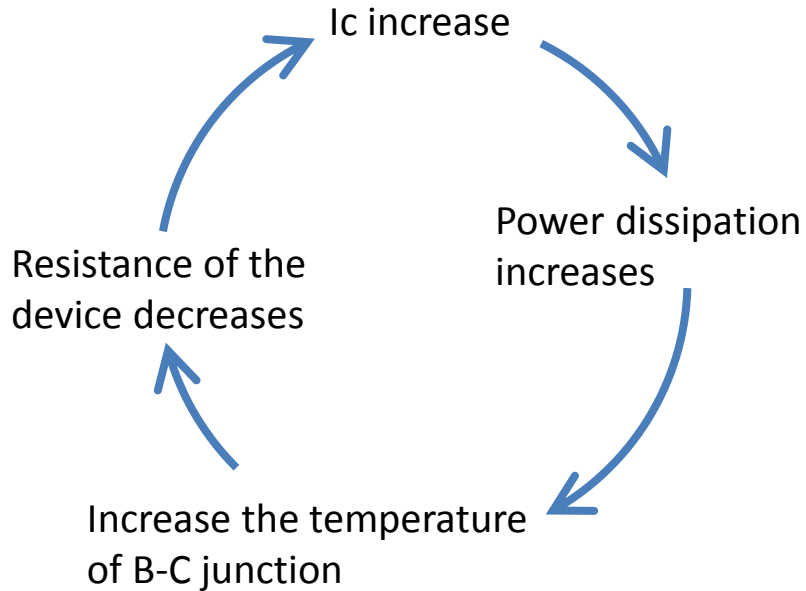
Envelope
VTB1_Env
Freq[1]=vtbFCarrier_Source
Order[1]=5

VTB1
FCarrier_In=1e+09 Hz
FCarrier_Out=1e+09 Hz
SignalPower=0.01 W
BaseSampleRate=1e+07 Hz
OversampleRatio=Ratio 2
IdleInterval=0 sec
ModType=QPSK
MirrorSignal=NO
GainImbalance=0
PhaseImbalance=0
I_OriginOffset=0
Q_OriginOffset=0
IQ_Rotation=0
PortZ[1]=50 Ohm
PortZ[2]=50 Ohm

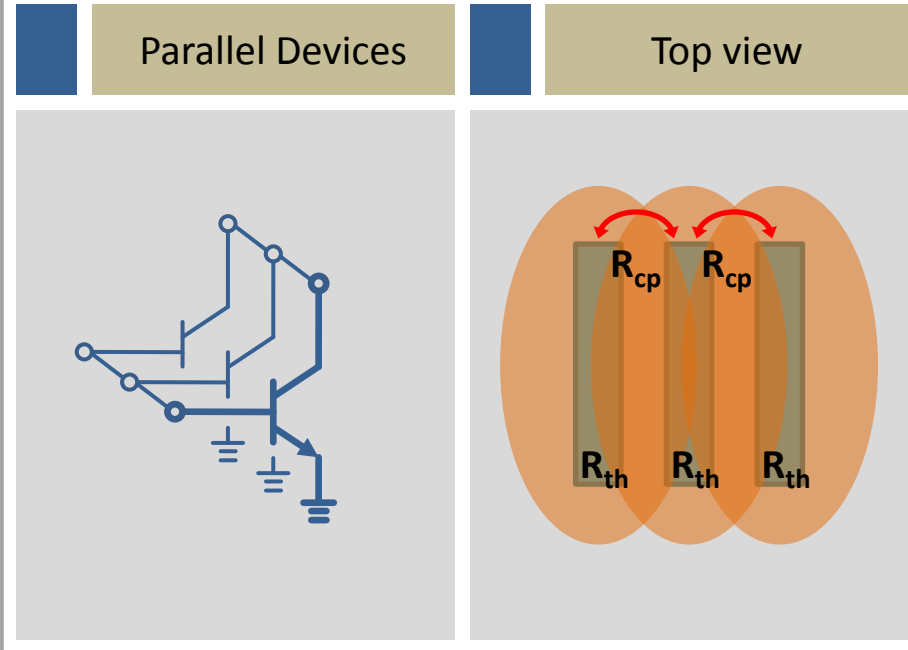


Thermal Issue in Power Cell

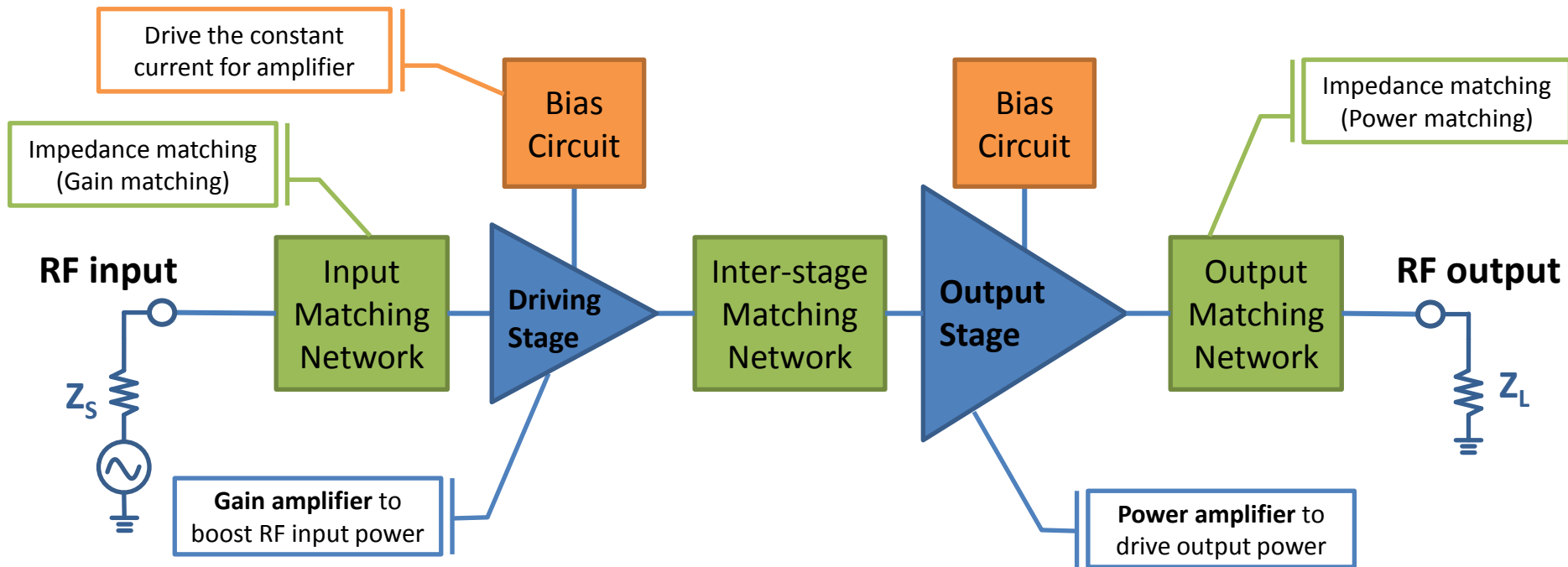
Electro-Thermal Interaction



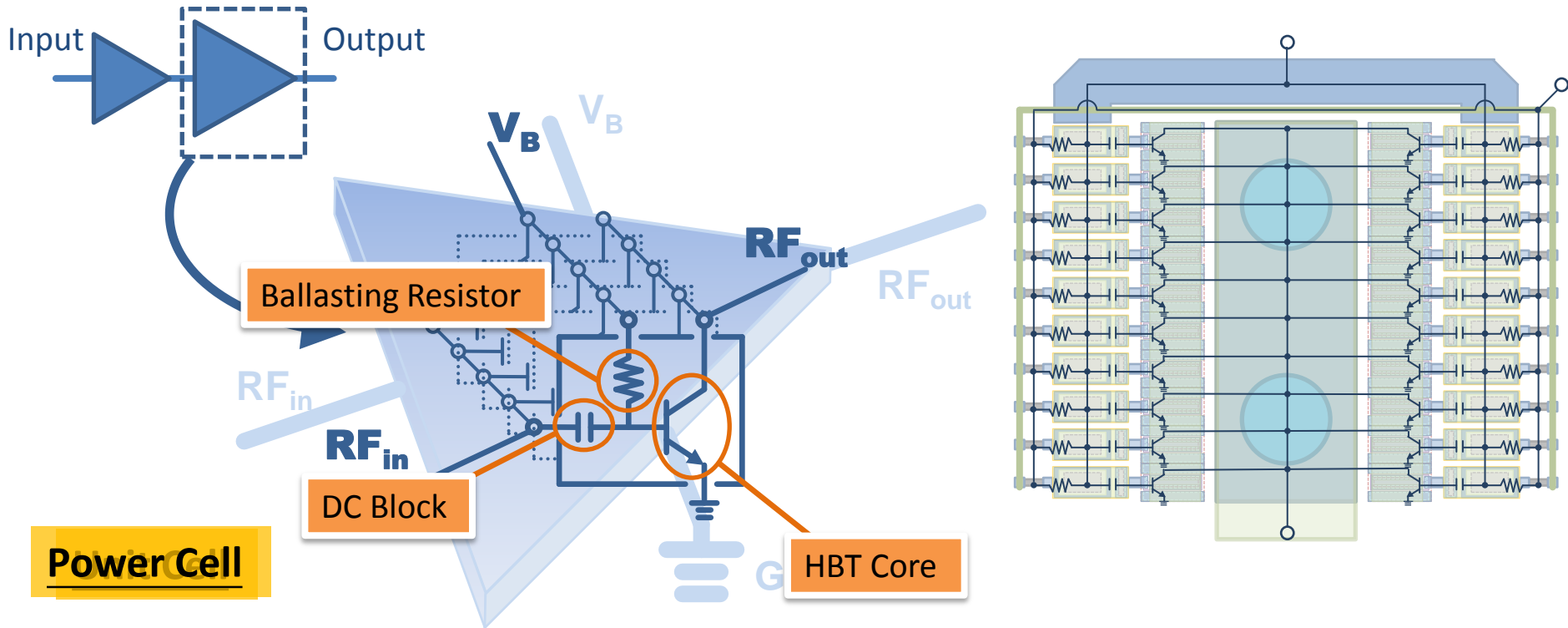
Thermal Coupling Effect



Block Diagram of Power Amplifier

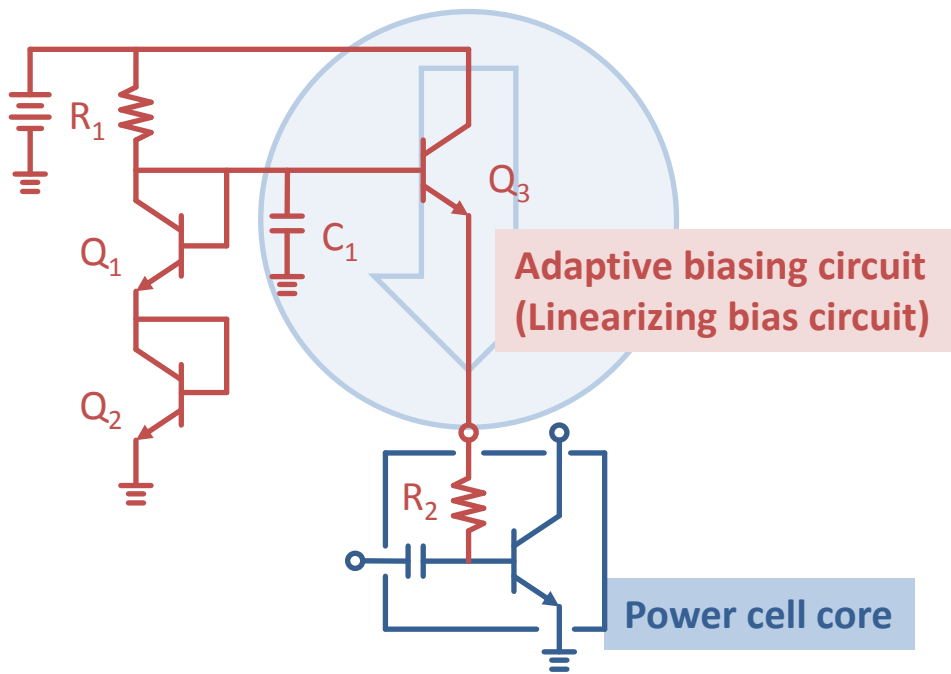


Power Cell



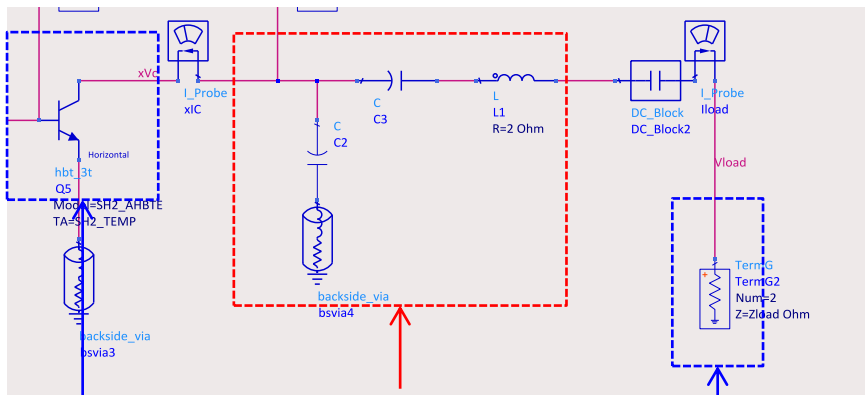
Power Cell

Biasing Circuit: Structure



Impedance Matching and Load Pull

Impedance Matching

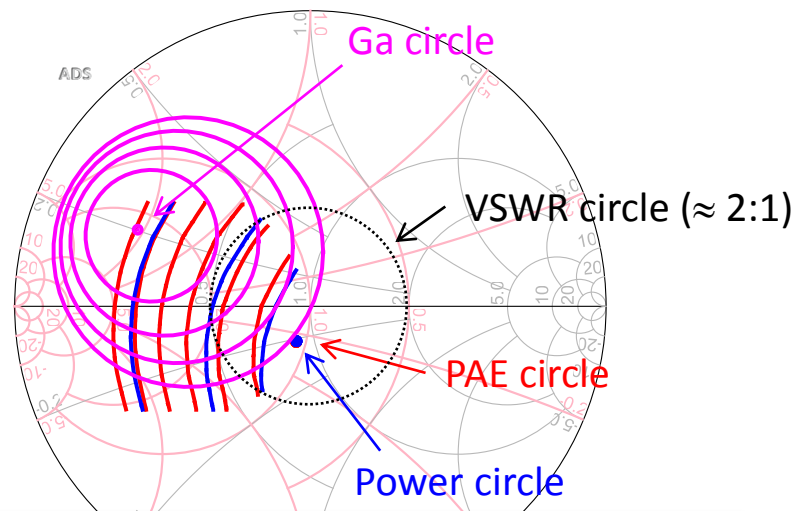


Device Impedance

Output matching network

Load Impedance (50 Ω)

Contours of PAE, Power and Gain



Optimized and trade amplifier performance between P_{out} , PAE, Ga and VSWR.

Pre-Layout and Post-Layout Simulation

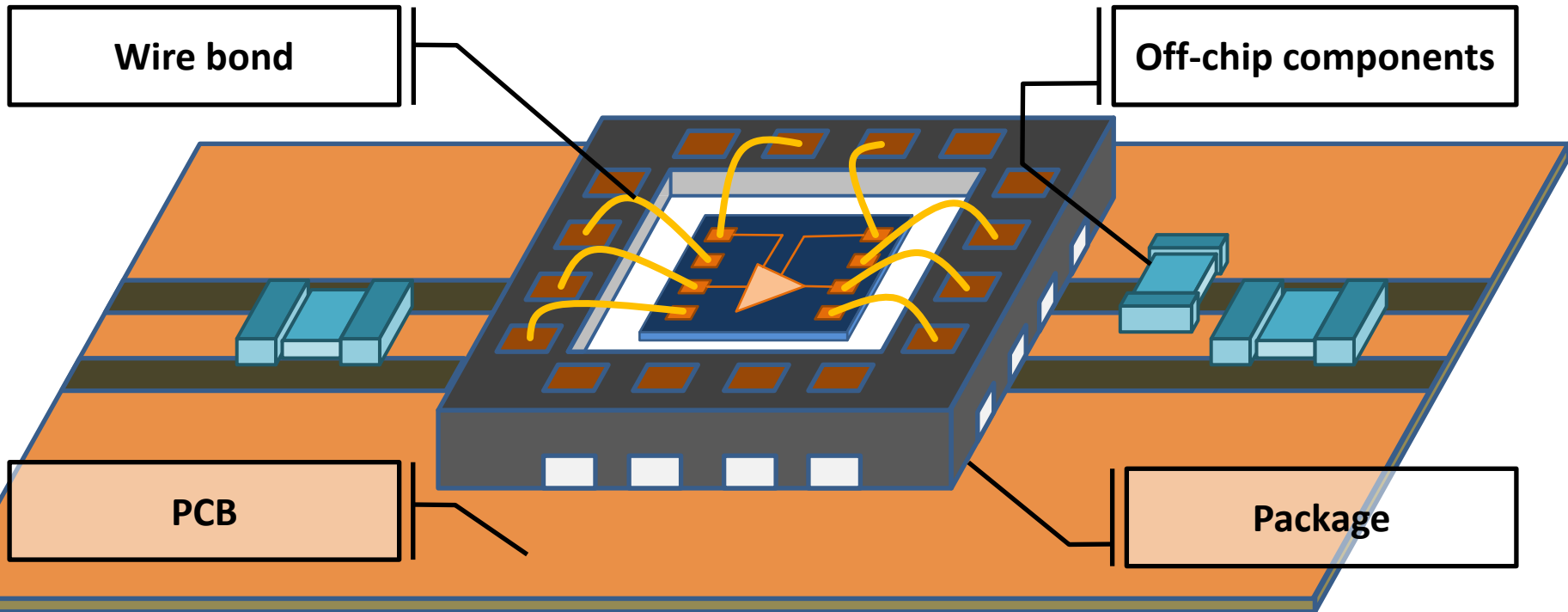
- **Pre-layout simulation**

- Using equivalent models.
- Coupling effect not considered.
- Less simulation time.

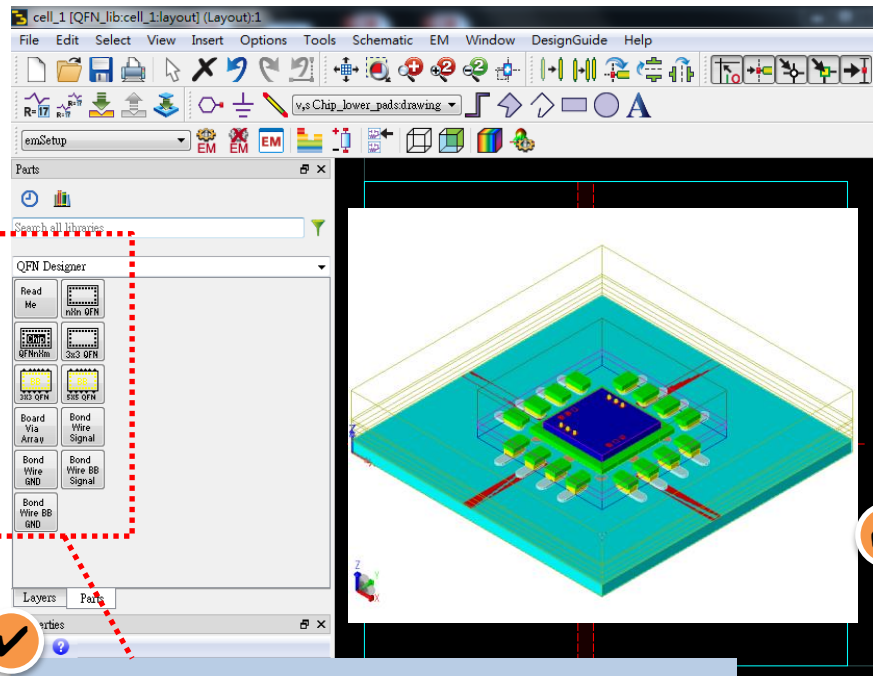
- **Post-layout (EM-) simulation**

- Performance extracted from the substrate definition file.
- Coupling effect considered.
- Taking more simulation time.

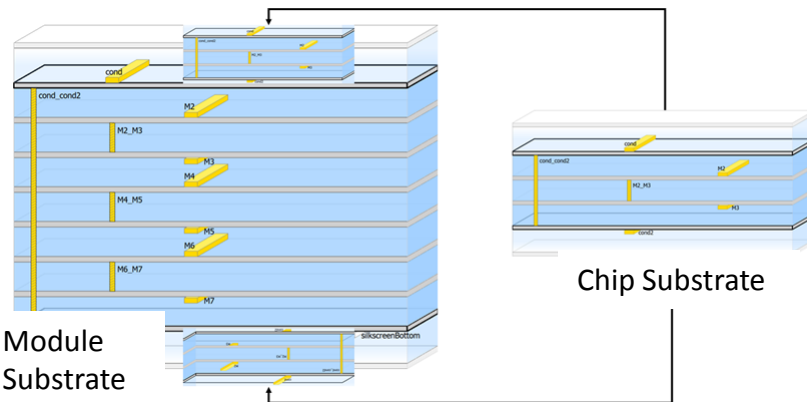
Off-Chip Elements



Smart Mount for Multi-Technology

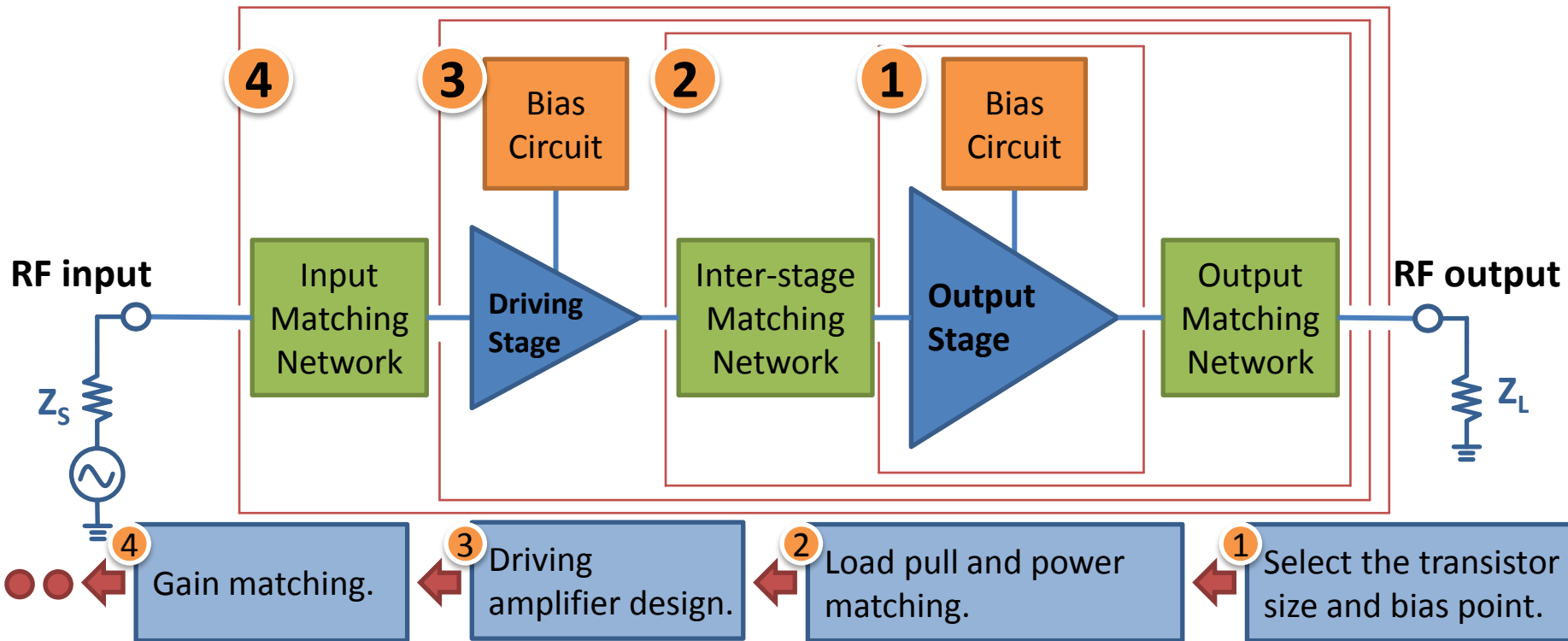


Reference demokit: QFN_Designer_V8

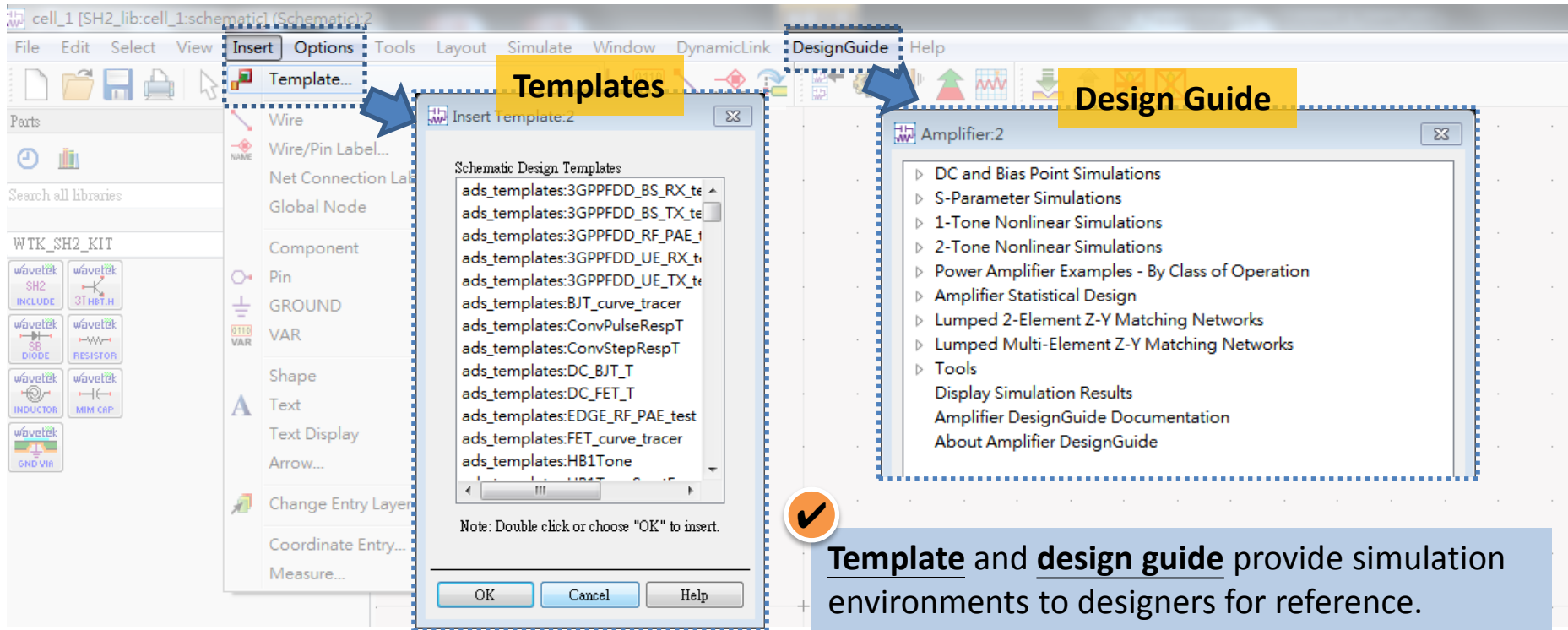


Smart Mount allows a component designed in one technology to be used in a design with a different technology.

Power Amplifier Design Flow




Test Bench from Design Guide



The screenshot displays the software interface with the following elements:

- Insert Menu:** Opened, showing options like Wire, Wire/Pin Label..., Net Connection Label..., Global Node, Component, Pin, GROUND, VAR, Shape, Text, Text Display, Arrow..., Change Entry Layer..., Coordinate Entry..., and Measure... A blue arrow points from the 'Template...' option to the 'Schematic Design Templates' dialog.
- Schematic Design Templates Dialog:** A list of templates including: ads_templates:3GPPFDD_BS_RX_te, ads_templates:3GPPFDD_BS_TX_te, ads_templates:3GPPFDD_RF_PAE_1, ads_templates:3GPPFDD_UE_RX_te, ads_templates:3GPPFDD_UE_TX_te, ads_templates:BJT_curve_tracer, ads_templates:ConvPulseRespT, ads_templates:ConvStepRespT, ads_templates:DC_BJT_T, ads_templates:DC_FET_T, ads_templates:EDGE_RF_PAE_test, ads_templates:FET_curve_tracer, and ads_templates:HB1Tone. A note at the bottom states: "Note: Double click or choose 'OK' to insert." Buttons for OK, Cancel, and Help are visible.
- Design Guide Dialog:** Titled 'Amplifier:2', it lists simulation and design resources:
 - ▷ DC and Bias Point Simulations
 - ▷ S-Parameter Simulations
 - ▷ 1-Tone Nonlinear Simulations
 - ▷ 2-Tone Nonlinear Simulations
 - ▷ Power Amplifier Examples - By Class of Operation
 - ▷ Amplifier Statistical Design
 - ▷ Lumped 2-Element Z-Y Matching Networks
 - ▷ Lumped Multi-Element Z-Y Matching Networks
 - ▷ Tools
 - Display Simulation Results
 - Amplifier DesignGuide Documentation
 - About Amplifier DesignGuideA blue arrow points from the 'DesignGuide' menu item to this dialog.

 **Template and design guide** provide simulation environments to designers for reference.

Device Analysis: DC Simulation

BJT Curve Tracer

Generates IV curves, computes Gm versus bias, and optimal bias for Class A operation.

wavetek SH2
 WTK_SH2_include
 Include
 Version=TPM_VOP2_01
 SH2_TEMP=25

PARAMETER SWEEP

ParamSweep
 Sweep1
 SweepVar="IBB"
 SimInstanceName[1]="DC1"
 SimInstanceName[2]="Sweep2"
 SimInstanceName[3]=
 SimInstanceName[4]=
 SimInstanceName[5]=
 SimInstanceName[6]=
 Start=500 uA
 Stop=8000 uA
 Step=500 uA

DC

DC
 DC1
 SweepVar="VCE"
 Start=VCE_Start
 Stop=VCE_Stop
 Step=VCE_Step

PARAMETER SWEEP

ParamSweep
 Sweep2
 SweepVar="VCE"
 SimInstanceName[1]="AC1"
 SimInstanceName[2]=
 SimInstanceName[3]=
 SimInstanceName[4]=
 SimInstanceName[5]=
 SimInstanceName[6]=
 Start=VCE_Start

AC

AC
 AC1

VAR

VAR2
 VCE =0 V
 IBB =0 A
 Rload = 50 _ohms

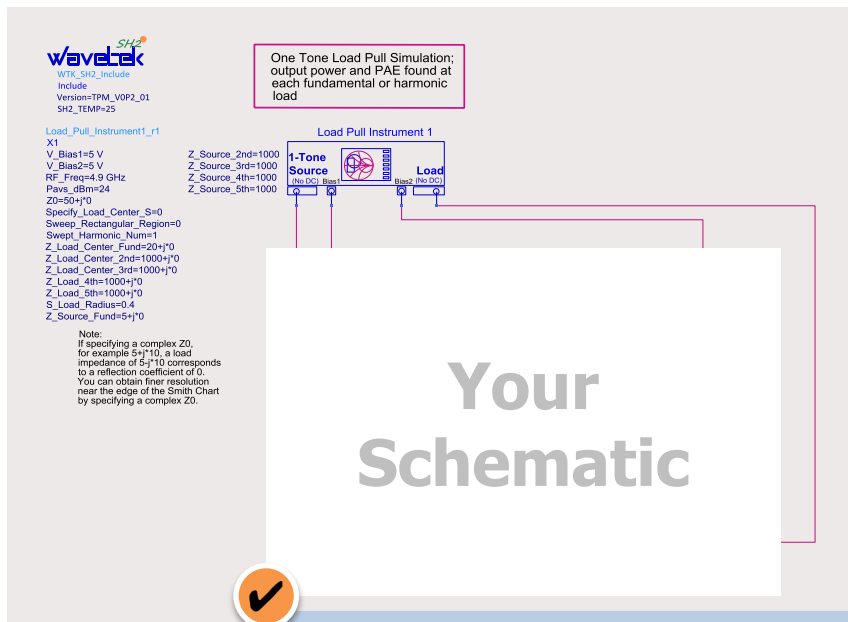
VAR

VAR1
 VCE_Start=0
 VCE_Stop=13
 VCE_Step=0.2

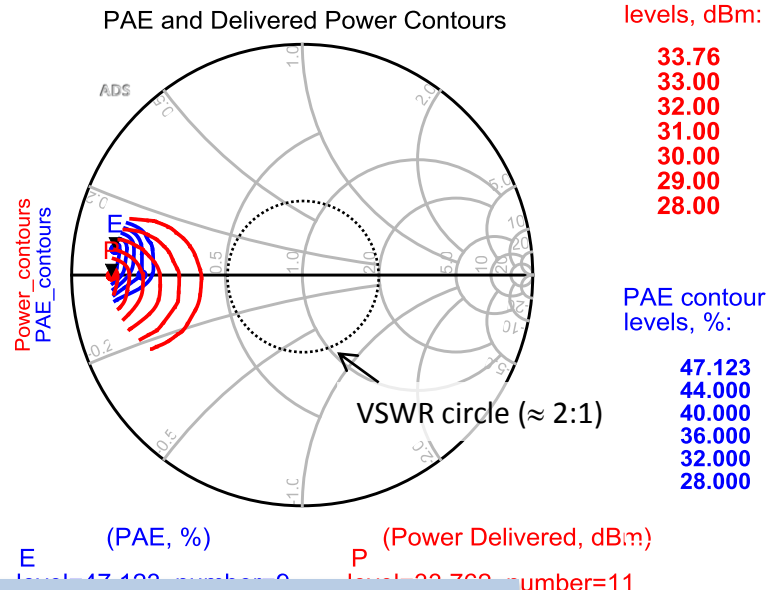
Set base current and collector voltage sweep limits and frequency at which the transconductance Gm will be calculated, as needed.

Reference design guide: **BJT I-V curve, Class A Power, Eff., Load, Gm vs. Bias**

Device Analysis: Load Pull



System Reference Impedance Z0:
 A Rho of 0 corresponds to a load impedance of conj(Z0).



- Power contour levels, dBm:
- 33.76
 - 33.00
 - 32.00
 - 31.00
 - 30.00
 - 29.00
 - 28.00
- PAE contour levels, %:
- 47.123
 - 44.000
 - 40.000
 - 36.000
 - 32.000
 - 28.000



Reference design guide: **Load Pull – PAE, Output Power Contours**

Device Analysis: Stability

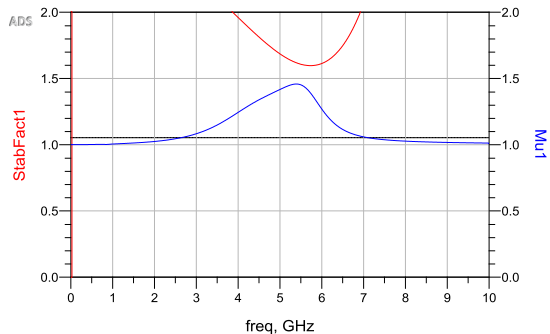
Mu and Stability Factor



StabFact
StabFact1
StabFact1=stab_fact(S)



Mu
Mu1
Mu1=mu(S)



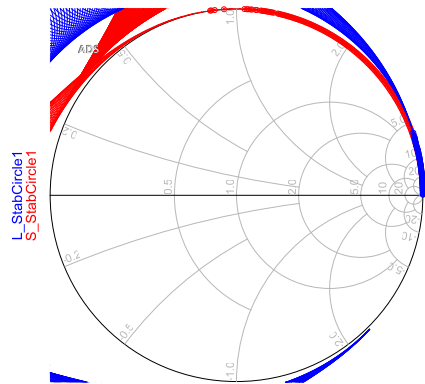
Stability Circle



S_StabCircle
S_StabCircle1
S_StabCircle1=s_stab_circle(S,51)

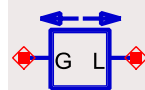


L_StabCircle
L_StabCircle1
L_StabCircle1=l_stab_circle(S,51)



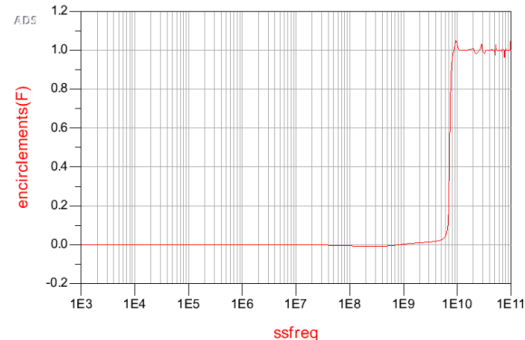
indep(S_StabCircle1) (0.000 to 51.000)
indep(L_StabCircle1) (0.000 to 51.000)

Winslow Stability Probe (WSProbe)

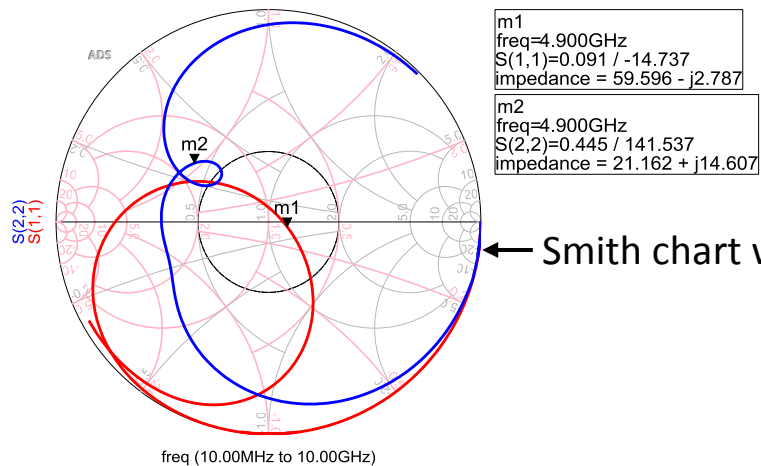


WSProbe
WSP1

ADS 2020
new function!

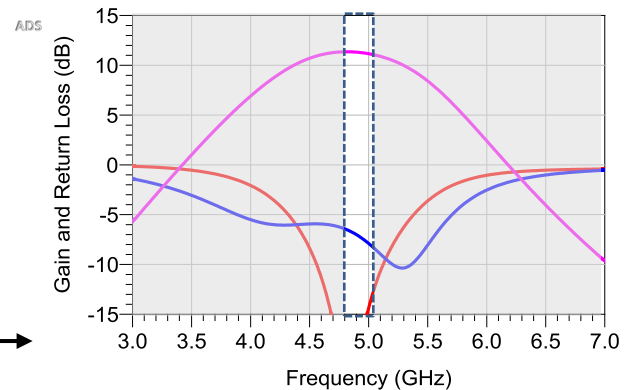


Simulation: S-Parameter



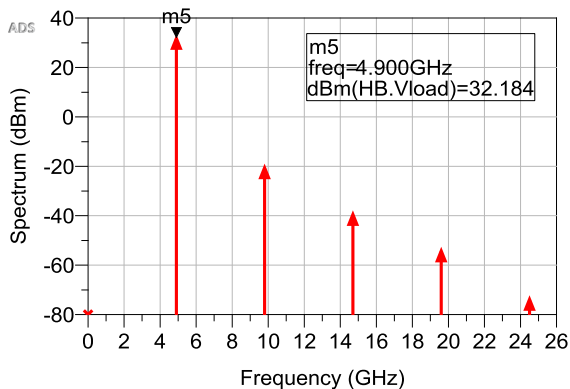
← Smith chart with S_{11} and S_{22}

Input / output return loss and gain →

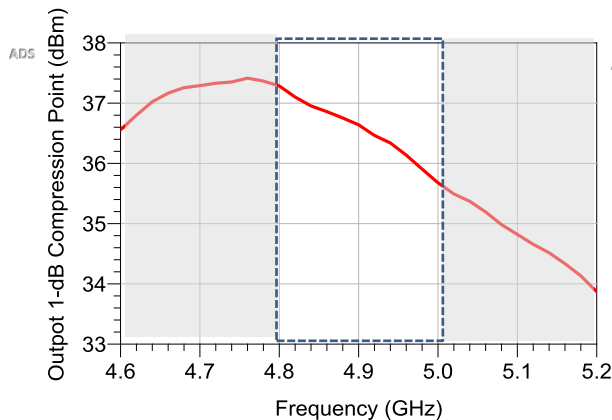


Simulation: Harmonic Balance

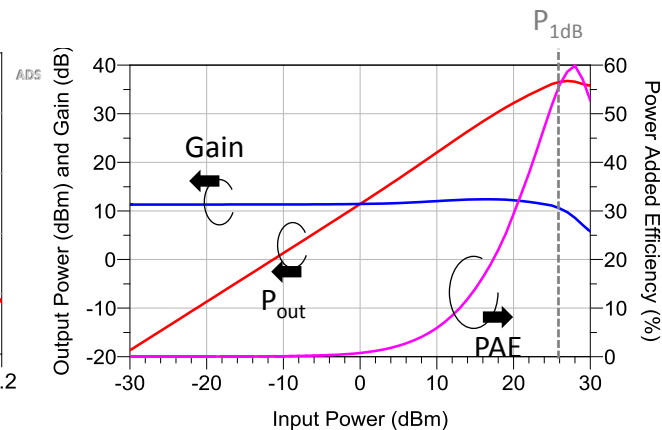
RF Spectrum



OP_{1dB} vs. Frequency



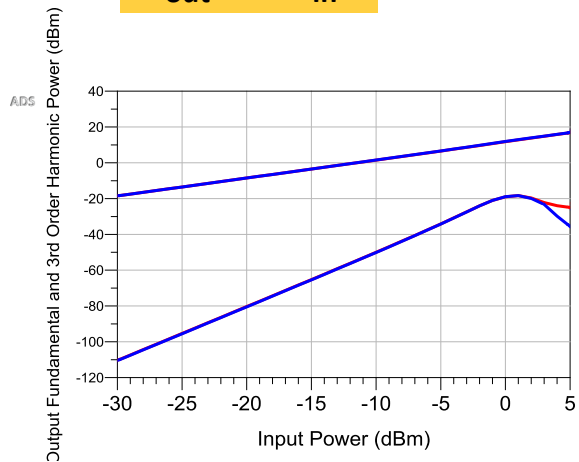
P_{out}, Gain and PAE vs. Frequency



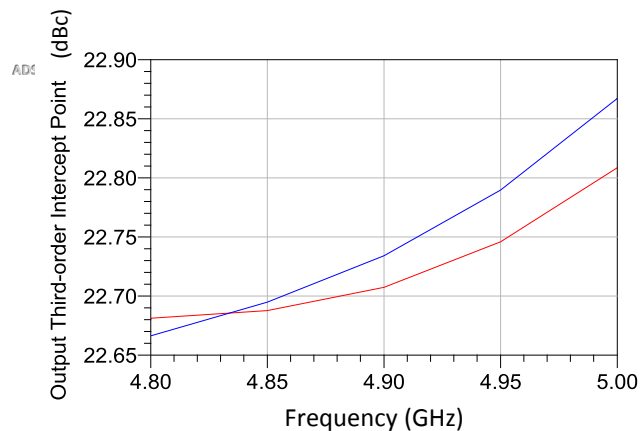
RF Frequency: 4.9 GHz

Simulation: Two-Tone and Modulation

P_{out} vs. P_{in}



OIP3 vs. Frequency



Complete Power Amplifier Design

Your Schematic



Complete your power amplifier!

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SUMMARY

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1. The power amplifier is a critical component in the RF transmission system. This work demonstrates a step-to-step power amplifier design and raises several considerations for new designers.
2. To provide a friendly circuit design environment, [Wavetek](#) and [Keysight](#) would continually provide improved PDK solutions to all partners.

Welcome to Visit Wavetek Website



<http://www.wtkmicro.com>

Thank you for your listening ○