A Power Amplifier Design Based on Wavetek Process Design Kits

Min-Li Chou Ph.D. / Wavetek (聯穎光電)

Sponsor: KEYSIGHT TECHNOLOGIES

What Can We Do for Customers…?

As a pure foundry provider, what can we do for our customer…?

Agenda

- Introduction of Wavetek (WTK)
- Overview of WTK process design kit
- Example of power amplifier design
  - General considerations on power amplifier design
  - Final stage and power cell design
  - Complete power amplifier design
- Summary

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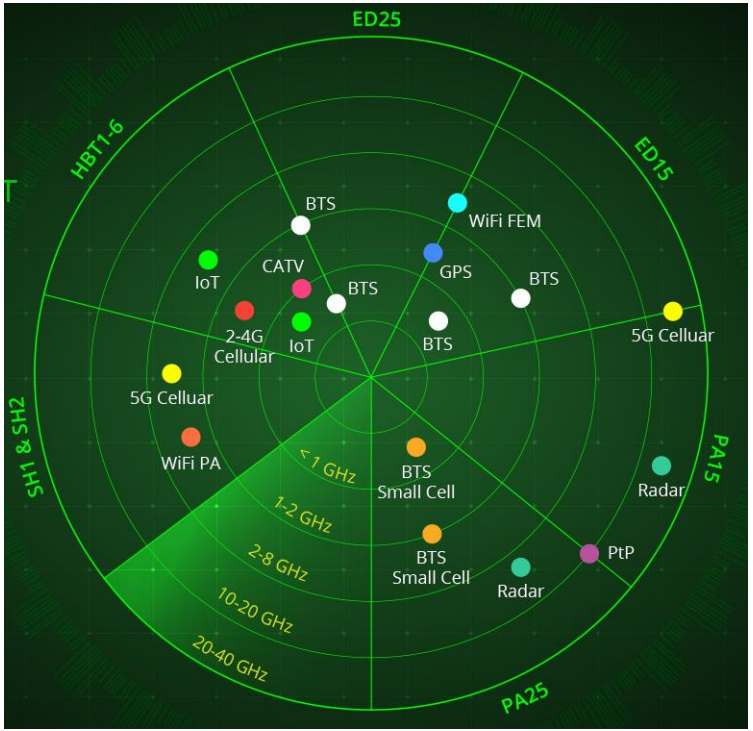
INTRODUCTION OF WAVETEK (WTK)

Process Map

HBT	pHEMT	Others
SH2 High Beta 120 for Excellent Linearity	**ED25** LNA/PA/Infrastructure/ RF switch	**IPD1** Polyimide
SH1 High Beta 125 for Excellent Linearity	**ED15-00** mmWave/LNA/5G Cellular	
HBT1/2 High Linearity 3G/LTE/WiFi	**ED15-01** 5G Cellular/mmWave	**IPD2** Air-bridge
HBT3 Medium Linearity GSM/GPRS/EDGE	**PA25** Power pHEMT [8V]	
HBT5 High Ruggedness PA		
HBT6 Small Cell [12V operation]		



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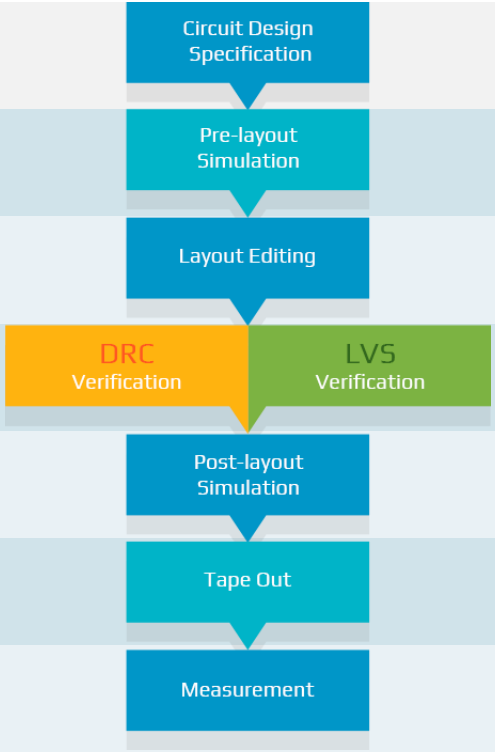
OVERVIEW OF WTK PROCESS DESIGN KIT

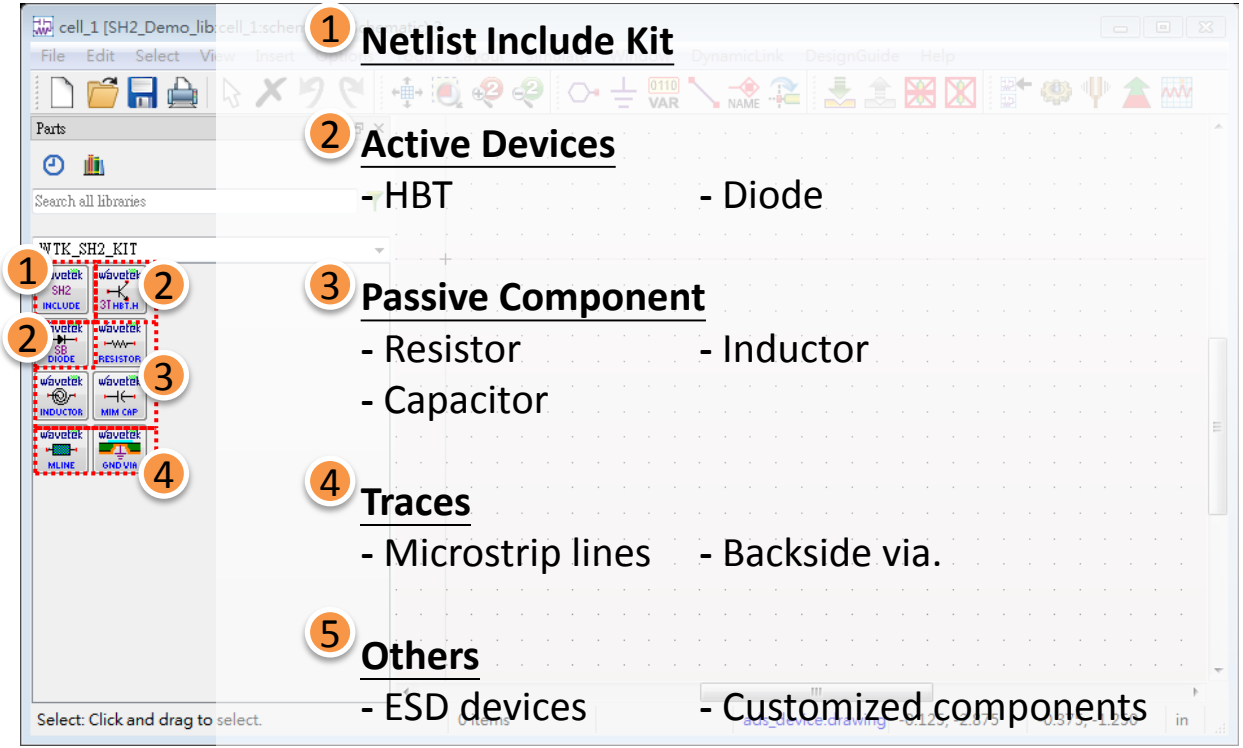
Keysight Advance Design System (ADS)

One Stop RF Circuit Design Flow



KEYSIGHT TECHNOLOGIES ADS	Wavetek PDK
Schematic view	Device models
Layout view	P-cells
Advance layout elements	DRC and LVS
Momentum (FEM) (ETH)	Substrate definition file
-	Customer engineer service

Components in Schematic Library



1. **Netlist Include Kit**

2. **Active Devices**
   - HBT
   - Diode

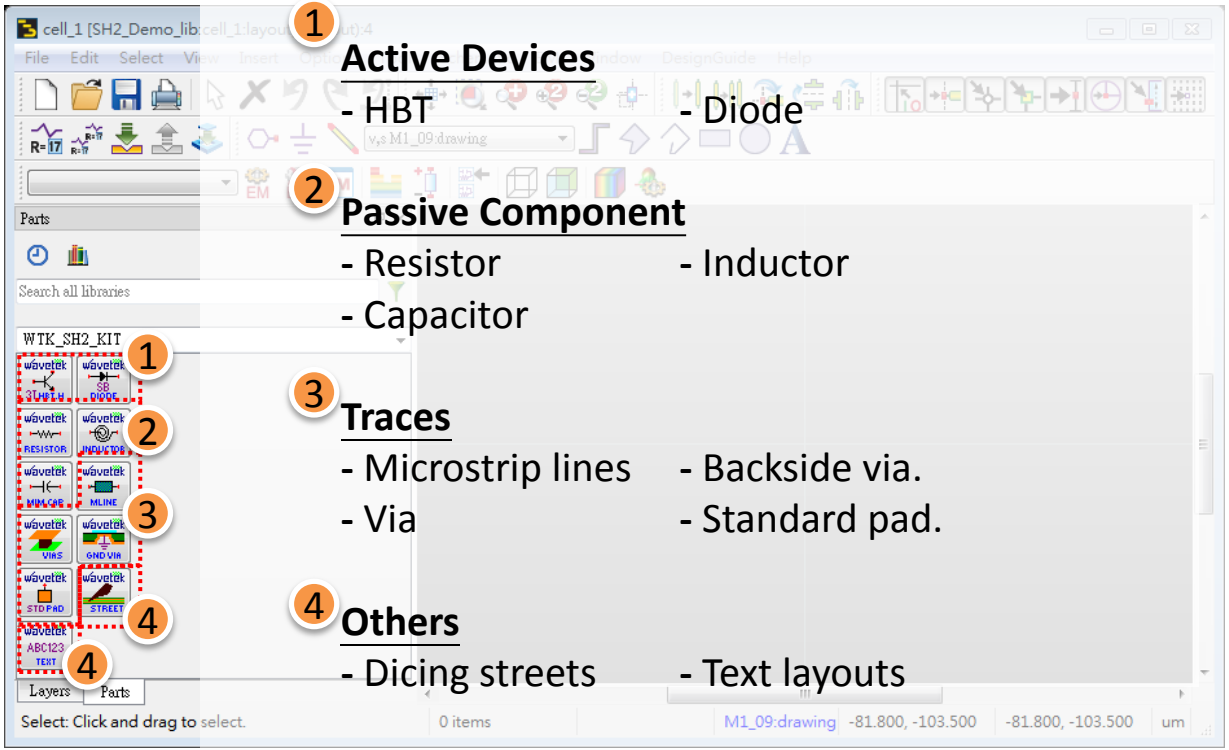
3. **Passive Component**
   - Resistor
   - Inductor
   - Capacitor

4. **Traces**
   - Microstrip lines
   - Backside via.

5. **Others**
   - ESD devices
   - Customized components

WTK_SH2_Include
Include
Version=TPM_V0P2_01
SH2_TEMP=25

Components in Layout Library



1 **Active Devices**

- HBT
- Diode

2 **Passive Component**

- Resistor
- Inductor
- Capacitor

3 **Traces**

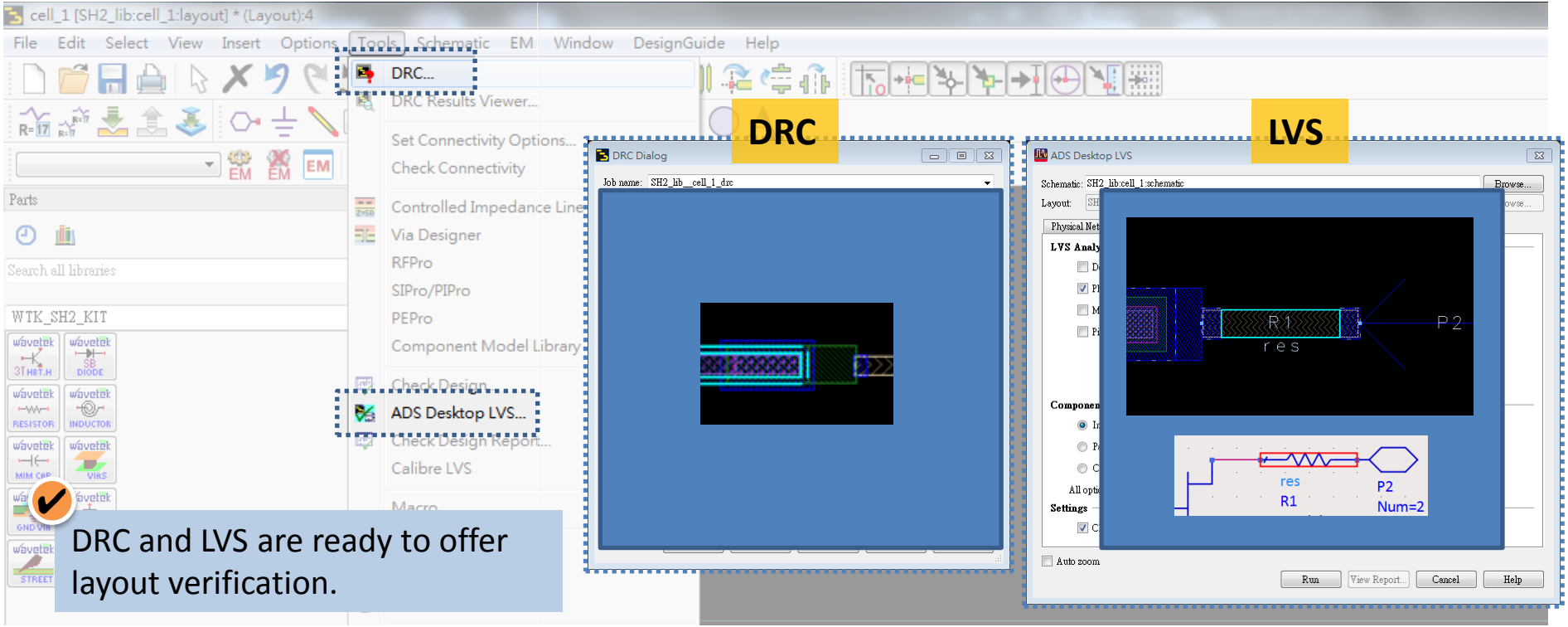
- Microstrip lines
- Backside via.
- Via
- Standard pad.

4 **Others**

- Dicing streets
- Text layouts

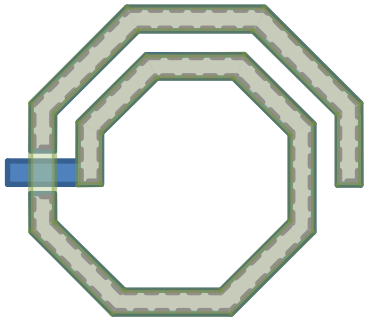
I LOVE WAVETEK

DRC / LVS (Layout Verification Tools)

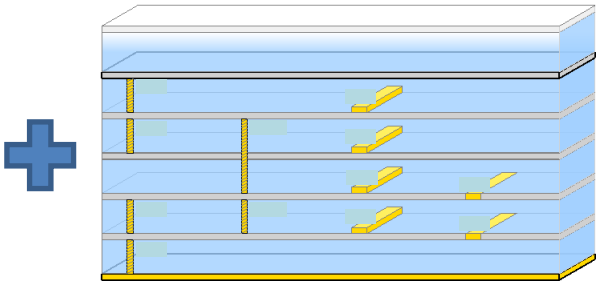


DRC and LVS are ready to offer layout verification.

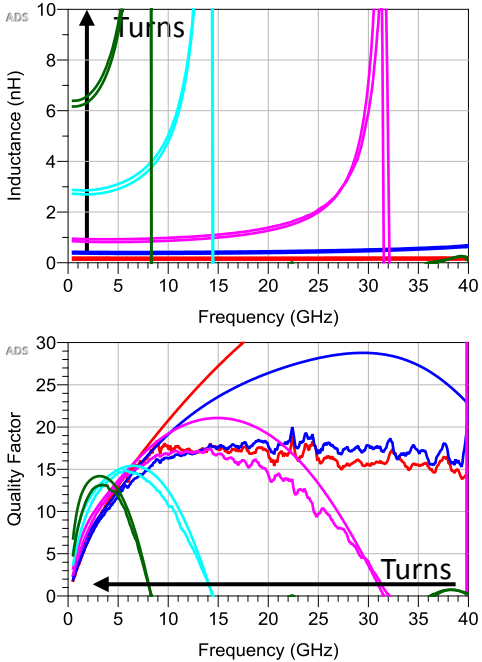
EM-Simulation on Momentum



Layout pattern



Substrate definition files



Measured (solid line) and simulated (dash line) inductance and quality factor with different turns.

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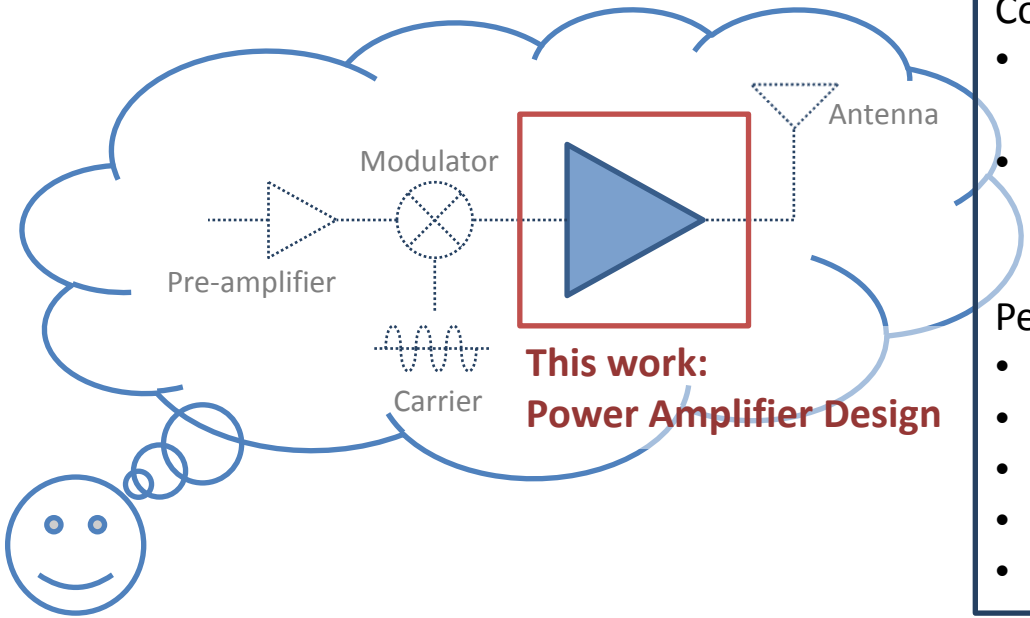
EXAMPLE OF POWER AMPLIFIER DESIGN

A Power Amplifier Design



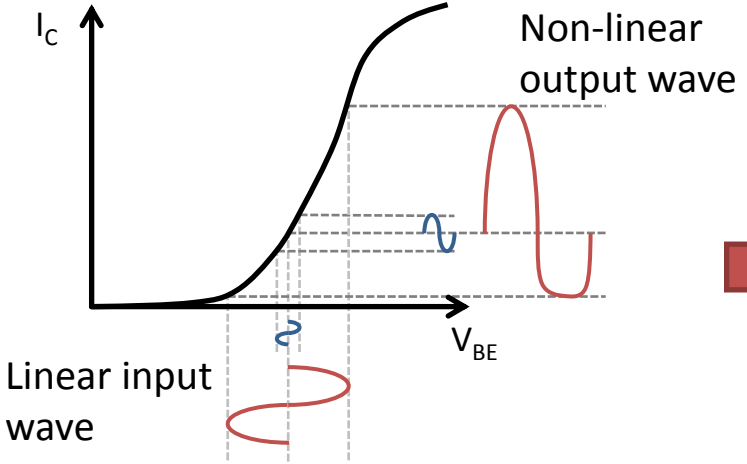
Considerations in power amplifier design

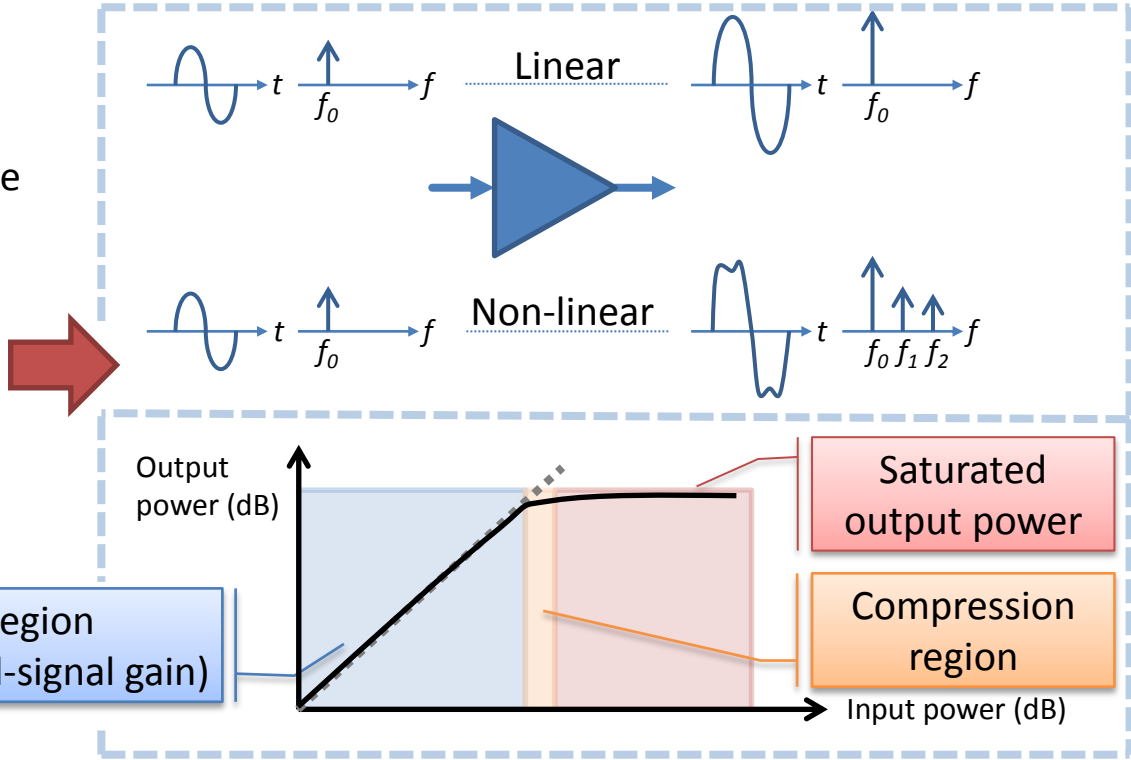
- **Linearity**: IP3, AM-AM/-PM conversion, ACLR…
- **Thermal**: electro-thermal interaction, thermal coupling effect

Performance of power amplifier design

- Return loss
- Gain
- P_{1dB}
- IP3
- …

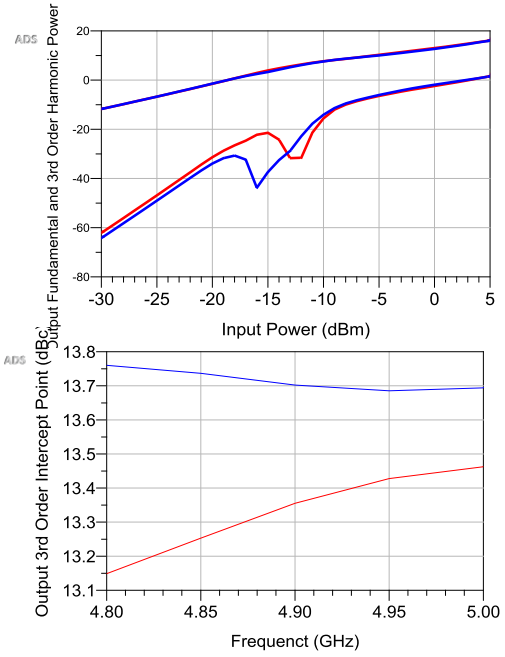
Non-Linear Effect



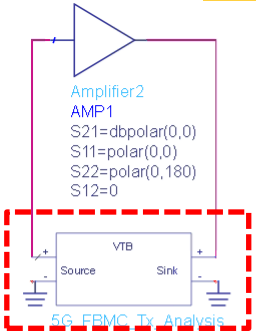


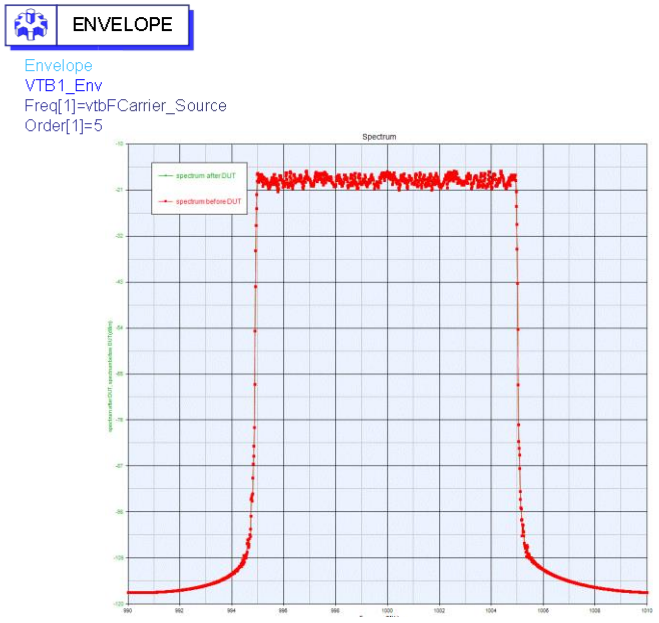
Modulation Issue

Intermodulation Distortion



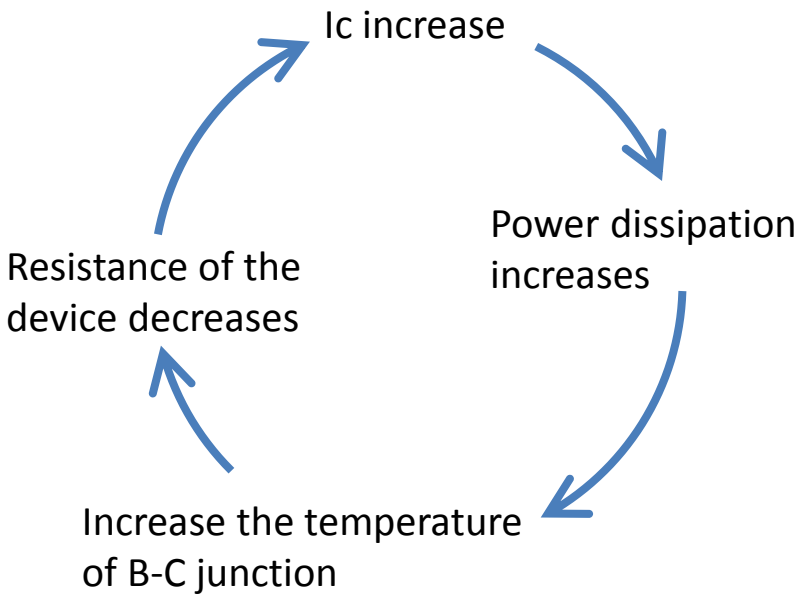
Verification Test Bench (VTB)





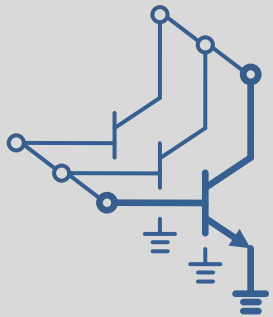
Thermal Issue in Power Cell

Electro-Thermal Interaction

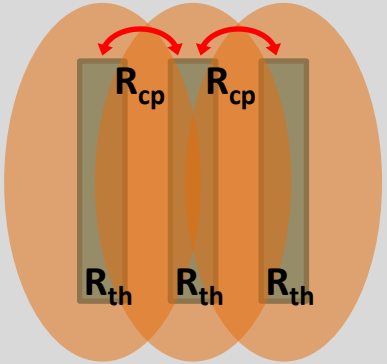


Thermal Coupling Effect

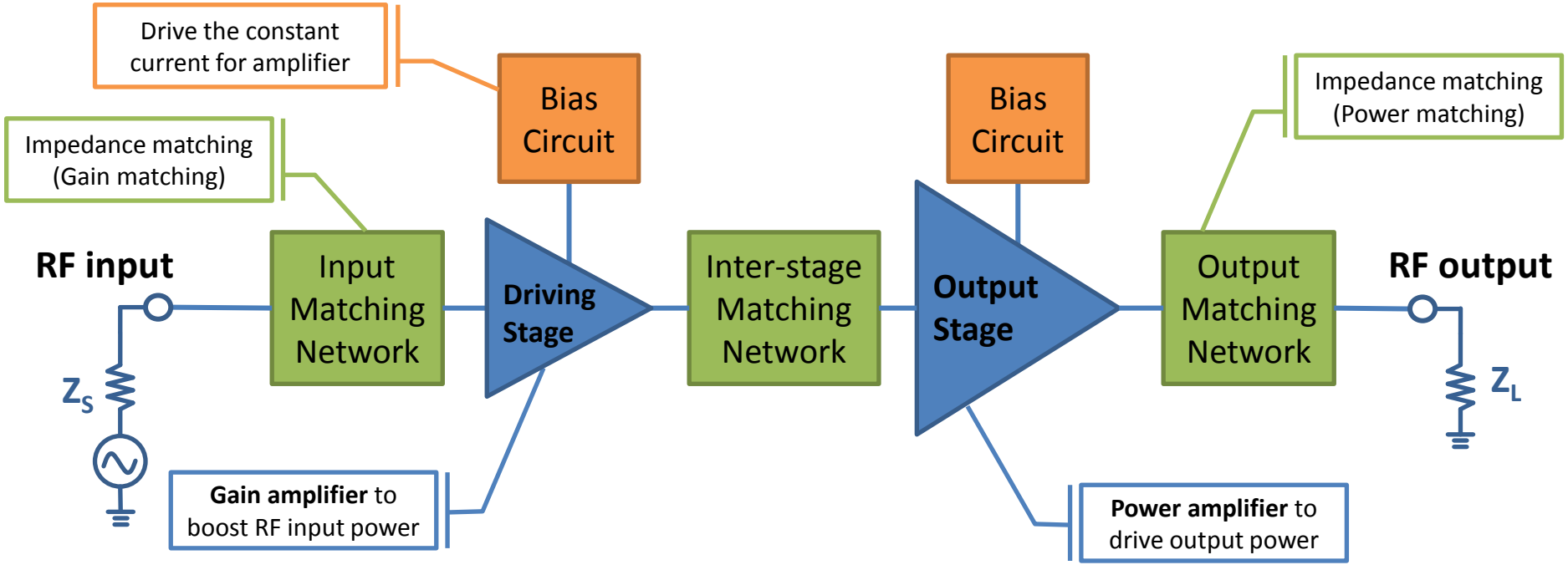
Parallel Devices



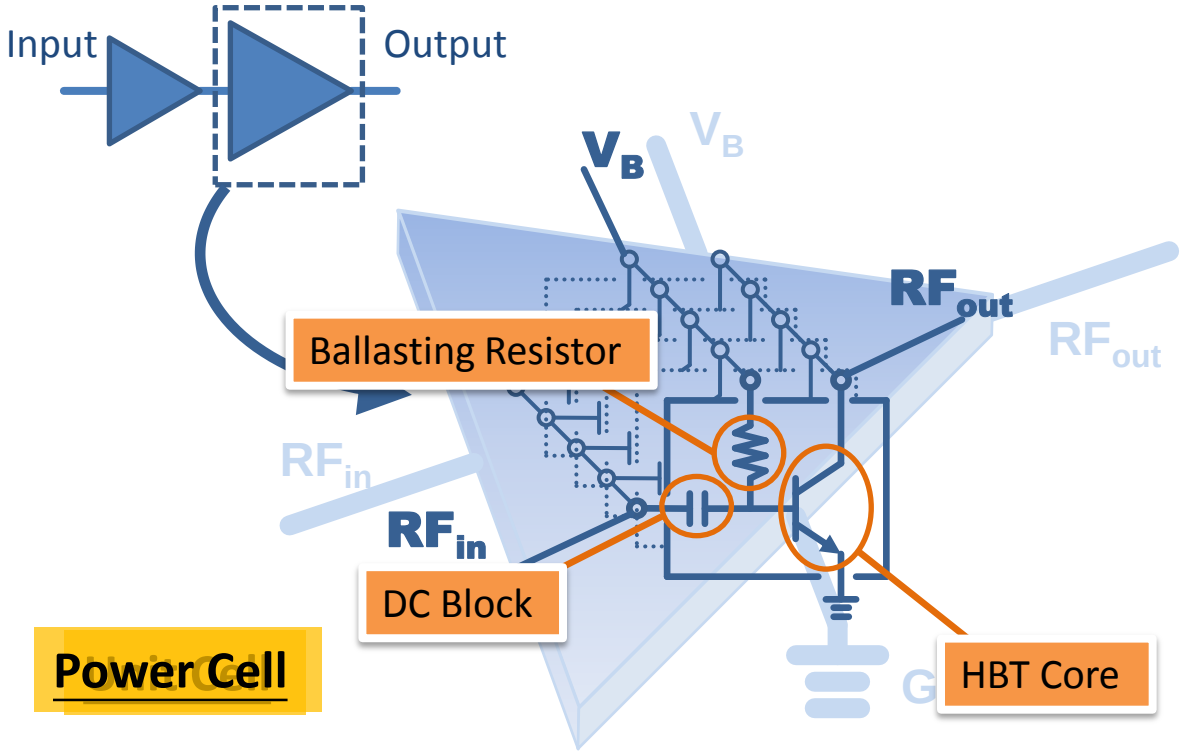
Top view

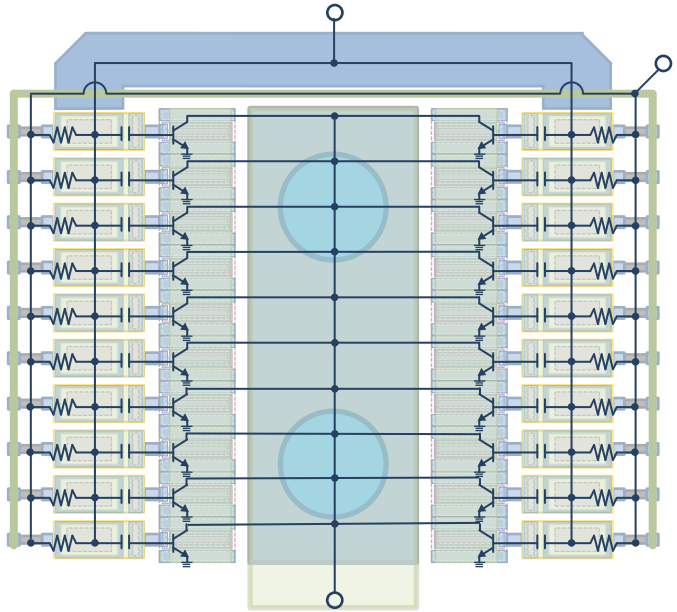


Block Diagram of Power Amplifier

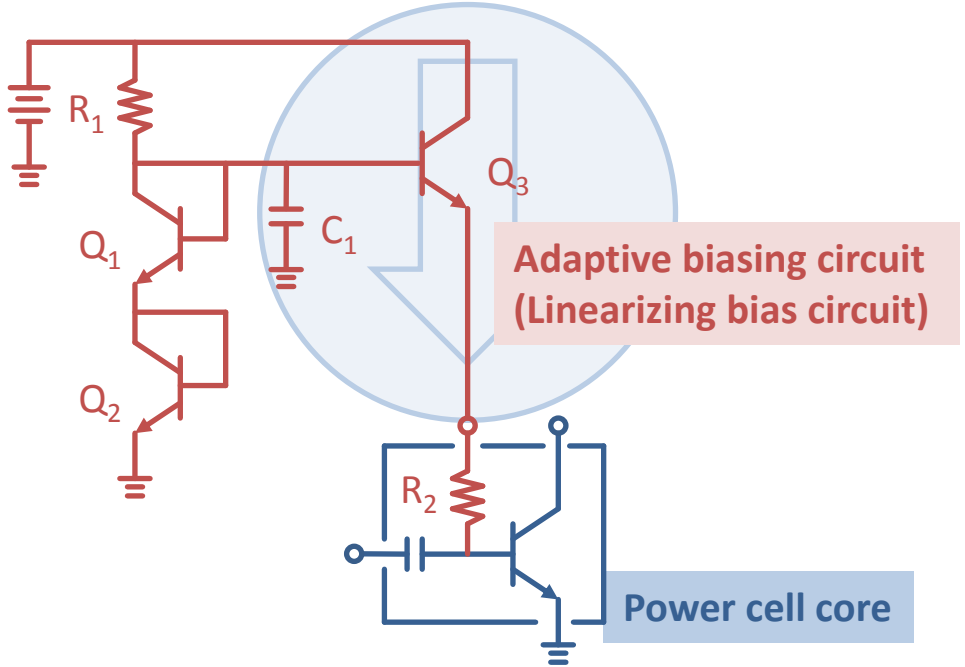


Power Cell



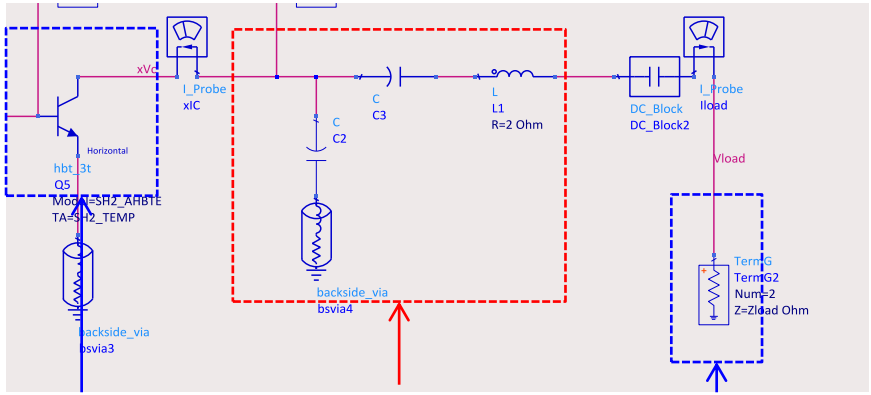


Biasing Circuit: Structure



Impedance Matching and Load Pull

Impedance Matching

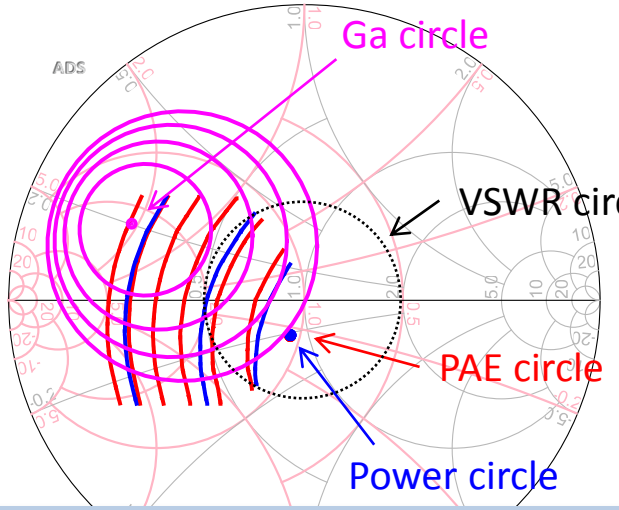


Device Impedance

Output matching network

Load Impedance (50 Ω)

Contours of PAE, Power and Gain



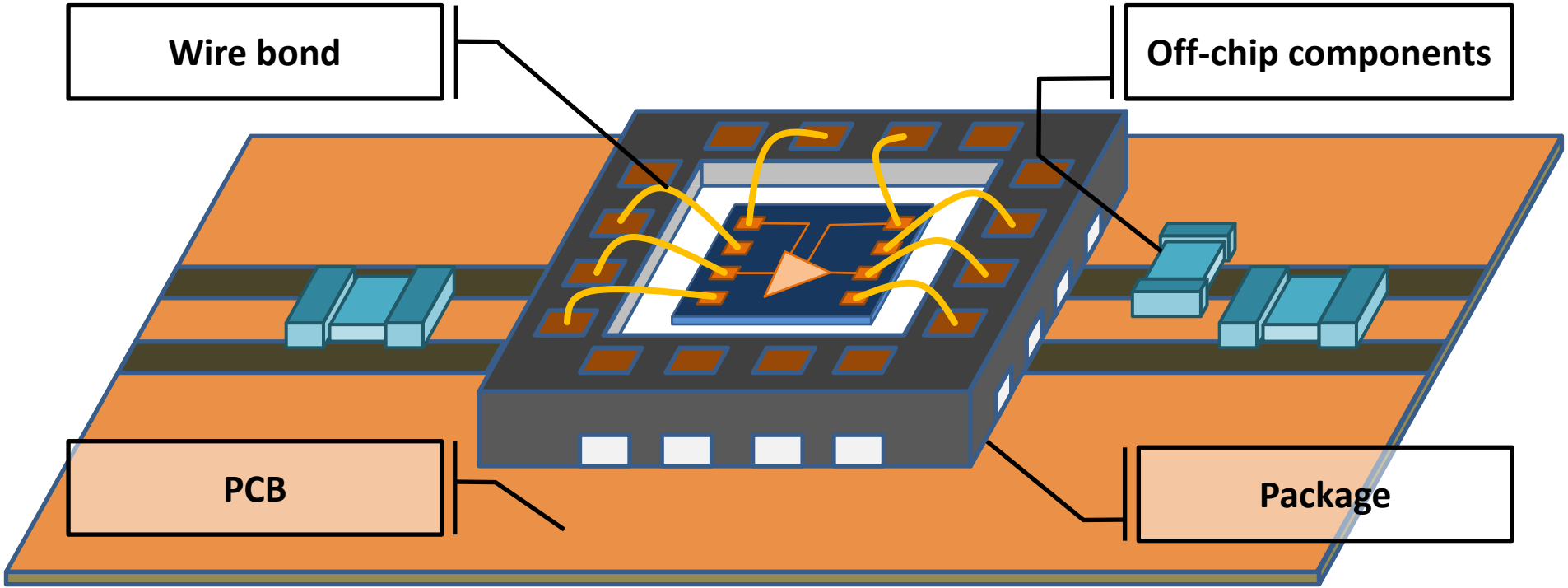
✔ Optimized and trade amplifier performance between P_{out}, PAE, Ga and VSWR.

Pre-Layout and Post-Layout Simulation

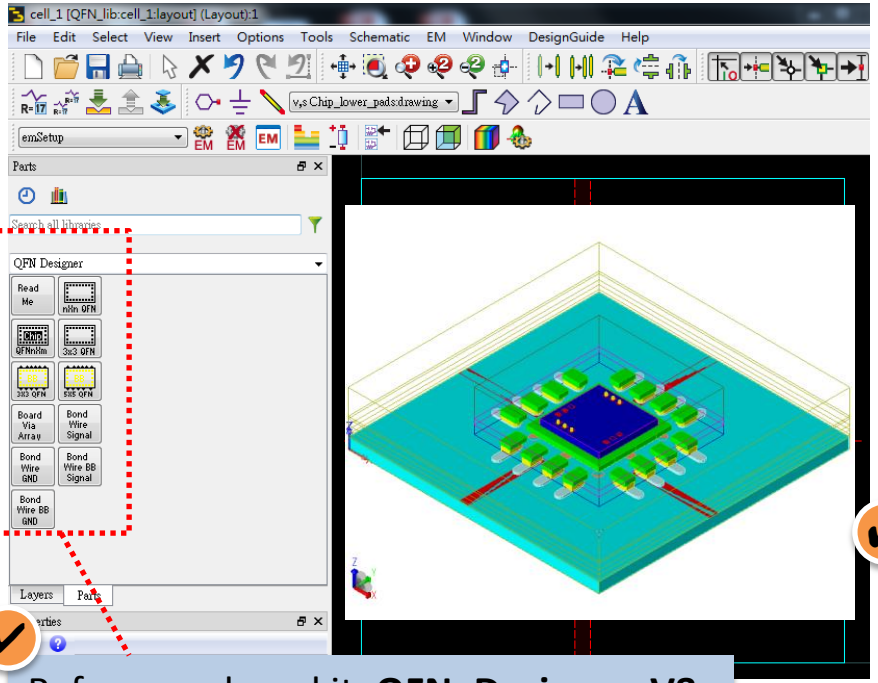
- **Pre-layout simulation**
  - Using equivalent models.
  - Coupling effect not considered.
  - Less simulation time.

- **Post-layout (EM-) simulation**
  - Performance extracted from the substrate definition file.
  - Coupling effect considered.
  - Taking more simulation time.

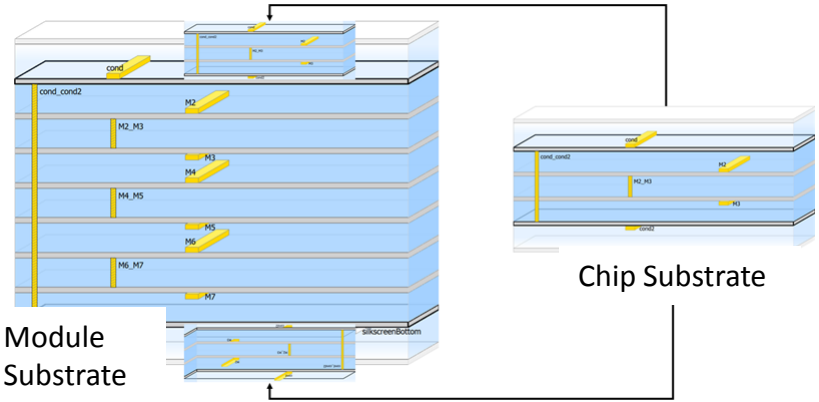
Off-Chip Elements



Smart Mount for Multi-Technology

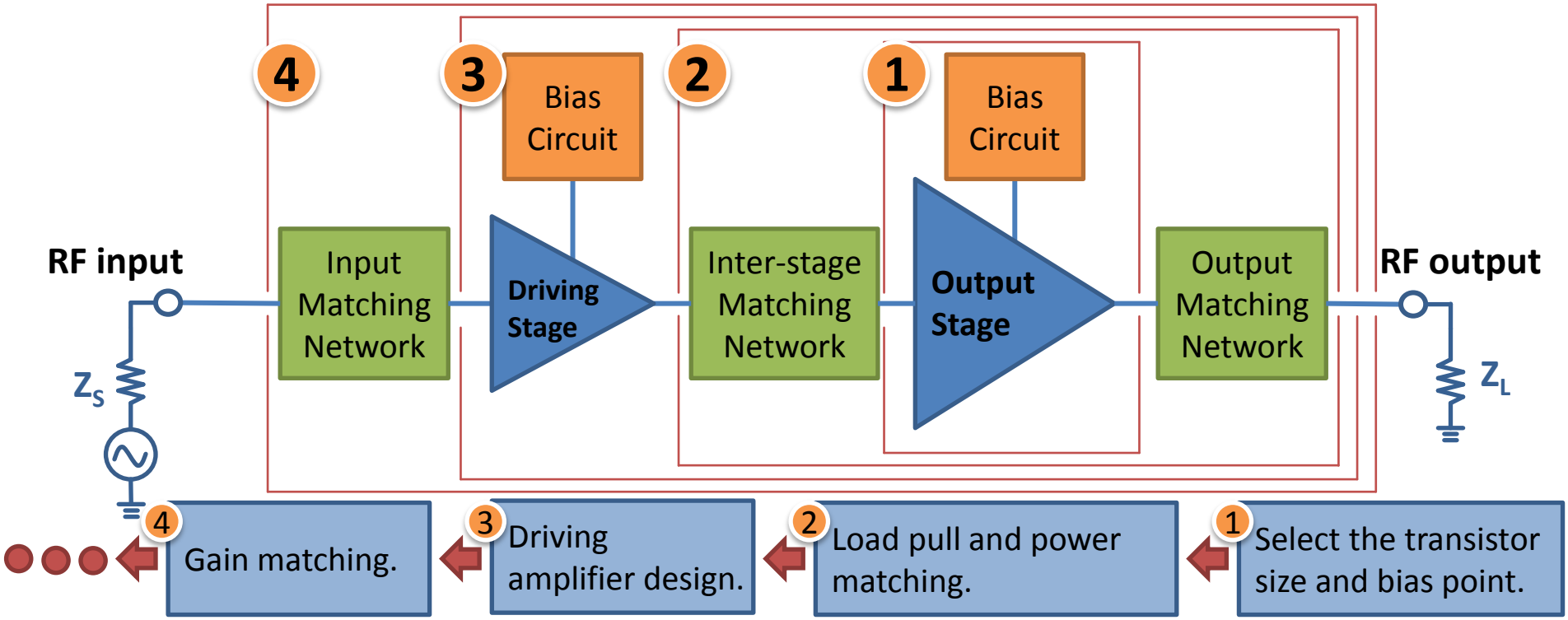


Reference demokit: **QFN_Designer_V8**

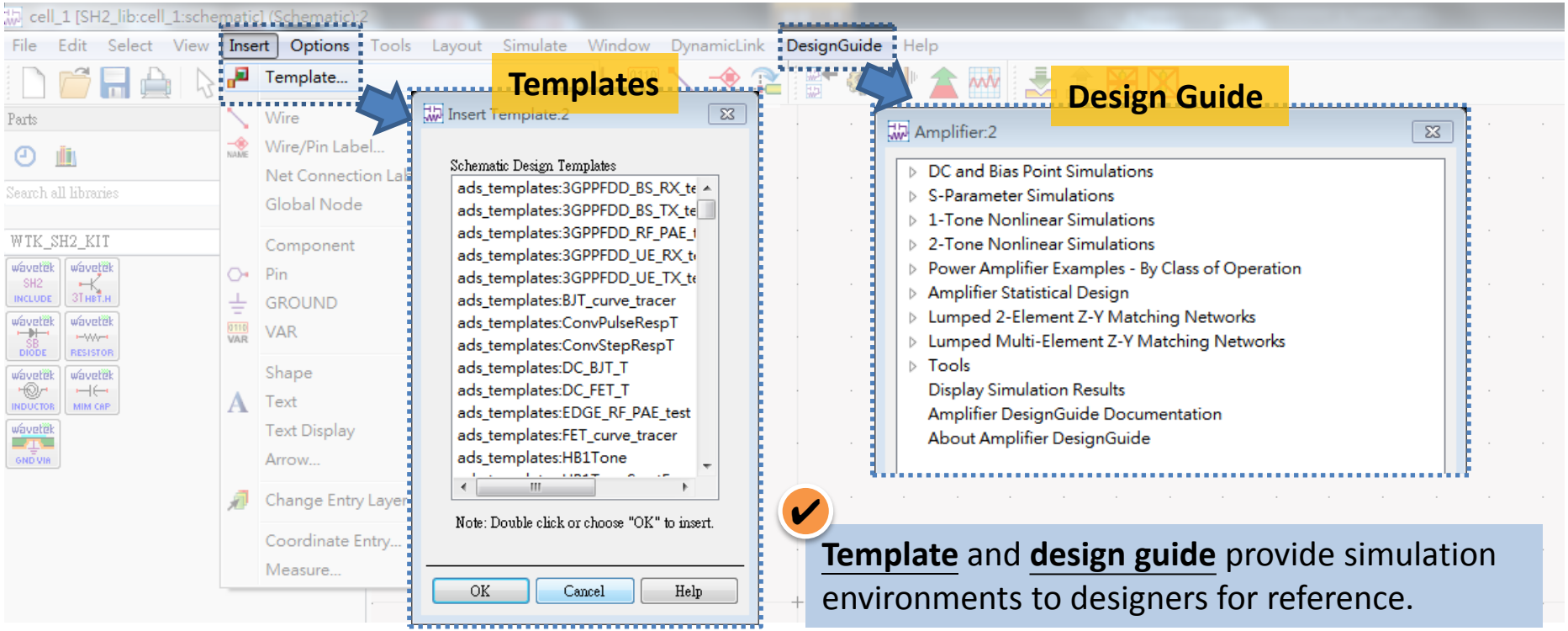


Smart Mount allows a component designed in one technology to be used in a design with a different technology.

Power Amplifier Design Flow

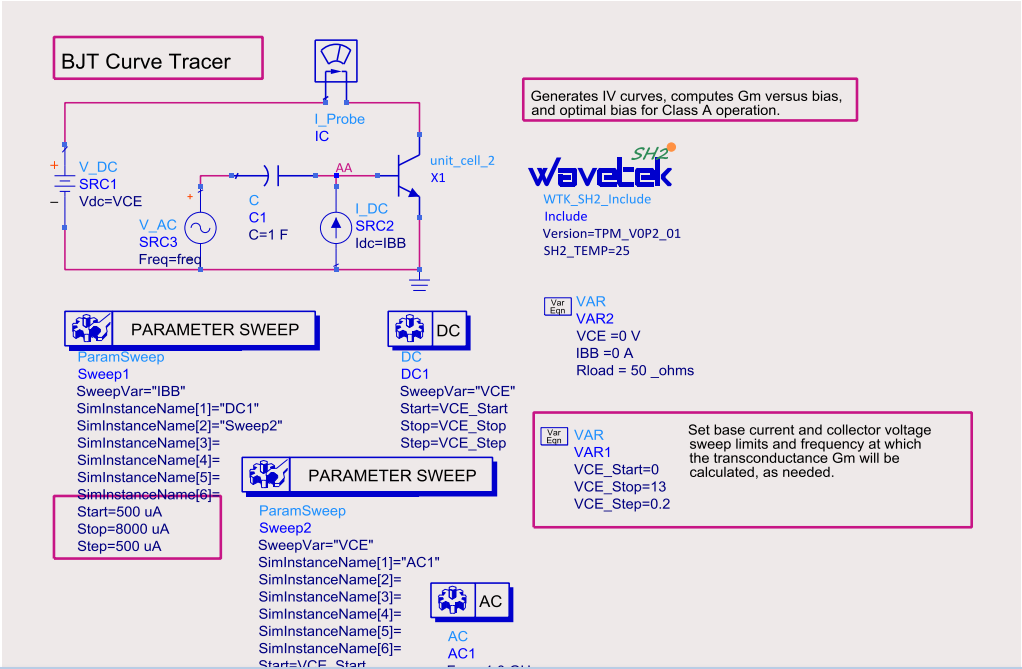


Test Bench from Design Guide



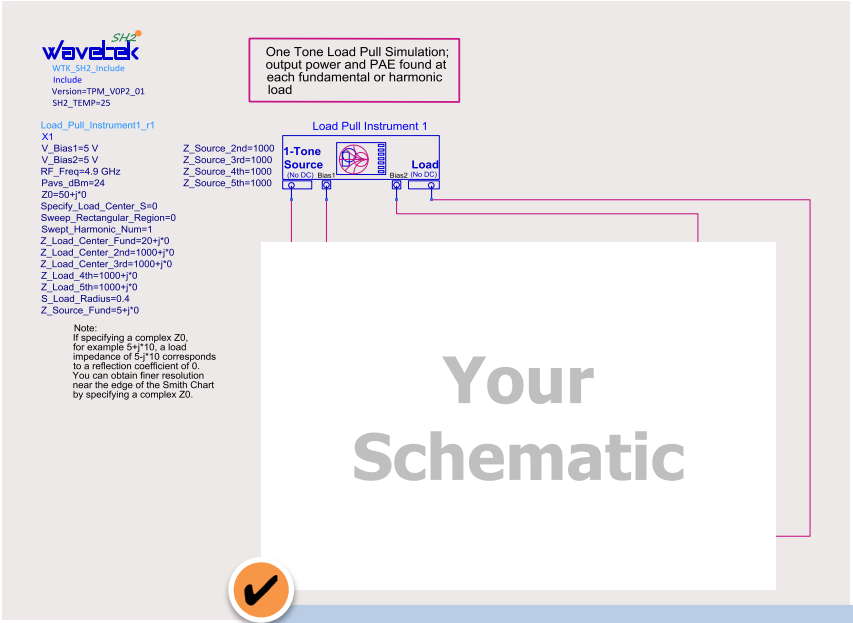
Template and **design guide** provide simulation environments to designers for reference.

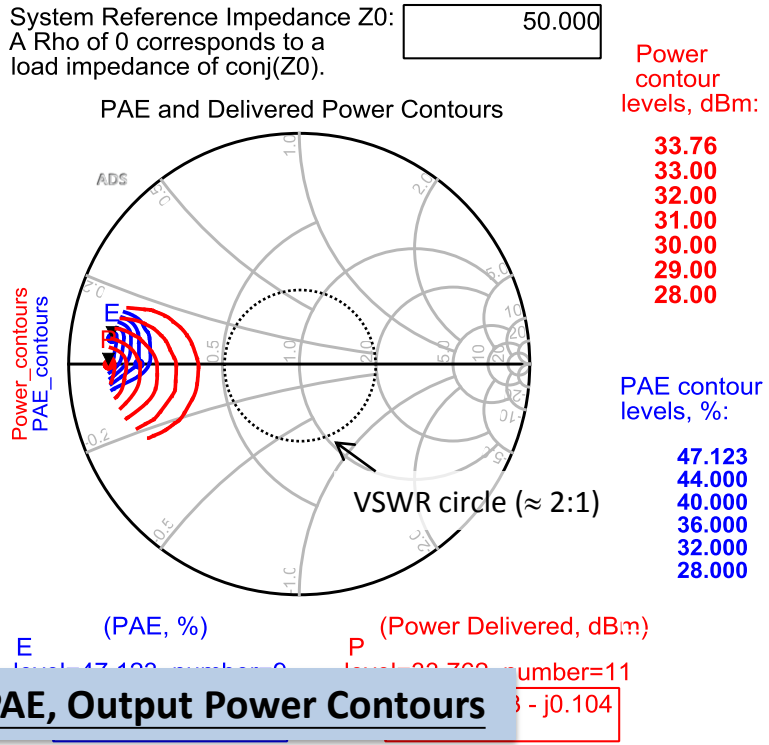
Device Analysis: DC Simulation



Reference design guide: **BJT I-V curve, Class A Power, Eff., Load, Gm vs. Bias**

Device Analysis: Load Pull

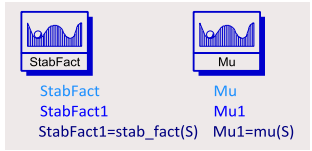


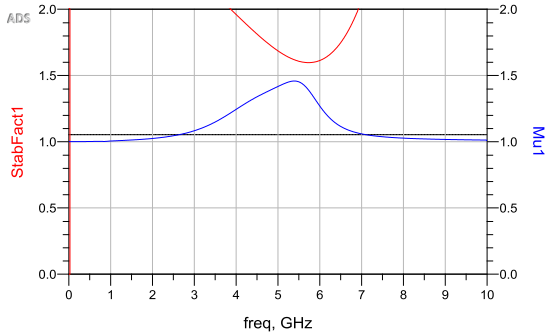


Reference design guide: **Load Pull – PAE, Output Power Contours**

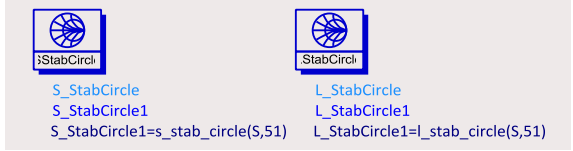
Device Analysis: Stability

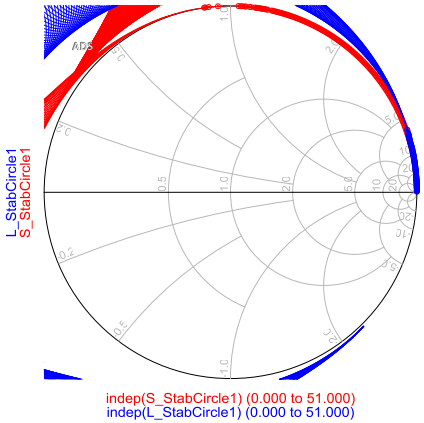
Mu and Stability Factor



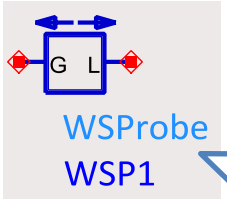


Stability Circle

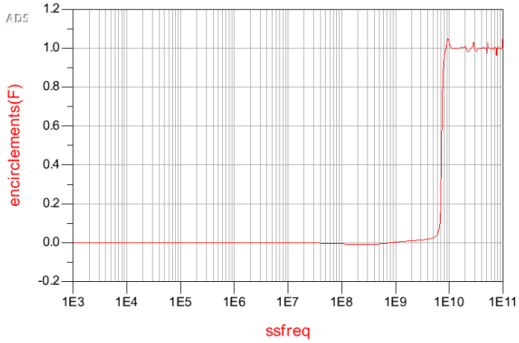




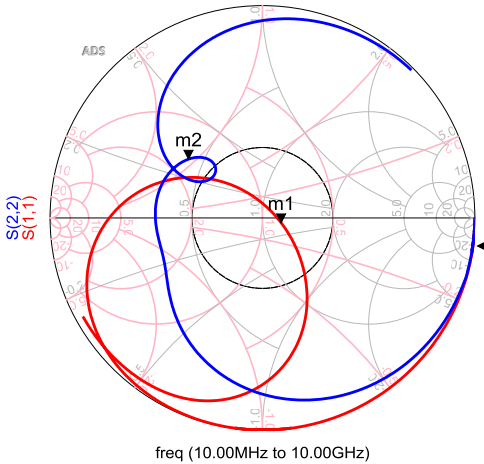
Winslow Stability Probe (WSProbe)



ADS 2020 new function!



Simulation: S-Parameter

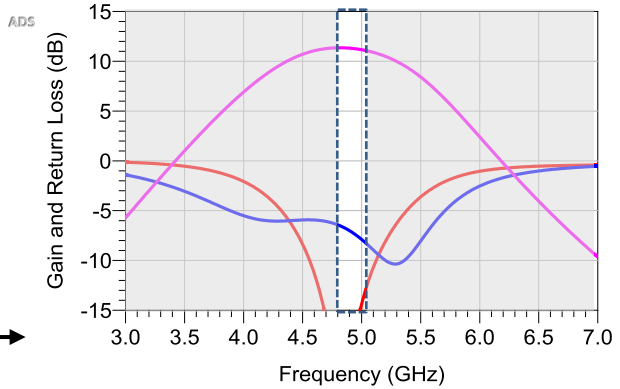


m1
freq=4.900GHz
S(1,1)=0.091 / -14.737
impedance = 59.596 - j2.787

m2
freq=4.900GHz
S(2,2)=0.445 / 141.537
impedance = 21.162 + j14.607

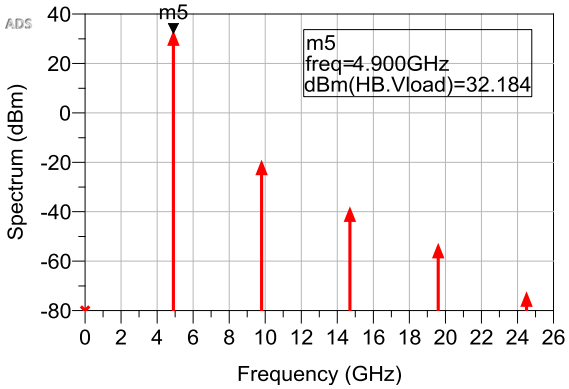
← Smith chart with S_{11} and S_{22}

Input / output return loss and gain →

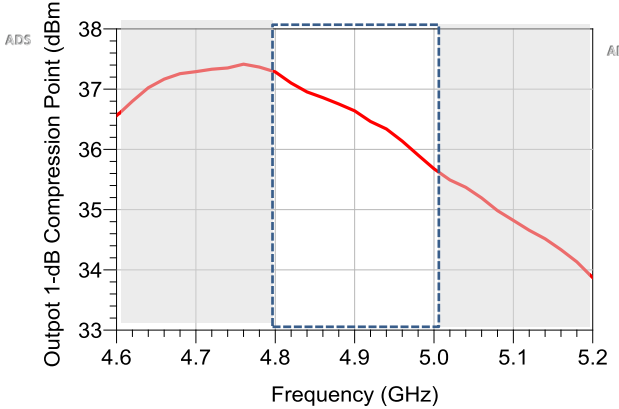


Simulation: Harmonic Balance

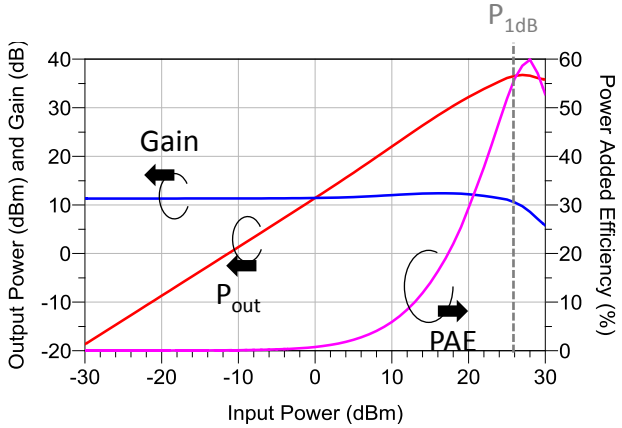
RF Spectrum



OP_{1dB} vs. Frequency



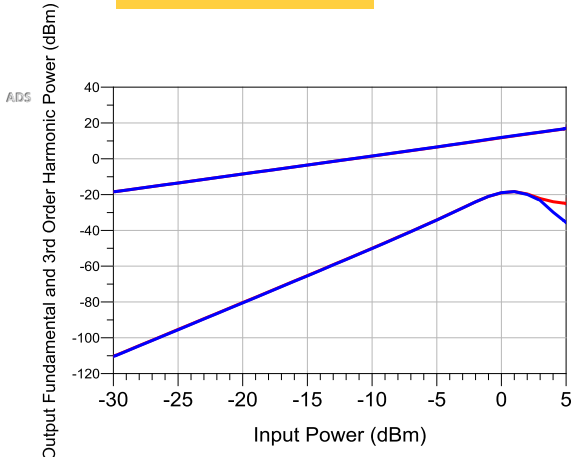
P_{out}, Gain and PAE vs. Frequency



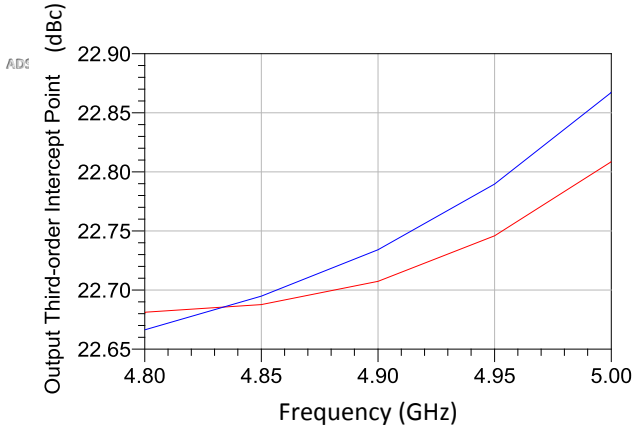
RF Frequency: 4.9 GHz

Simulation: Two-Tone and Modulation

P_{out} vs. P_{in}



OIP3 vs. Frequency



Complete Power Amplifier Design

Your Schematic

Complete your power amplifier!

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SUMMARY

Summary

1. The power amplifier is a critical component in the RF transmission system. This work demonstrates a step-to-step power amplifier design and raises several considerations for new designers.

2. To provide a friendly circuit design environment, ***Wavetek*** and ***Keysight*** would continually provide improved PDK solutions to all partners.

Welcome to Visit Wavetek Website

http://www.wtkmicro.com

Thank you for your listening