PathWave RFIC Design (GoldenGate) 2020

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Application Engineer	

KEYSIGHT TECHNOLOGIES

Keysight EEsof RFIC solutions

FROM TRANSISTORS TO CONNECTORS

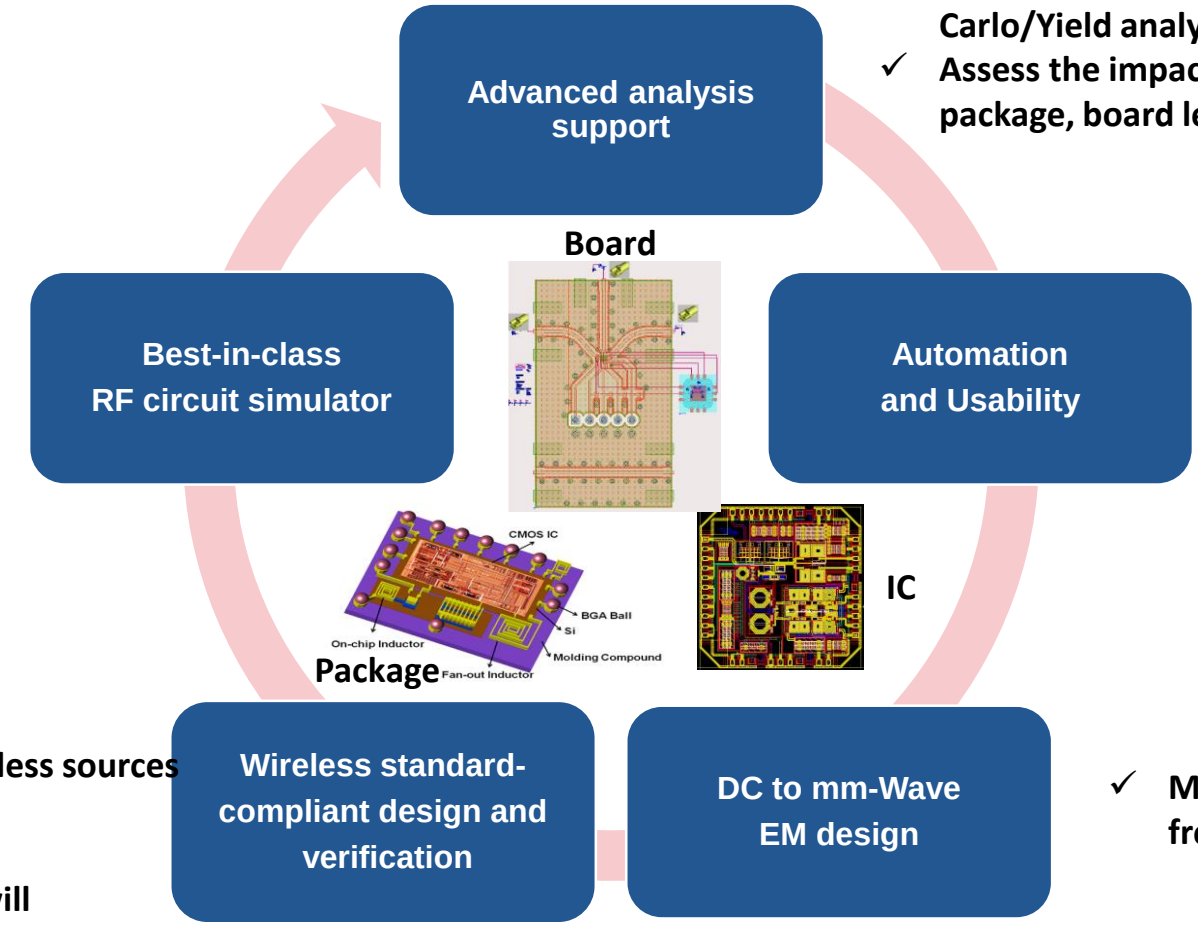
- ✓ Improve your on-chip test coverage (Monte Carlo/Yield analysis/Design centering)
- ✓ Assess the impact of thermal effects at chip, package, board levels

- ✓ Native support of distributed clusters
- ✓ Easily add packages and PCBs to your chip to assess impairments

- ✓ Monitor coupling, crosstalk and other frequency dependent effects up to mmWave

- ✓ Benefit of Keysight-graded wireless sources and sinks
- ✓ Customize the system tests at will

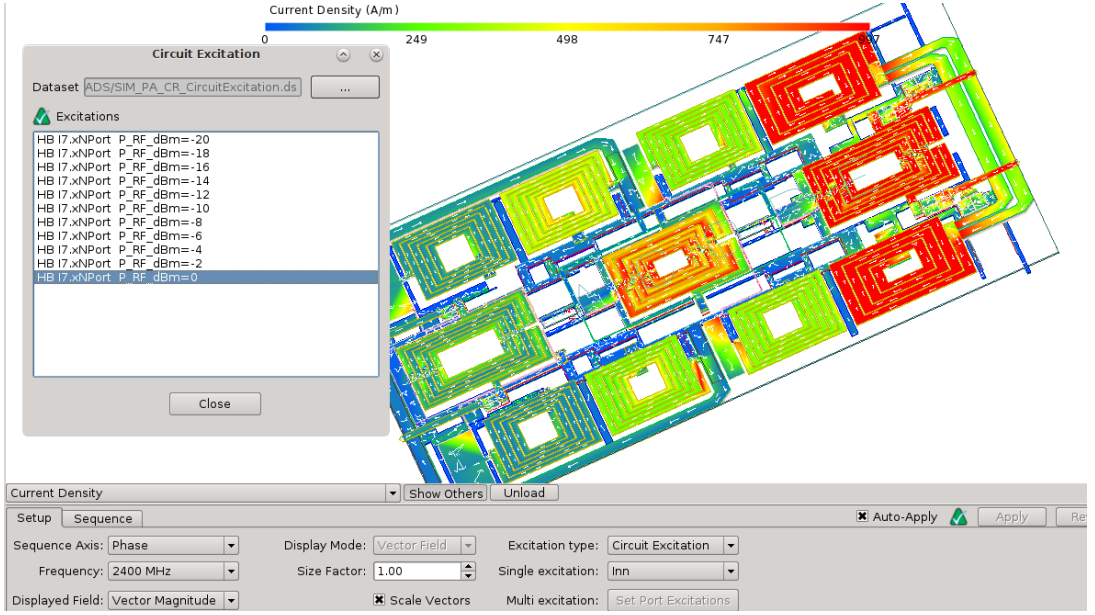
- ✓ Take advantage of the most robust RF engines



Analyze your EM circuit under real conditions

- Challenge:
  - At high frequencies, coupling is one of the most common problems designers face
  - But EM coupling is often analyzed without any non-linear devices and them improper loading
- GoldenGate 2020 now allows interaction with RFPro to look at current densities that correspond to your design under operating conditions

Look at current densities at the harmonic or power you want

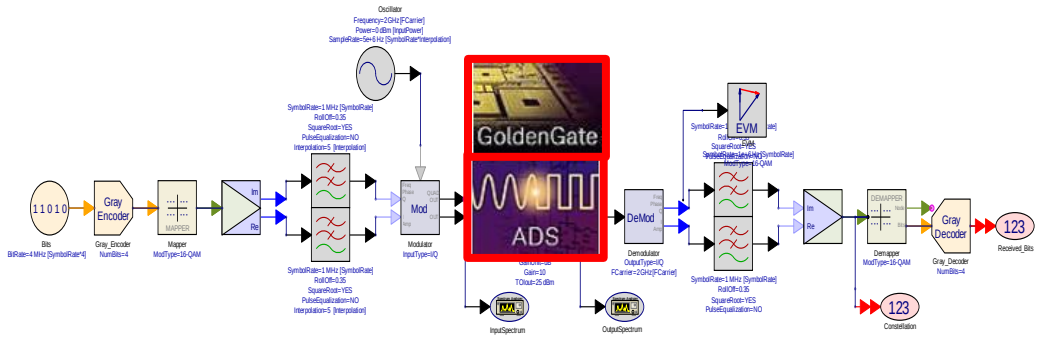


Design with modulated signals

DIFFERENT PLATFORMS BUT A COMMON NEED

System architecture engineers needs

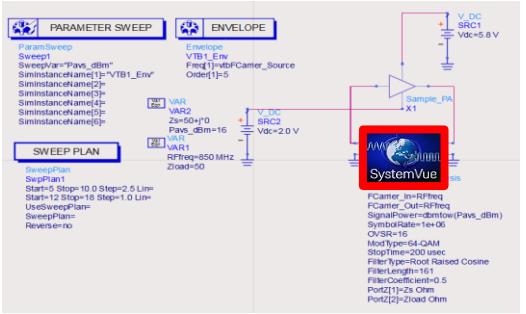
- Check RF impairments without loss of speed
- Be proactive on the RF impairments with digital processing
- Want to stay inside a system platform



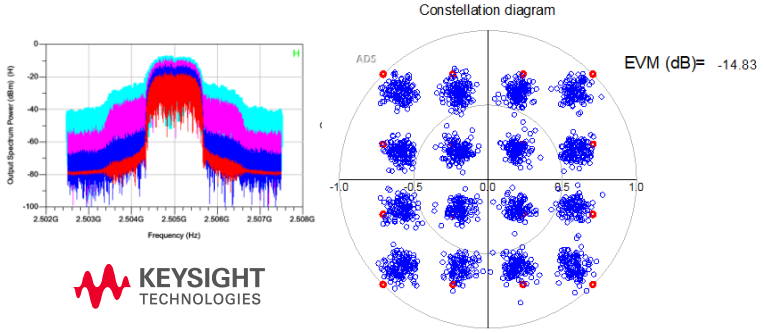
Solution : Bring circuit accuracy inside SystemVue

RF designer needs

- Quickly test their RF IPs on the latest wireless standards
- Do not want to understand fully the standards
- Want to stay inside Cadence Virtuoso or Keysight ADS
- Want to avoid overdesign due to IP3/IP5… approximations

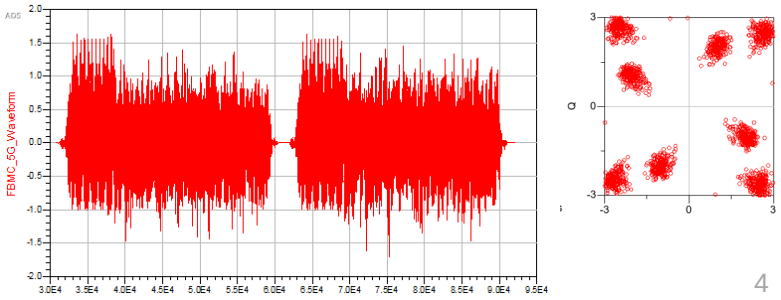


Solution : Bring SystemVue libraries inside Cadence



Same sources, same outputs !

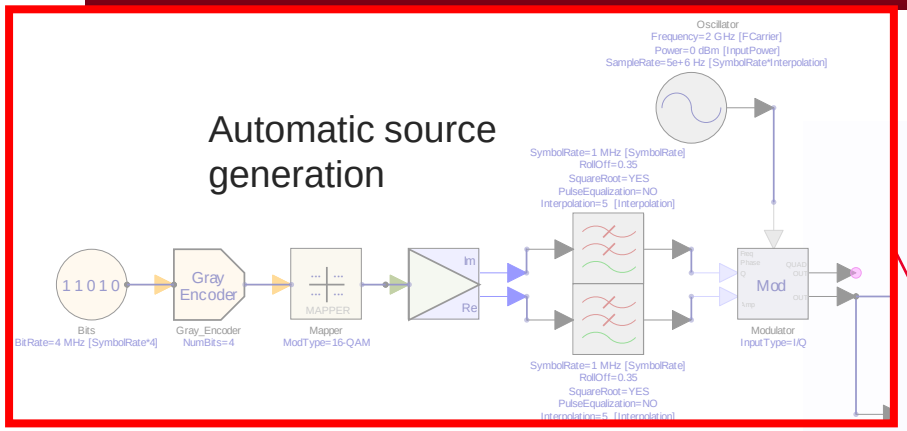
EVM Peak	EVM RMS	IQ Offset (dB20)	Phase Error Peak (°)	Phase Error RMS(°)
28.086	8.676	-51.79	-9.313	2.017

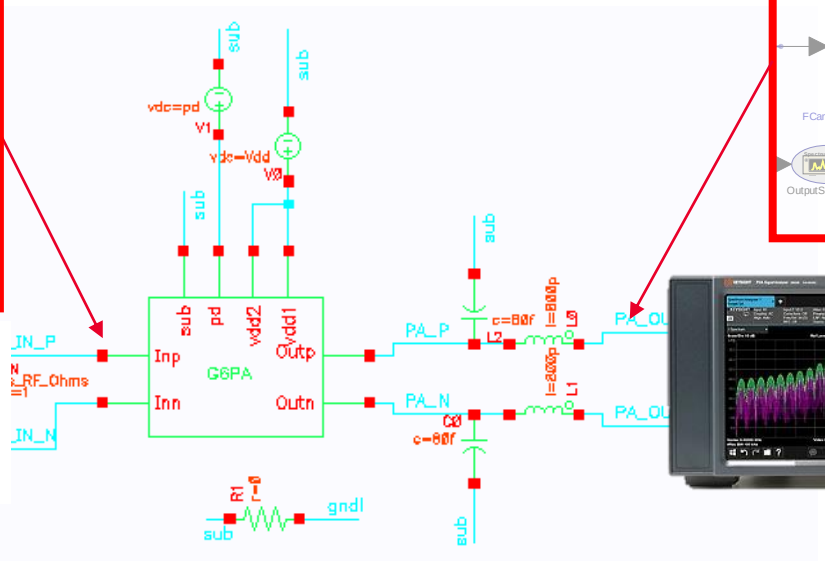


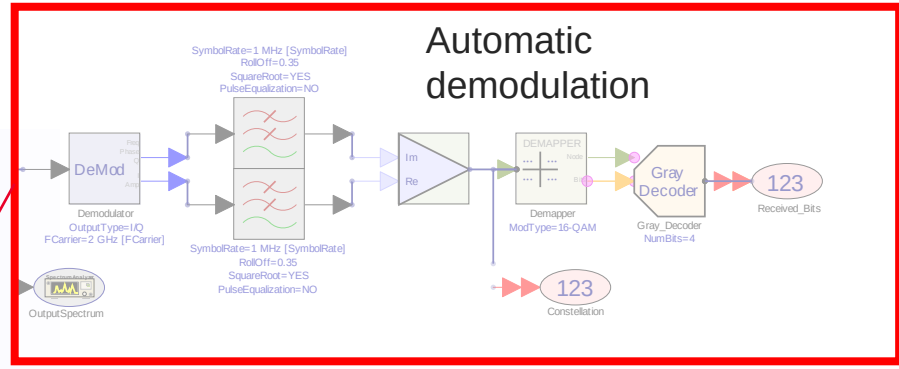
KEYSIGHT TECHNOLOGIES

RF designers workflow : Virtual Testbenches

BRING SYSTEMVUE INSIDE ADS OR VIRTUOSO







ADS/GoldenGate can use SystemVue Virtual Testbenches (VTB) to **automatically**

- Generate a waveform compliant with wireless standards
- Demodulate the signal to produce system figures of merits (EVM, CCDF,…)

Keysight Fast Envelope algorithms speed up simulations by orders of magnitude vs. classical Envelope

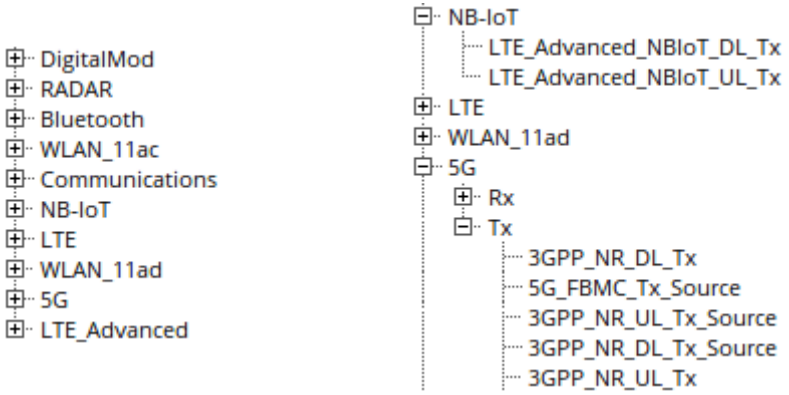
VTBs boast traceability of the tests used (bandwidth, modulation scheme, source power) than classical methods using files do not offer.

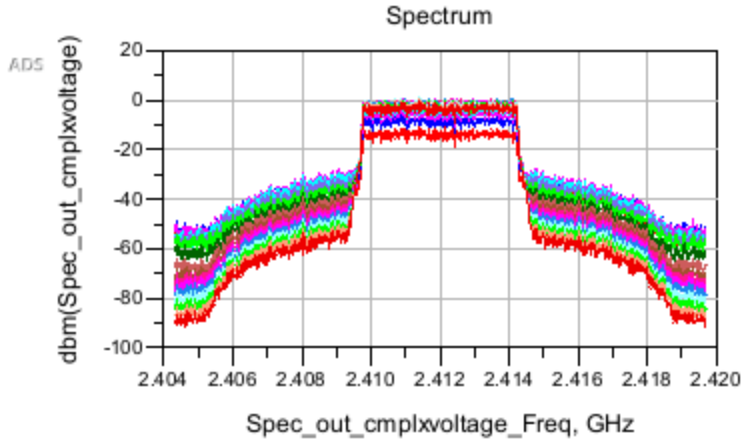
5G NR, Verizon, (U)F-OFDM, FBMC
3GPP / LTE, LTE Advanced
802.11 a/b/n/ac/ad/ah
802.15.3c, 802.15.4, 802.16e
Bluetooth (Basic, Enhanced and BLE)
GNSS/GPS
DVB-x2

Modulated signals update in GoldenGate 2020

THE LATEST STANDARDS ARE EMBEDDED !

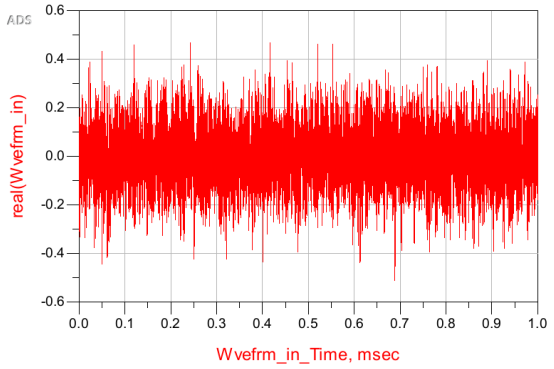
- No need to look for a file or install something else, the modulated signals are one toggle away





P_RF_dBm	N1_EVM N1_EVM_Frame=0
-5.000	11.526
-6.000	9.121
-7.000	6.936
-8.000	5.068
-9.000	3.592
-10.000	2.524
-11.000	1.824
-12.000	1.402

EVM and Output Spectrum of a PA under 5GNR conditions



IP analyses assume a couple of sines. 5GNR waveform [PAPR > 15 dB] is far from being a sine !

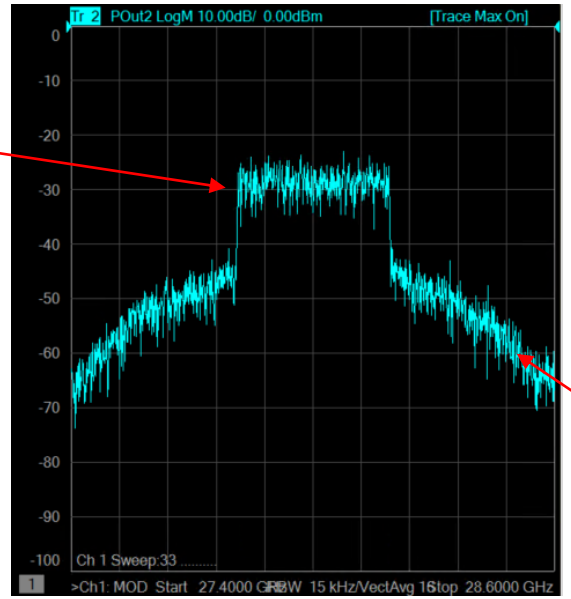
Distortion EVM

BRING A PNA-X INSIDE VIRTUOSO

Output Signal Spectrum

- If you have your own IQ files, computing an EVM is a challenge
  - What are the bandwidth/numerology/number of subcarriers/…?
  - Spectral regrowth (ACPR) does not give all the needed insights

In-band distortion
Typically represented as NPR or EVM



Out-band distortion
Typically represented as ACPR

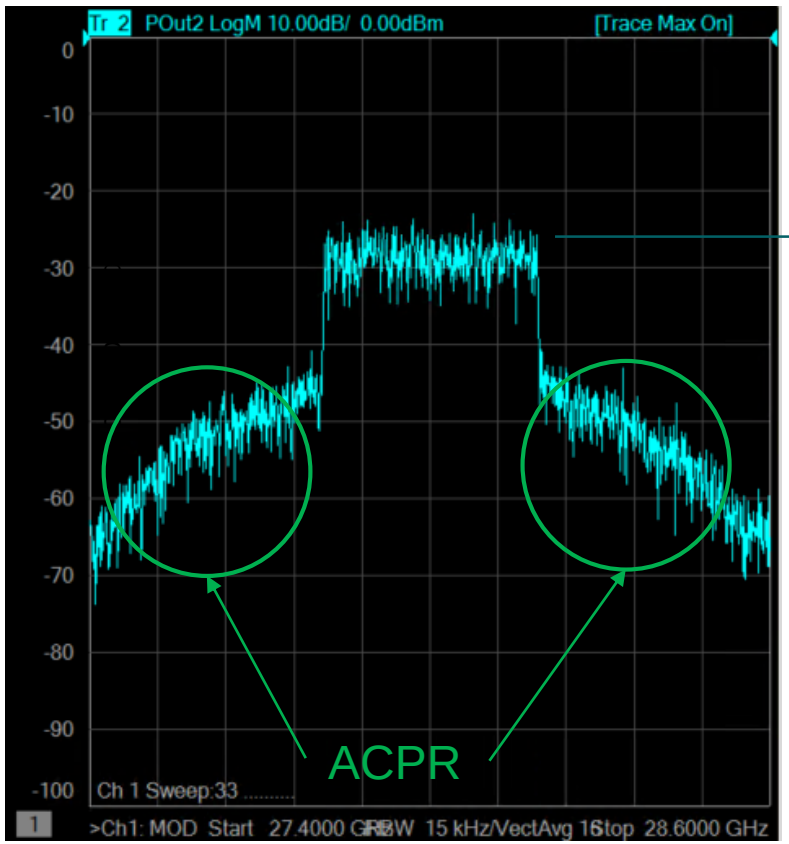
Underlying Technology

COMPUTING FIGURE OF MERITS

$Y(f)$:Output signal

$H(f)X(f)$:Linear part

$D(f)$:Distortion part



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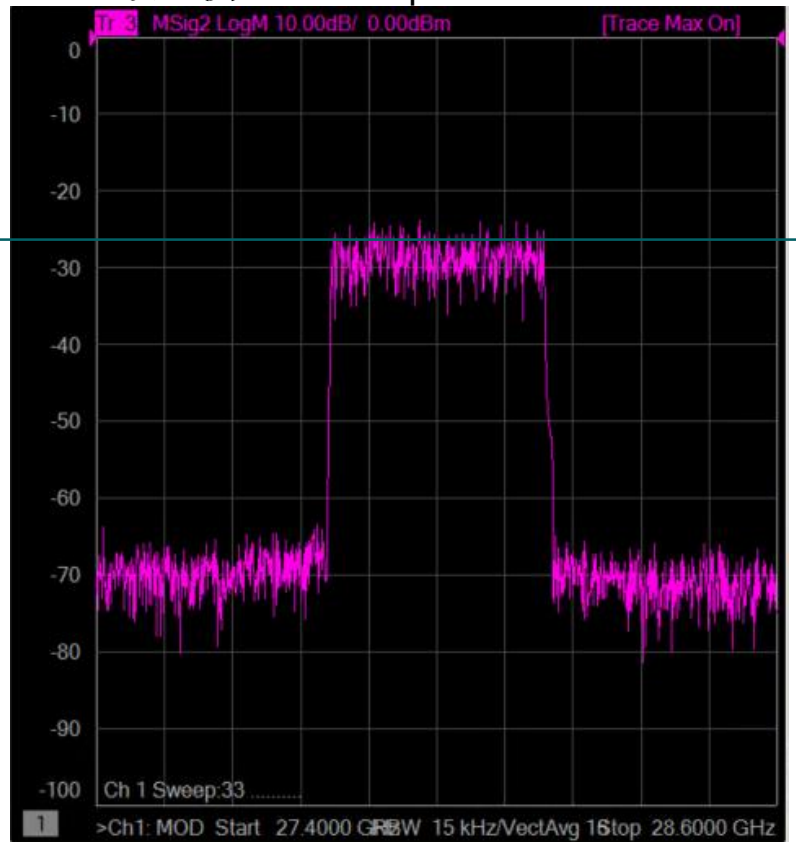

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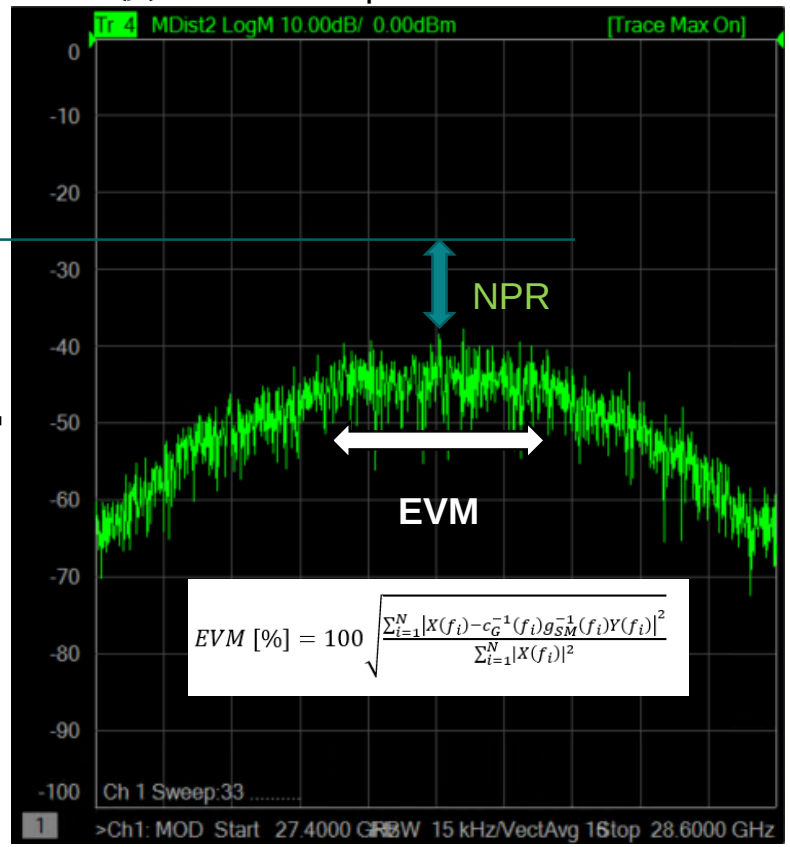
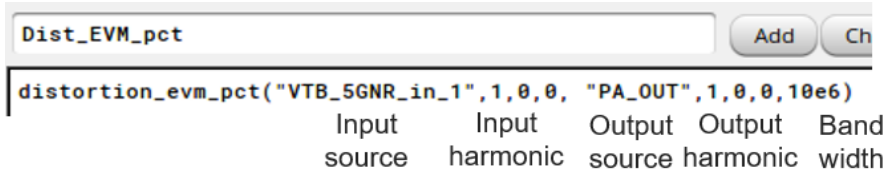


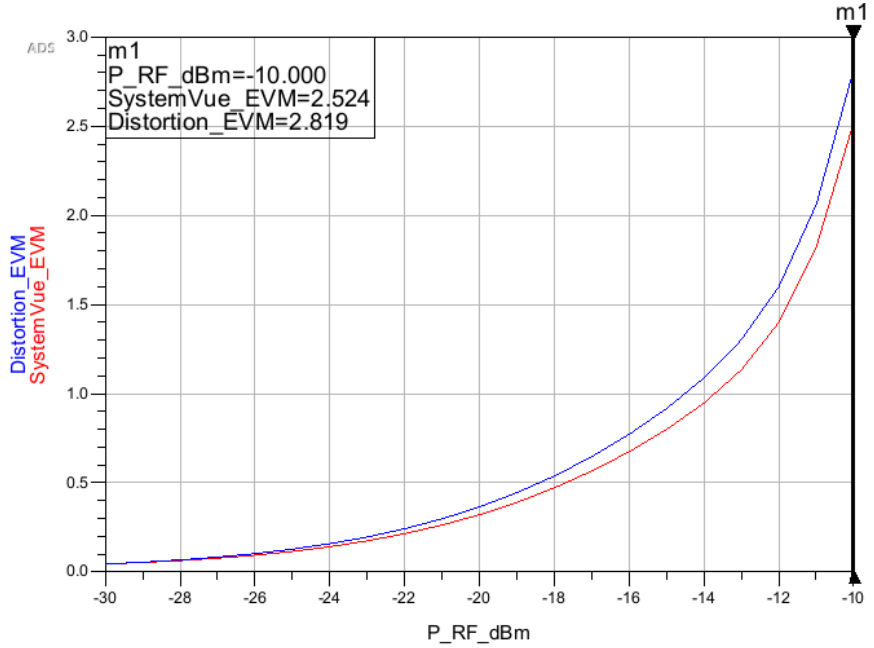
- EVM computed from time domain and frequency domain are mathematically equivalent (Parseval's theorem)

Distortion EVM inside GoldenGate

- Available as a performance (percent or dB) inside GoldenGate
  - Allows sweeps, MonteCarlo, LoadPull, integration into ADE-XL or Maestro
  - Extended to devices with frequency translation
  - Complements VTB reference EVMs

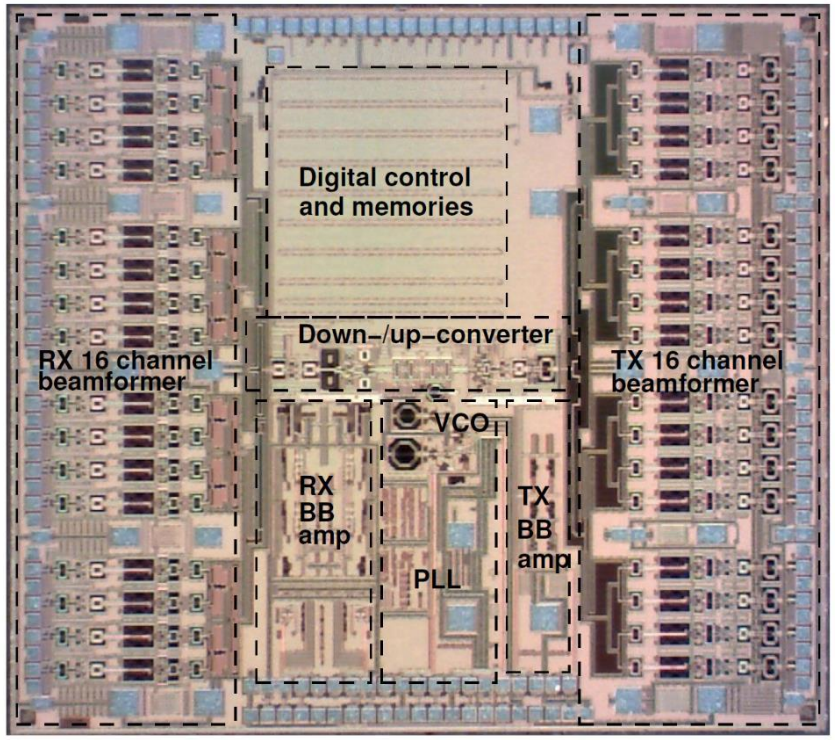


5GNR PA EVM
SystemVue
Distortion
Less than 0.3% diff



Designing an Award-Winning mmWave RFIC: Experiences and Insights

Erik Öjefors, Mikael Andreasson, Torgil Kjellberg, Håkan Berg, Lars Aspemyr, Richard Nilsson, Klas Brink, Robin Dahlbäck, Dapeng Wu, Kristoffer Sjögren and Mats Carlsson



802.11ad 60-GHz RF transceiver chip

Outline

- **Introduction of Sivers IMA AB**
- **Application of the 802.11ad standard for fixed-wireless access and backhaul**
  - Key performance parameters and design challenges
- **Overview of the Keysight tools used in the design flow**
  - SystemVue, GoldenGate, and VTBs
- **Chip design and simulation**
  - Architecture and key circuit blocks, beamformer, LNA, PA and VCO
  - Modulated signals and EVM performance on transistor level, early feedback to system simulation
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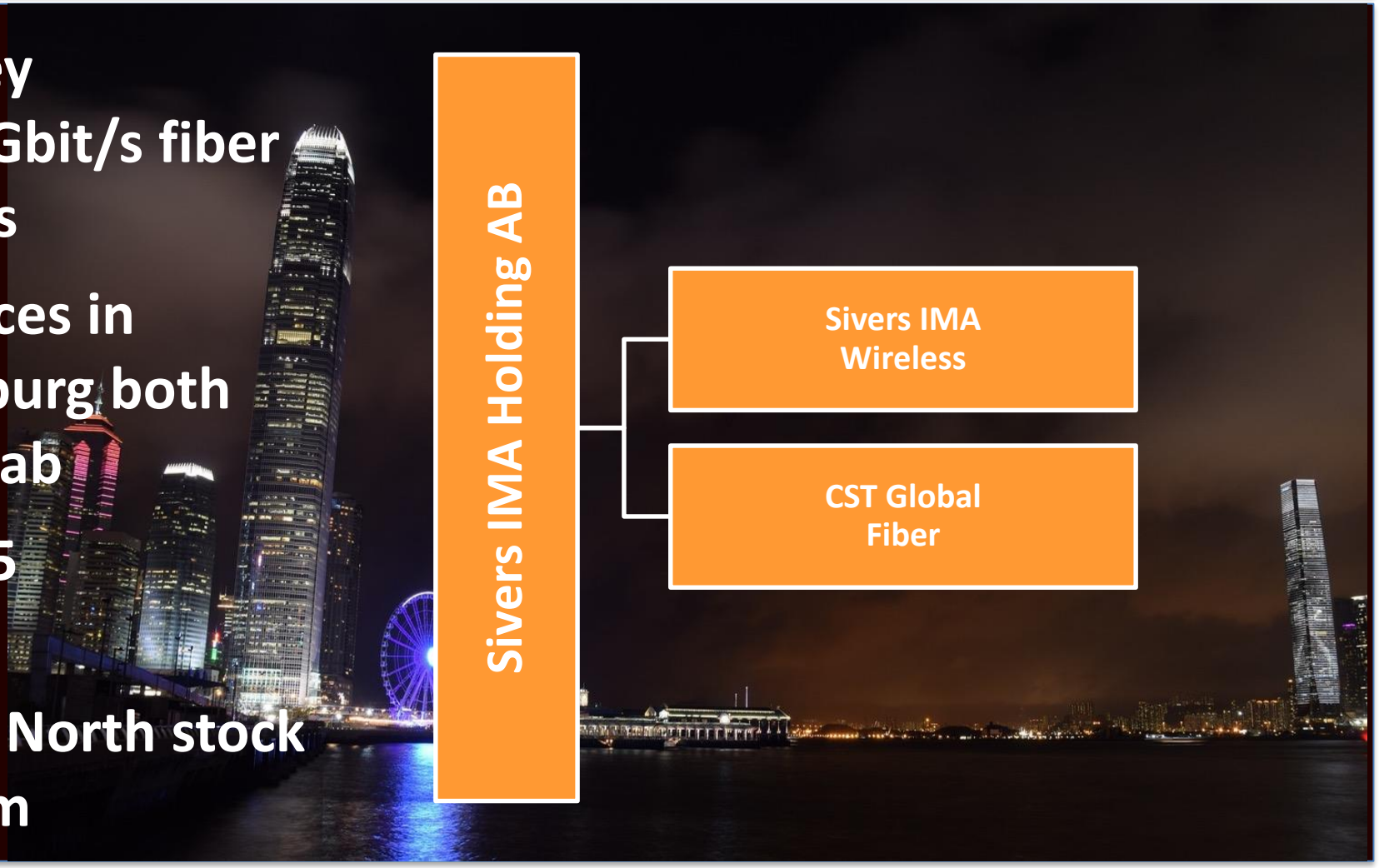
Sivers IMA Holding AB in Short

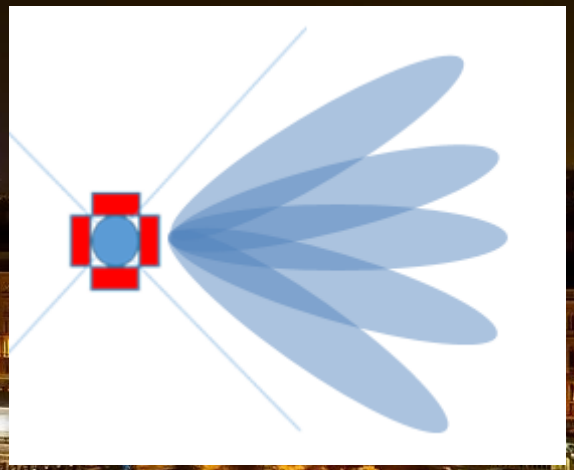
- Sivers IMA delivers key technology for multi-Gbit/s fiber and wireless networks
- HQ in Stockholm, offices in Glasgow and Gothenburg both with sales, R&D and Lab
- 100 employees and 15 consultants
- Listed at Nasdaq First North stock exchange in Stockholm

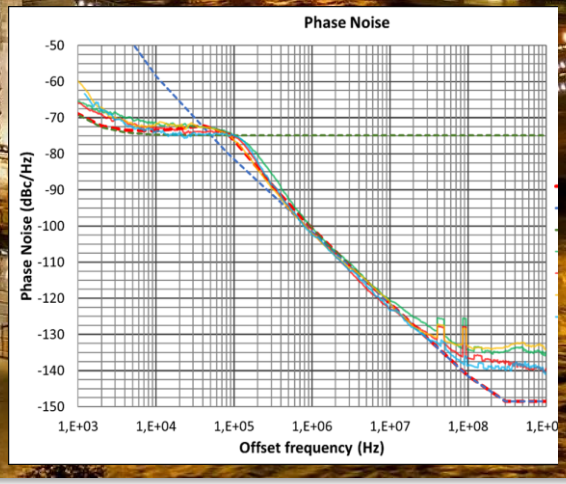


The Road to Gigabit Speeds Goes Via mmWave

KEY RF COMPETENCE:

- mmWave
  - 802.11ad/ay and 5G
- Phased array antennas
- Beam steering/ Beam forming
- Low phase-noise synthesizers





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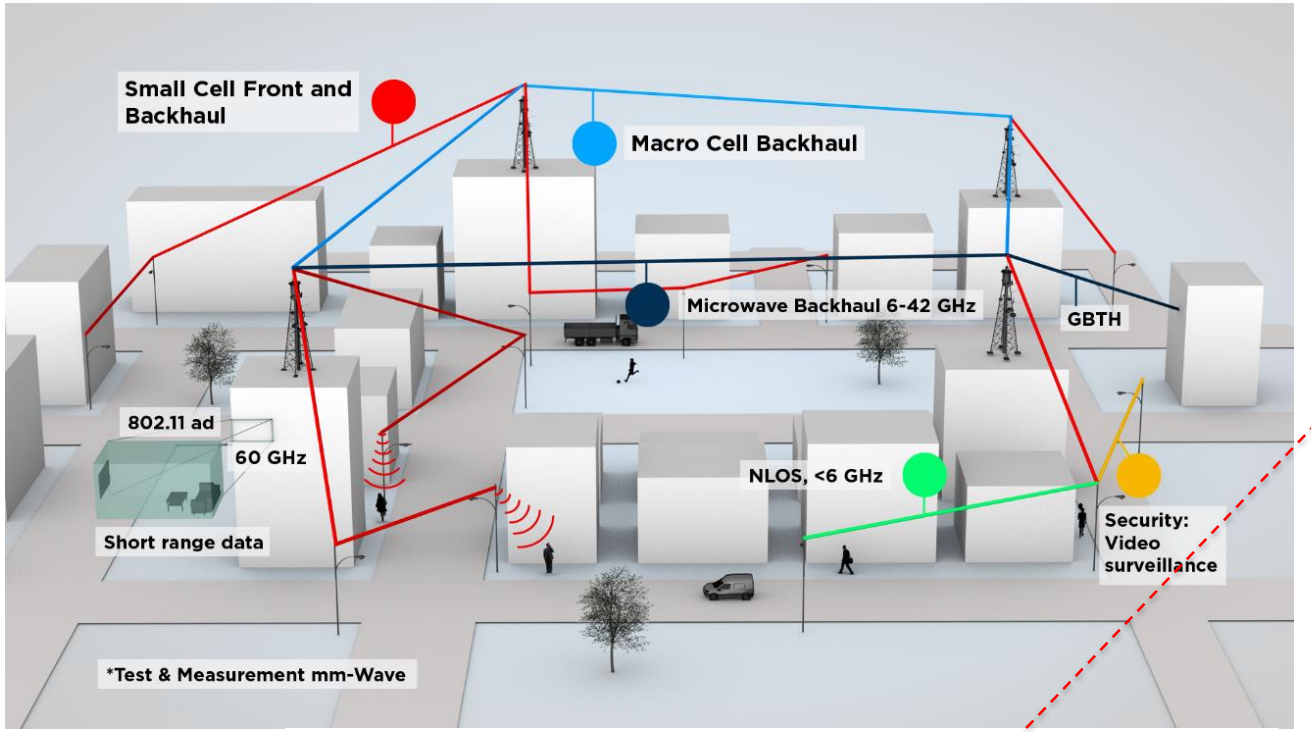
FWA and Backhaul with 60-GHz 802.11ad (WiGig)

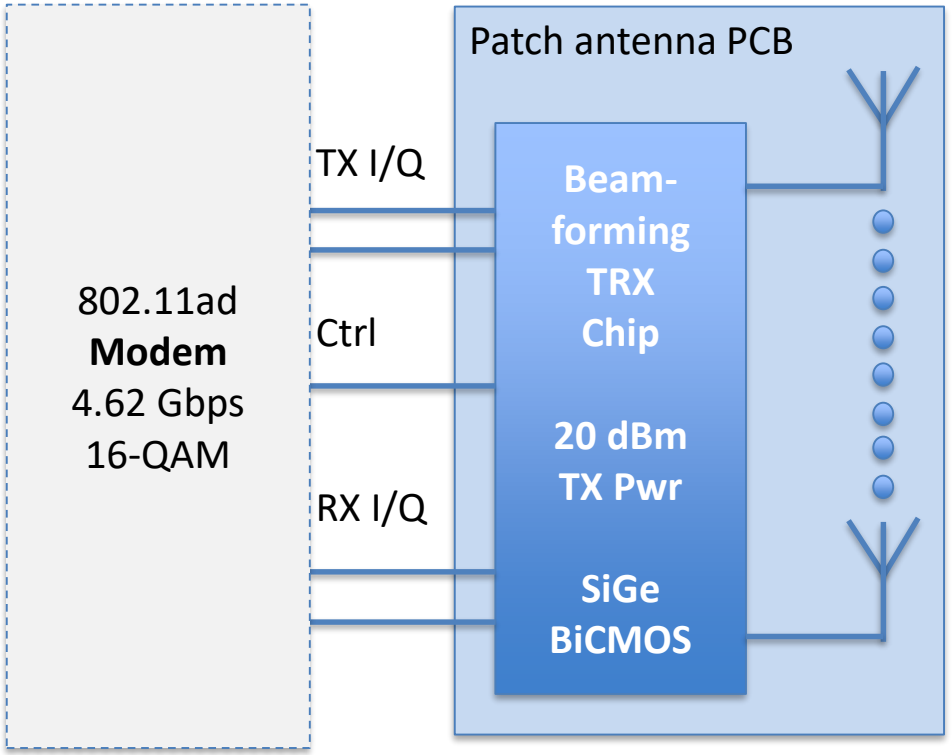


Self-organizing mesh networks for 60GHz carrier-grade access points with Gbit speed up to 500m distance based on 802.11ad

Key performance parameters!

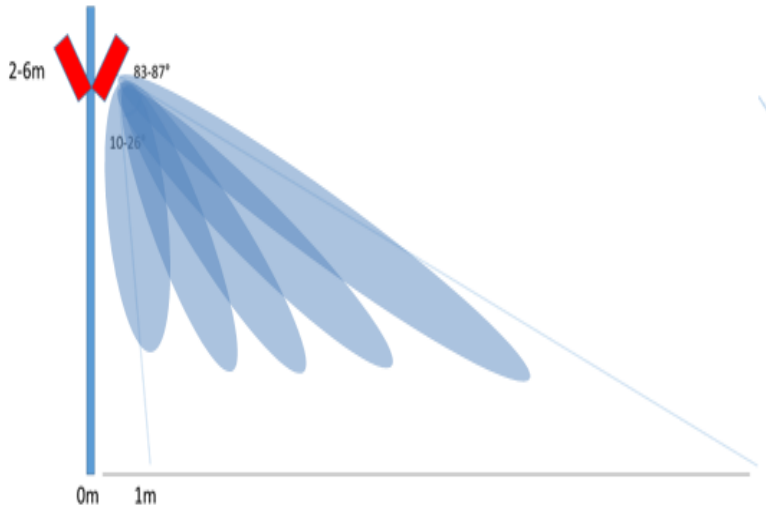
- New FCC/ETSI rules drive new radio spec
  - **40 dBm EIRP** allowed with a low-gain (typ. 20 dBi) antenna, requires **> 20 dBm TX** power
  - Frequency range **57-71 GHz** (previously 57-66 GHz), two extra channels
- Half-channel 64/128/256 QAM modulation for dense networks
  - **Phase noise, < 100 dBc@1MHz**

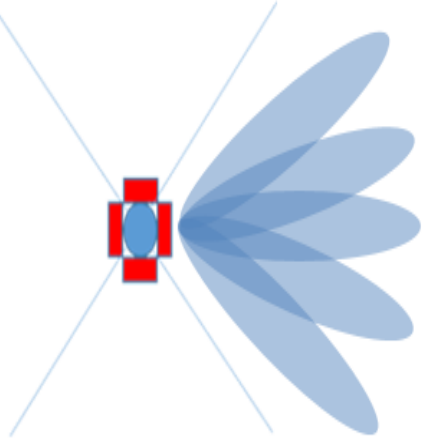
Our 802.11ad Solution for Infrastructure Equipment



16 TX/RX 20 dBi antenna array

EIRP > 40 dBm coverage, full 57-71GHz BW





Elevation: ± 9°deg (fixed beam)

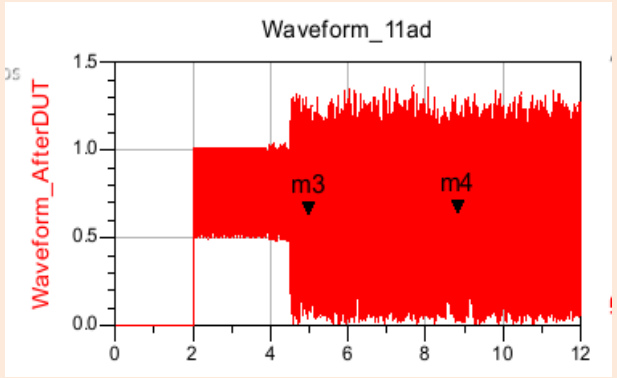
Azimuth: ±45°steering

- Challenging system design, baseband 0-1 GHz, severe timing requirements
- Rapid (<35 ns) steering over 64 beams
- Competitive market, demand for first-time right designs

Design Challenges (i)

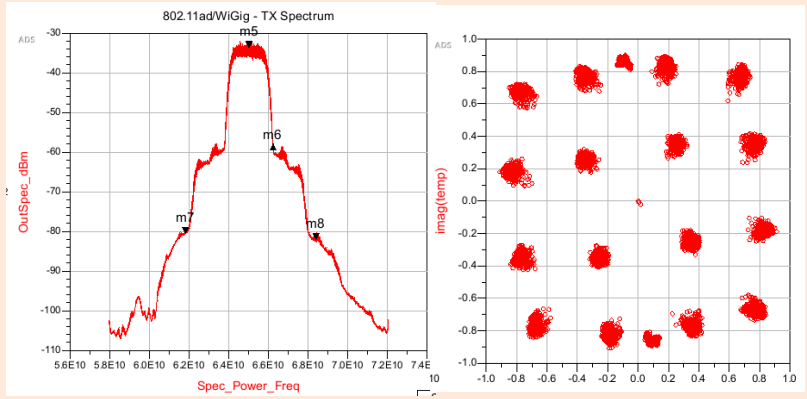
Maximizing output power with acceptable EVM and DC power

- Modulations in 802.11ad are quite robust, operation close to P1dB possible
- OIP3 not useful when operating close to close compression!
- Predicting output power using 802.11ad waveform in envelope simulation



- **Goal: Maximize output power with TX EVM < -21 dB (802.11ad spec)**
  - On transistor level in Cadence, check PA load and bias
  - EVM partitioning (PA, VCO...) in system simulator

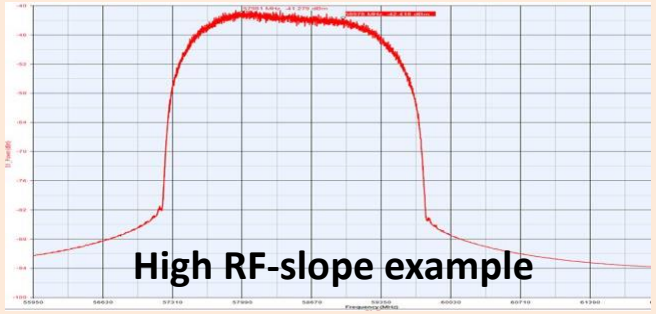
- **Get constellation diagrams early in circuit design**, great for intuitive understanding
    - AM-PM and unsymmetries



Design Challenges(ii)

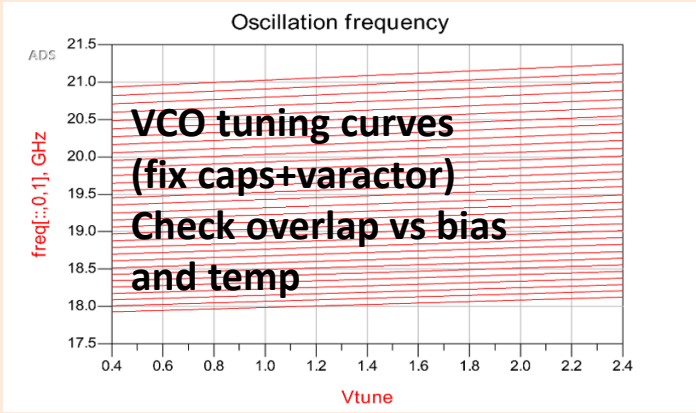
Channel width 2 GHz, 57-71 GHz freq. range

- Frequency response not flat in either RF or analog BB
- Need to model EVM degradation and spectrum in system simulator



Phase noise

- High phase-noise requirements, and a large band
  - Two VCO cores and varactor/fix cap topology
  - Large simulation matrix requires fast simulator



High circuit complexity, 16 TX/RX paths and on-chip frequency generation

- HB simulator speed and ability to handle large designs

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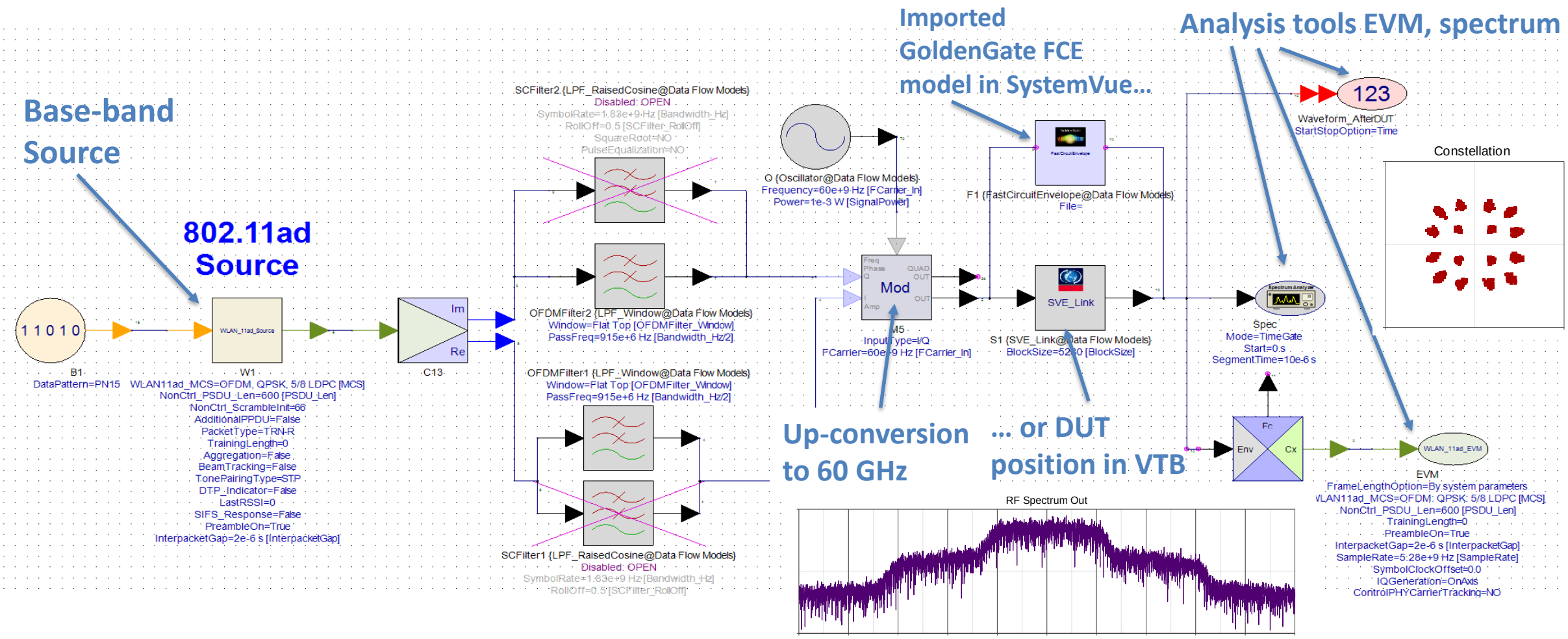
An 802.11ad Testbench for SystemVue and GoldenGate

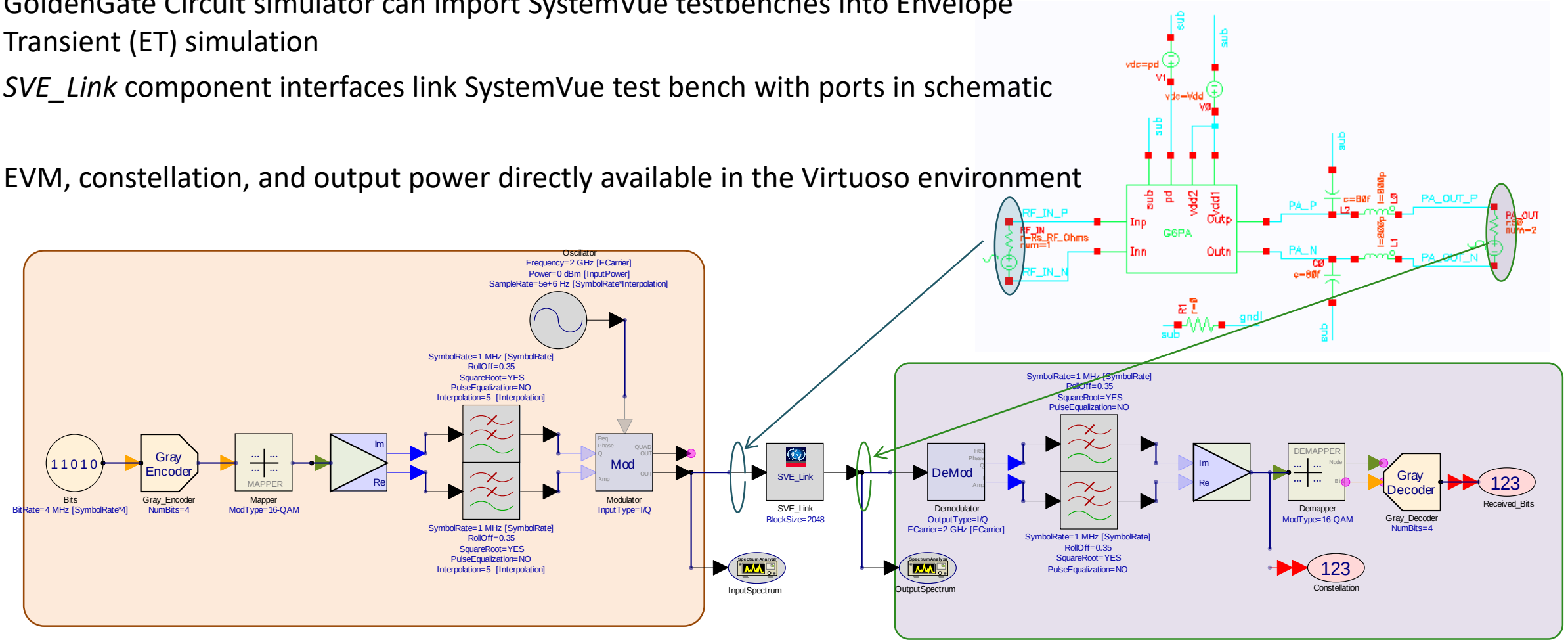


Virtual Test Bench - Using VTBs in Cadence Virtuoso

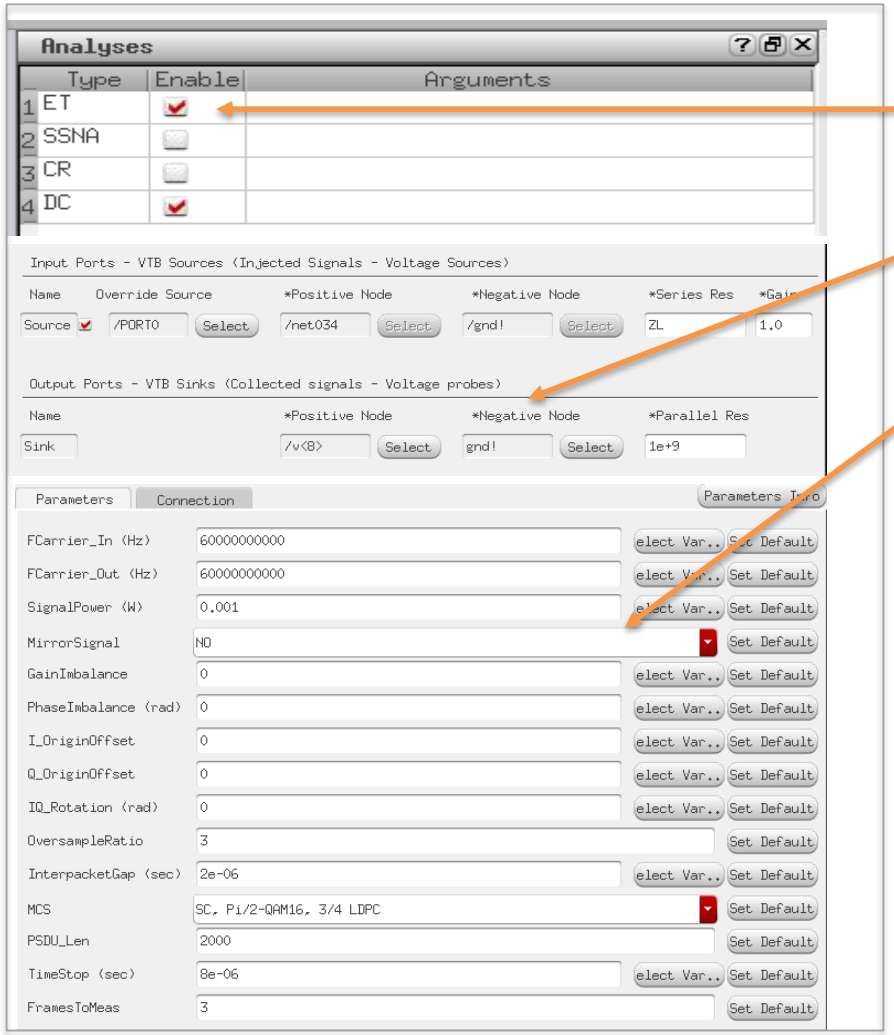
GoldenGate Circuit simulator can import SystemVue testbenches into Envelope Transient (ET) simulation

SVE_Link component interfaces link SystemVue test bench with ports in schematic

EVM, constellation, and output power directly available in the Virtuoso environment

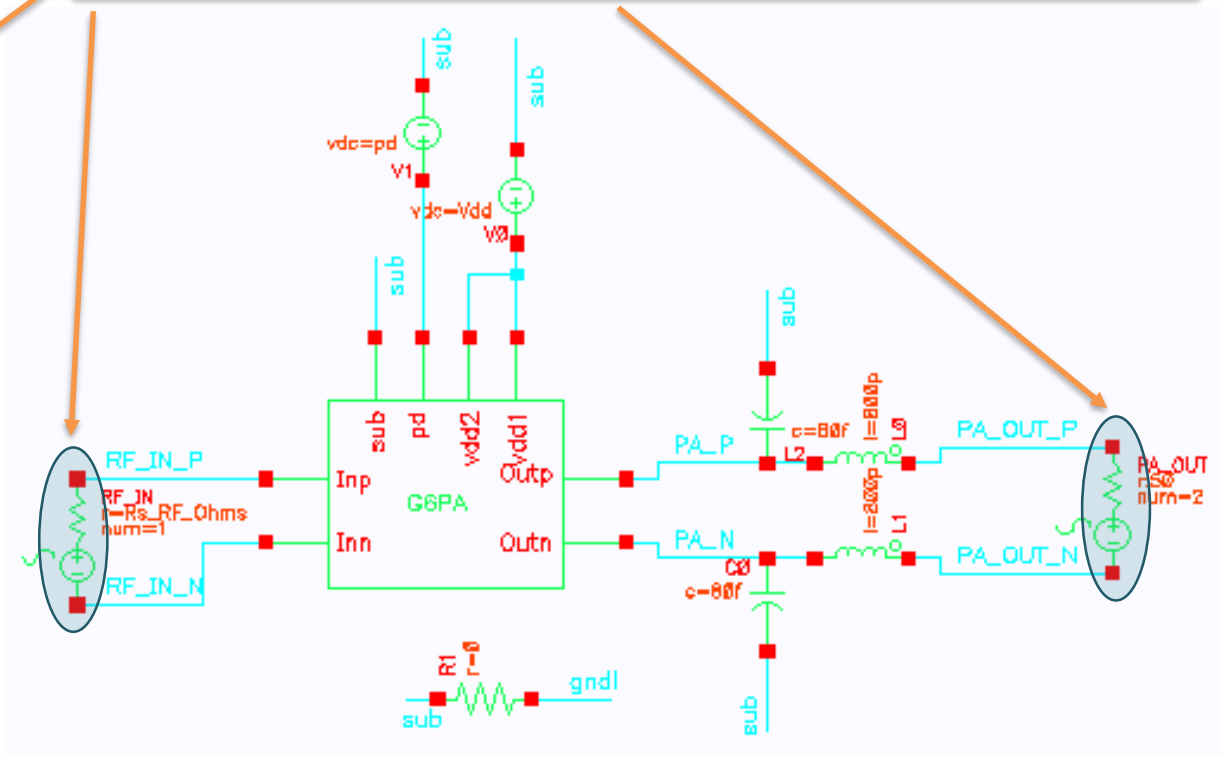


VTB Setup in Cadence Schematic and ADE/Explorer



GoldenGate Simulator settings in Analog Environment

- Choosing Envelope simulation
- Variables that can changed in the SystemVue
- Defining in/out ports in schematic window



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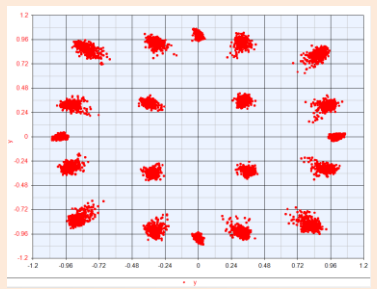
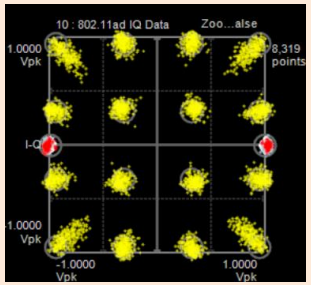


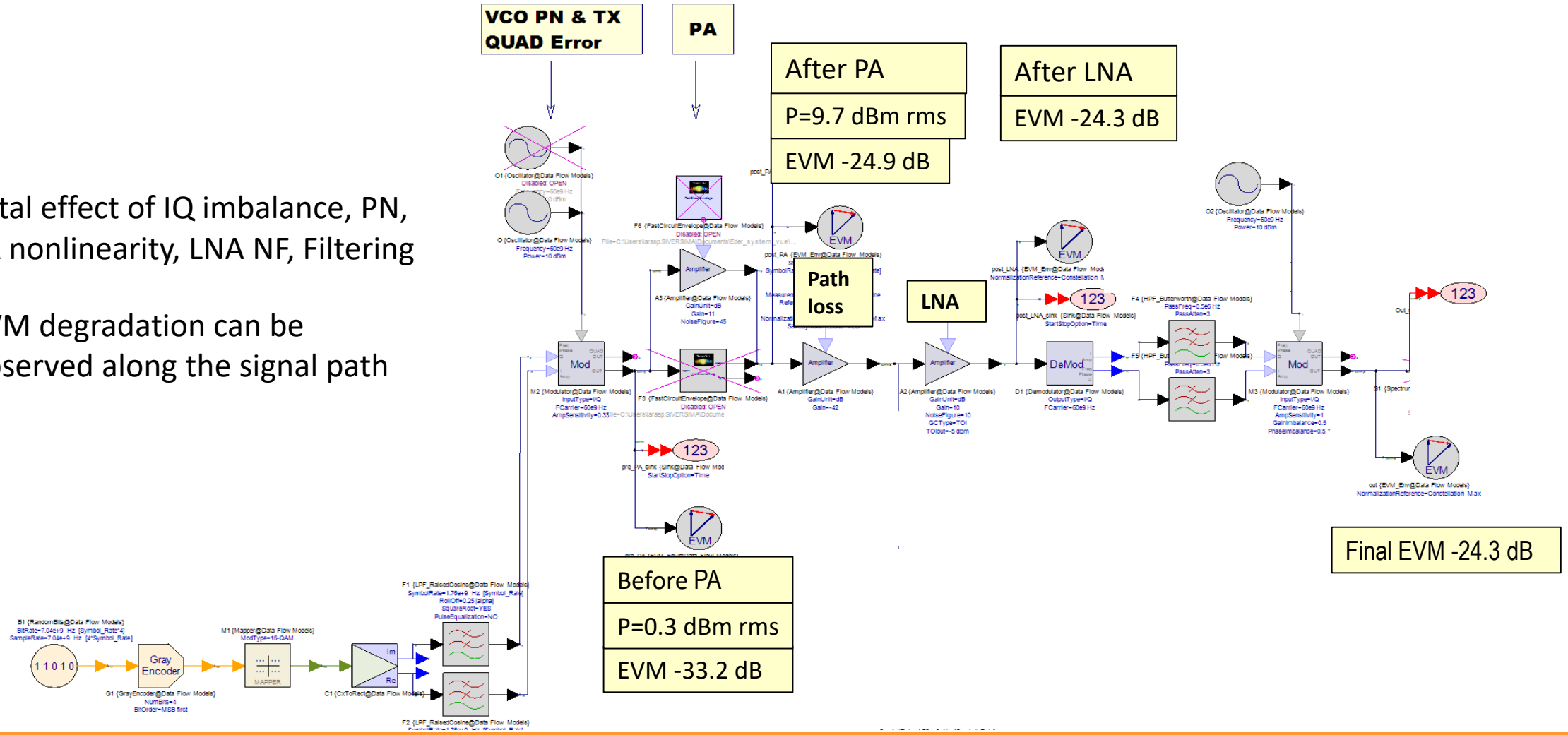


Chip Evaluation Results

- TX compression and EVM measurements
- RX NF and EVM measuremens
- Synthesizer phase-noise compared to simulations
- Beam-steering results with a PCB patch-array antenna
- Over-the-Air (OTA) full system tests up to 10 Gbit/s

Full TX-RX System Analysis using SystemVue and FCEs

- Total effect of IQ imbalance, PN, PA nonlinearity, LNA NF, Filtering
- EVM degradation can be observed along the signal path



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Beamsteering 60GHz TRX Comparison

Reference	Technology/ Configuration	Oper. freq. [GHz]	Combined Output Power/P1dB [dBm]	Phase noise [dBc@1MHz]	DC power [W]
Emami *et al*, ISSCC 2011 (Sibeam)	65nm CMOS 32RX+8TX	59.4-63.72	28 dBm EIRP	-96	0.9-2.2
Boers *et al*, JSSC 2014 (Broadcom)	40nm CMOS 16RX+16TX	57-66	24 dBm EIRP	-	0.96-1.2
Valdes-Garcia *et al*, JSSC 2010 (IBM)	130nm SiGe 16 TX (sep. RX)	51-65	21-25.5	-90 to -87	3.8-6.4
This work	130nm SiGe 16RX+16TX	57-71	22 (57-66 GHz) 20 (66-71 GHz) **>40 dBm EIRP (20 dBi ant.)**	-101	2.6 - 5

Conclusion

- A 60-GHz 16-ch beam-steering transceiver demonstrated capable of **+40dBm EIRP** when used with a 20 dBi PCB antenna array
- The frequency range **57-71 GHz** covered with wide-band matching and VCO design techniques
- **ADS Momentum** used for custom inductors/transformers and full sub-circuit passive modelling
- Phase-noise performance of **-101 dBc@ 1 MHz** supports **256QAM** modulation across OTA link
- **GoldenGate and Virtual Test Benches (VTBs)** used in circuit design on transistor level. Delivers EVM and spectrum estimations with 802.11ad waveforms in the Cadence environment
- **Fast Circuit Envelope (FCE) models exported to SystemVue** to refine system simulation
- **GoldenGate** speed and convergence supported top level simulations of full TX/RX path