PCI Express RX and LinkEQ Testing

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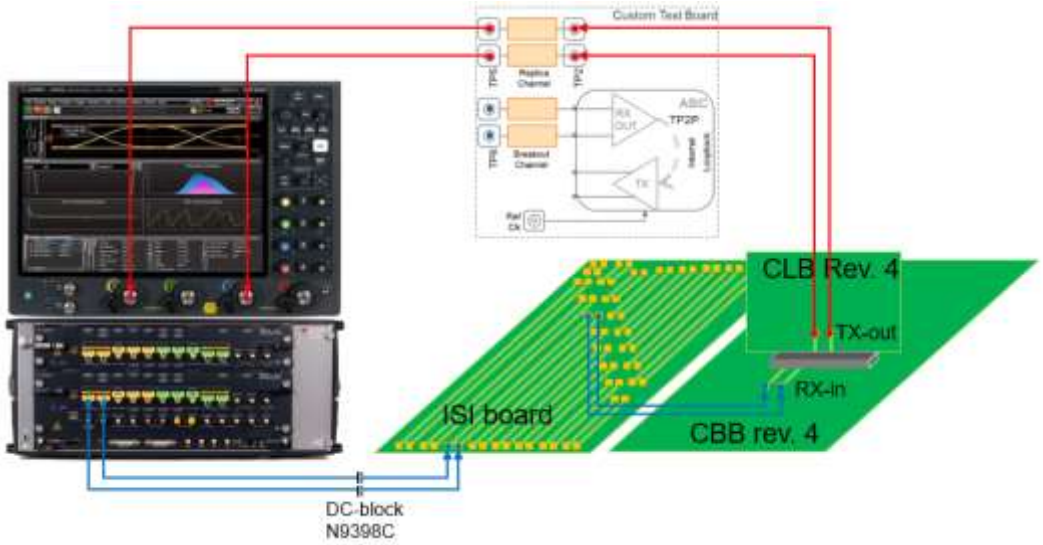
2019 OCT

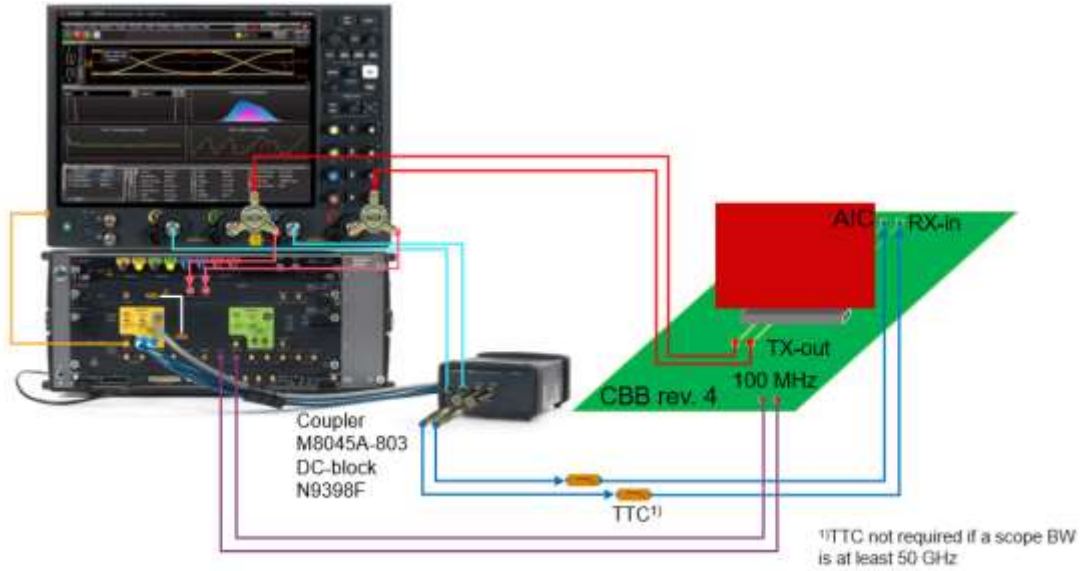
Keysight Electrical RX Test Solution Planning

Agenda

Agenda

Keysight PCI Express Receiver Test Solutions





- Versatile – tailored solutions for both the computer and server application spaces
- Proven – M8000 BERT Series has been an effective tool for both compliance workshop testing and pathfinding
- Accurate – vast experience in test automation combined with great instruments
- Integration – built-in pattern generator de-emphasis, reference clock multiplier and error detectors equipped with clock recovery and equalization

Differences between PCI Express 3 and PCI Express 4

	PCI Express 3.0/3.1	PCI Express 4.0 rev 0.5	PCI Express 4.0 rev 0.7
added transfer rate	8 GT/s	16 GT/s	
coding	128B/130B		
block alignment & scrambler reset	EIEOS for block alignment		
EIEOS	10 00FF 00FF 00FF 00FF 00FF 00FF 00FF 00FF ➔ 500 MHz	10 00FF 00FF 00FF 00FF 00FF 00FF 00FF 00FF ➔ 1 GHz	10 0000 FFFF 0000 FFFF 0000 FFFF 0000 FFFF ➔ 500 MHz
scrambling	control: no (partially), data: always PRBS 2^{23}-1; scrambler reset through EIEOS		
Adaptable TX link equalization	yes	yes, two step process: first 8G link eq followed by 16G link eq if 8G link eq is successful	
RX tests	stressed jitter test and stressed voltage test	one RX stress test	
rSSC for common reference clock	no	no	yes
eye opening after reference RX for stress signal cal	0.3 UI, 25 mV, BER of 10^{-12}	0.3 UI, 15 mV (RX eye spec. is actually 14 mV), BER of 10^{-12}	
stress signal adjustment using	RJ, DM-SI and V_{diff}	coarse: ISI fine: DM-SI + SJ or DM-SI + V_{diff}	
CTLE pole 1 frequency	2 GHz	4 GHz	2 GHz
Channel for RX test	No connector required	PCIe 4.0 CEM connector required as part of RX test channel	

Differences between PCI Express 3 and PCI Express 4

RELEVANT CHANGES WITH PCI EXPRESS 4.0 REV 0.5

	PCI Express 3.0/3.1	PCI Express 4.0 rev 0.5	PCI Express 4.0 rev 0.7
added transfer rate	8 GT/s	16 GT/s	
coding	128B/130B		
block alignment & scrambler reset	EIEOS for block alignment		
EIEOS	10 00FF 00FF 00FF 00FF 00FF 00FF 00FF 00FF ➔ 500 MHz	10 00FF 00FF 00FF 00FF 00FF 00FF 00FF 00FF ➔ 1 GHz	10 0000 FFFF 0000 FFFF 0000 FFFF 0000 FFFF ➔ 500 MHz
scrambling	Link EQ gets more important PRBS 2^{23}-1; scrambler reset through EIEOS		
Adaptable TX link equalization	yes	yes, two step process: first 8G link eq followed by 16G link eq if 8G link eq is successful	
RX tests	stressed jitter test and stressed voltage test	one RX stress test	
rSSC for common reference clock	no	no	yes
eye opening after reference RX for stress signal cal	Different cal procedure	mV (RX eye spec. is actually 14 mV), BER of 10^{-12}	
stress signal adjustment using	RJ, DM-SI and V_{diff}	coarse: ISI fine: DM-SI + SJ or DM-SI + V_{diff}	
Reference CTLE changes: pole 1 frequency ➔ affects RX cal	Special cal channel fixture required		2 GHz
Channel for RX test	No connector required	PCIe 4.0 CEM connector required as part of RX test channel	

Differences between PCI Express 3 and PCI Express 4

RELEVANT CHANGES FROM PCI EXPRESS 4.0 REV 0.5 TO PCI EXPRESS 4.0 REV 0.7

	PCI Express 3.0/3.1	PCI Express 4.0 rev 0.5	PCI Express 4.0 rev 0.7
added transfer rate	8 GT/s	16 GT/s	
coding			
block alignment & scrambler reset	EIEOS for block alignment		
EIEOS	10 00FF 00FF 00FF 00FF 00FF 00FF 00FF 00FF ➔ 500 MHz	10 00FF 00FF 00FF 00FF 00FF 00FF 00FF 00FF ➔ 1 GHz	10 0000 FFFF 0000 FFFF 0000 FFFF 0000 FFFF ➔ 500 MHz
scrambling	control: no (partially), data: always PRBS $2^{23}-1$; scrambler reset through EIEOS		
Adaptable TX link		yes, two step process: first 8G link eq followed by 16G link eq if 8G link eq is successful	
RX tests	stressed jitter test and stressed voltage test	one RX stress test	
rSSC for common reference clock	no	no	yes
eye opening after reference RX for stress signal cal	0.3 UI, 25 mV, BER of 10^{-12}	0.3 UI, 15 mV (RX eye spec. is actually 14 mV), BER of 10^{-12}	
stress signal adjustment using	RJ, DM-SI and V_{diff}	coarse: ISI fine: DM-SI + SJ or DM-SI + V_{diff}	
Channel for RX test	No connector required	PCIe 4.0 CEM connector required as part of RX test channel	

Affects block alignment and descrambler reset

A new type of impairment. Amplitude is significantly higher compared to PCIe 2.0

Differences between PCI Express 4 and PCI Express 5

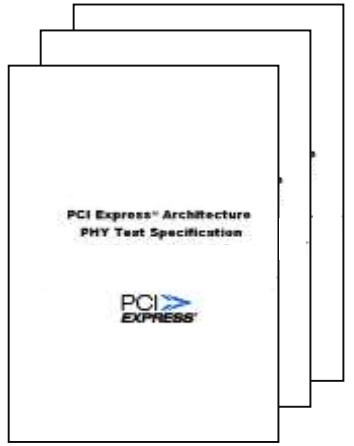
	PCI Express 3.0/3.1	PCI Express 4.0	PCI Express 5.0 rev 0.9
added transfer rate	8 GT/s	16 GT/s	32 GT/s
Coding for added transfer rate	128B/130B		
block alignment & scrambler reset for added transfer rate	EIEOS for block alignment		
EIEOS for added transfer rate	10 00FF 00FF 00FF 00FF 00FF 00FF 00FF 00FF ➔ 500 MHz	10 0000 FFFF 0000 FFFF 0000 FFFF 0000 FFFF ➔ 500 MHz	10 0000 0000 FFFF FFFF 0000 0000 FFFF FFFF 10 0000 0000 FFFF FFFF 0000 0000 FFFF FFFF ➔ 500 MHz, but EIEOS @ 32 GT/s is now 2 blocks
Scrambling for added transfer rate	control: no (partially), data: always PRBS 2^{23}-1; scrambler reset through EIEOS		
Precoder for added transfer rate	no	no	Yes, but can be deactivated upon request from RX
Adaptable TX link equalization for added transfer rate	yes	yes, two step process: first 8G link eq followed by 16G link eq if 8G link eq is successful	yes, three step process: 8G, if successful try 16G, if successful try 32G. Optional bypass modes are available
RX tests	stressed jitter test and stressed voltage test. Different SJ masks for CC and IR	one RX stress test. But different SJ masks for CC and IR	One RX test same swept SJ masks applied for CC and IR plus additional 33kHz spur. Amplitude of spur differes between CC and IR. Swept SJ mask is different for 16G and 32G
rSSC for common reference clock	no	yes	no
eye opening after reference RX for stress signal cal	0.3 UI, 25 mV, BER of 10^{-12}	0.3 UI, 15 mV (RX eye spec. is actually 14 mV), BER of 10^{-12}	
stress signal adjustment using	RJ, DM-SI and V_{diff}	coarse: ISI fine: DM-SI + SJ + Vdiff	ISI + DM-SI + SJ + V_{diff} Preference on combination with higher channel loss

Agenda

- PCI Express Generic
- Challenge 1 – Which Test Setup Do You Need?
- Challenge 2 – PCI Express LTSSM
- Challenge 3 – PCI Express Stress Signal
- Challenge 4 – PCI Express RX and LinkEQ Tests
- Challenge 5 – Calibration / Test Complexity and Time
- Solution Overview
- Appendix

PCI Express

SPECIFICATION FRAMEWORK



Base Specification

- Contains all the system knowledge
- Can directly be applied to Chip Test

Form Factor Specifications

- Card Electromechanical (CEM) Spec
  - Applies to Add-In Cards and Mother Boards
  - Mitigates card manufacturer's need to study the base specification
  - Increases reproducibility through PCI-SIG supplied test tools CBB and CLB (compliance base and load board)
- U.2 Specification
- M.2 Specification
- …

Phy Test Specification

- Defines compliance tests of form factor spec in detail
- Different PHY Test Specifications for each form factor

PCI Express

WHICH TEST SETUP DO YOU NEED?

To answer this question we need additional information:

- What is your device under test (DUT)?
  - The answer to this question will help narrow down the specification type from the PCI Express specification framework which needs to be considered. Possible answers are
    - ASIC
    - A CEM DUT: System / mainboard or an add-in card
    - An U.2 DUT: An U.2 host or an U.2 device, e.g. a SSD
    - An M.2 DUT: An M.2 host or an M.2 device, e.g. a SSD
    - A RX in an embedded PCI Express application
    - Or something else
- What are the transfer rates you wish to test?
  - 32 GT/s
  - 16 GT/s
  - 8 GT/s
  - 5 GT/s
  - 2.5 GT/s
- According to which PCI Express Specification revisions do you want to test?
  - 5.0
  - 4.0
  - 3.1 / 3.0
  - 2.0
  - 1.1
  - 1.0

The answers to above questions help to decide on the best PCI Express RX and LinkEQ test solution for you.

PCI Express

LOOKUP SPECIFICATION TYPE

Device Type	32 GT/s	16 GT/s	8 GT/s	5 GT/s	2.5 GT/s
ASIC	Base Specification	Base Specification	Base Specification	Base Specification	Base Specification
CEM	PHY Architecture Test Specification for CEM	PHY Architecture Test Specification for CEM	PHY Architecture Test Specification for CEM	(CEM Specification)	(CEM Specification)
U.2	n/a	n/a	PHY Architecture Test Specification for U.2	n/a	n/a
M.2	n/a	n/a	PHY Architecture Test Specification for M.2	n/a	n/a
Other	Base Specification	Base Specification	Base Specification	Base Specification	Base Specification

2019/04/09

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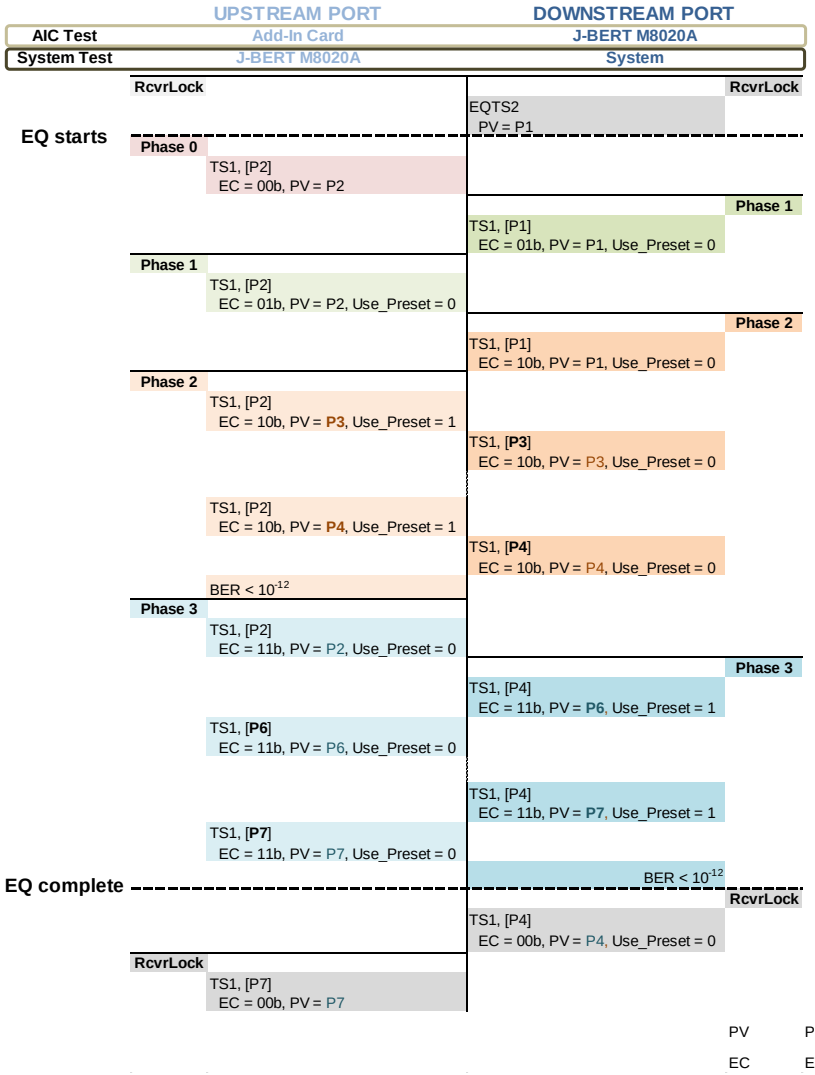
Dynamic Link Equalization Handshake 8 GT/s

THE FOUR PHASES OF THE LINK EQUALIZATION PROTOCOL



Phase 0:

- 2.5 Gb/s
- Downstream port tells upstream port which initial preset to use after the speed change will have been done.

Phase 1:

- 8 Gb/s
- Link partners settle on 8 GT/s speed.
- Exchange FS/LF values.

Phase 2:

- 8 Gb/s
- Add-in Card sets up the de-emphasis of the System Board's transmitter.

Phase 3:

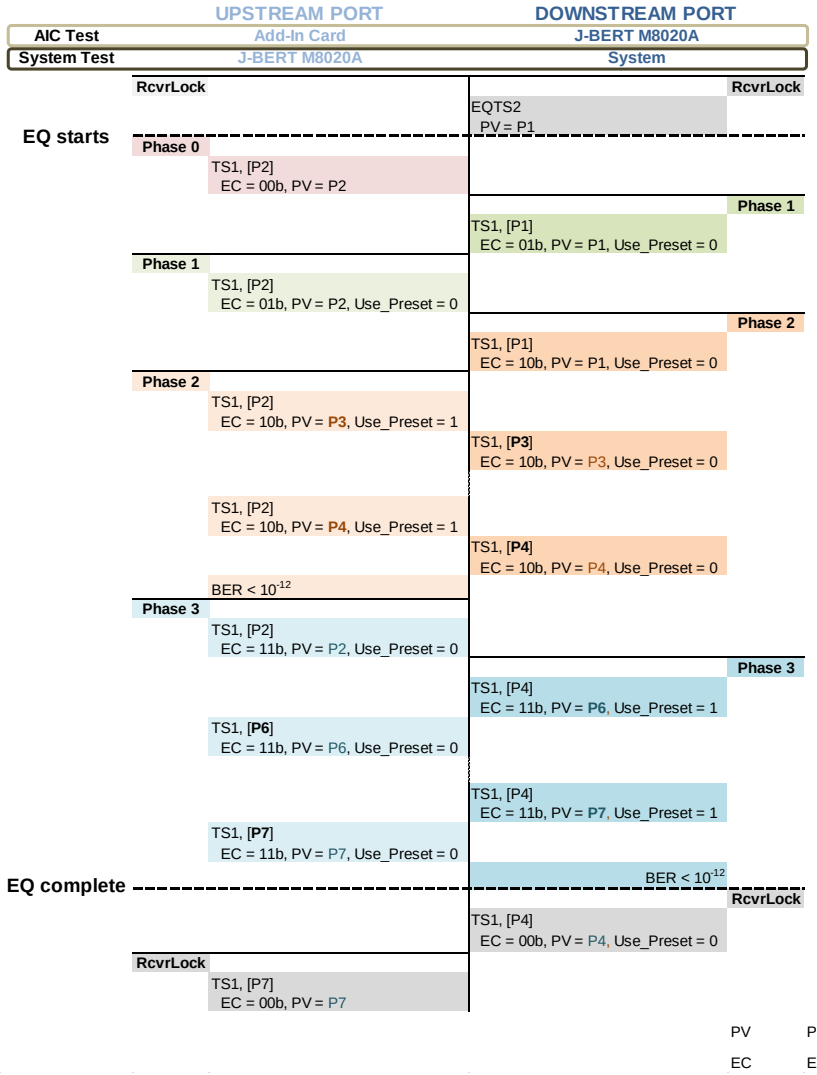
- 8 Gb/s
- System Board sets up the de-emphasis of the Add-in Card's transmitter.

PV Preset Value

EC Equalization Control

Dynamic Link Equalization Handshake 16 GT/s

THE FOUR PHASES OF THE LINK EQUALIZATION PROTOCOL



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- Downstream port tells upstream port which initial preset to use after the speed change will have been done.

Phase 1:
- 8 Gb/s
- Link partners settle on 8 GT/s speed.
- Exchange FS/LF values.

Phase 2:
- 8 Gb/s
- Add-in Card sets up the de-emphasis of the System Board's transmitter.

Phase 3:
- 8 Gb/s
- System Board sets up the de-emphasis of the Add-in Card's transmitter.

IF SUCCESSFUL

Phase 0:
- 8 Gb/s
- Downstream port tells upstream port which initial preset to use after the speed change will have been done.

Phase 1:
- 16 Gb/s
- Link partners settle on 16 GT/s speed.
- Exchange FS/LF values.

Phase 2:
- 16 Gb/s
- Add-in Card sets up the de-emphasis of the System Board's transmitter.

Phase 3:
- 16 Gb/s
- System Board sets up the de-emphasis of the Add-in Card's transmitter.

PV Preset Value

EC Equalization Control

Dynamic Link Equalization Handshake 32 GT/s

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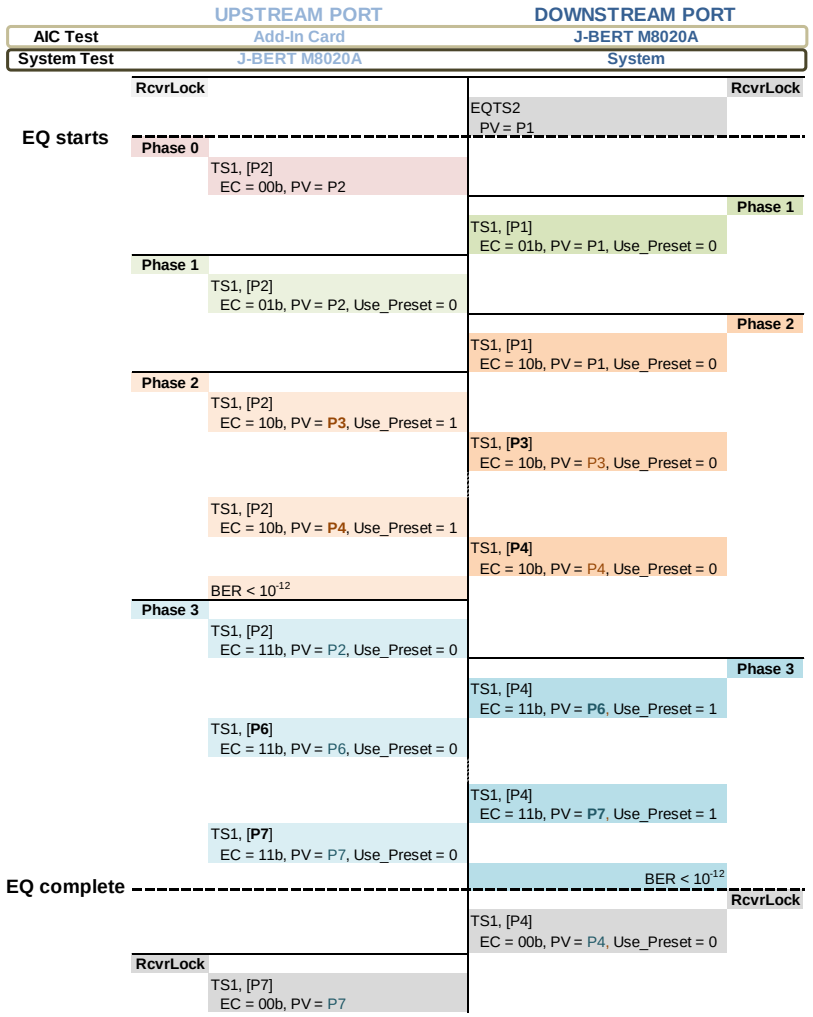

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- 8 Gb/s
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Phase 3:
- 8 Gb/s
- System Board sets up the de-emphasis of the Add-in Card's transmitter.

IF SUCCESSFUL

Phase 0:
- 8 Gb/s
- Downstream port tells upstream port which initial preset to use after the speed change will have been done.

Phase 1:
- 16 Gb/s
- Link partners settle on 16 GT/s speed.
- Exchange FS/LF values.

Phase 2:
- 16 Gb/s
- Add-in Card sets up the de-emphasis of the System Board's transmitter.

Phase 3:
- 16 Gb/s
- System Board sets up the de-emphasis of the Add-in Card's transmitter.

IF SUCCESSFUL

Phase 0:
- 16 Gb/s
- Downstream port tells upstream port which initial preset to use after the speed change will have been done.

Phase 1:
- 32 Gb/s
- Link partners settle on 16 GT/s speed.
- Exchange FS/LF values.

Phase 2:
- 32 Gb/s
- Add-in Card sets up the de-emphasis of the System Board's transmitter.

Phase 3:
- 32 Gb/s
- System Board sets up the de-emphasis of the Add-in Card's transmitter.

M8000 Setup – PCI Express

LTSSM LOG – EXAMPLE FOR END POINT – TIMING OF LTSSM STEPS – 16 GT/S

Link Training Logging for M1.DataOut1 at 11/09/2018 13:42:59

State	Execution Time	Transfer Rate
Detect.Active	1,04864 ms	2.5 GT/s
Polling.Active	2,097184 ms	2.5 GT/s
Polling.Configuration	1,36 us	2.5 GT/s
Configuration.Linkwidth.Start	2,192 us	2.5 GT/s
Configuration.Linkwidth.Accept	256 ns	2.5 GT/s
Configuration.Lanenum.Wait	2,208 us	2.5 GT/s
Configuration.Lanenum.Accept	544 ns	2.5 GT/s
Configuration.Complete	3,296 us	2.5 GT/s
Configuration.Idle	240 ns	2.5 GT/s
L0	224 ns	2.5 GT/s
Recovery.RcvrLock	2,8 us	2.5 GT/s
Recovery.RcvrCfg	2,512 us	2.5 GT/s
Recovery.Speed	10,608 us	2.5 GT/s
Recovery.RcvrLock	448 ns	8.0 GT/s
Recovery.Equalization.Phase1	131,328 us	8.0 GT/s
Recovery.Equalization.Phase2	14,578208 ms	8.0 GT/s
Recovery.Equalization.Phase3	1,12 us	8.0 GT/s
Recovery.RcvrLock	1,84 us	8.0 GT/s
Recovery.RcvrCfg	640 ns	8.0 GT/s
Recovery.Idle	1,328 us	8.0 GT/s
L0	224 ns	8.0 GT/s
Recovery.RcvrLock	1,936 us	8.0 GT/s
Recovery.RcvrCfg	800 ns	8.0 GT/s
Recovery.Speed	9,248 us	8.0 GT/s
Recovery.RcvrLock	448 ns	16.0 GT/s
Recovery.Equalization.Phase1	141,568 us	16.0 GT/s
Recovery.Equalization.Phase2	6,850304 ms	16.0 GT/s
Recovery.Equalization.Phase3	1,408 us	16.0 GT/s
Recovery.RcvrLock	288 ns	16.0 GT/s
Recovery.RcvrCfg	1,424 us	16.0 GT/s
Recovery.Idle	112 ns	16.0 GT/s
Loopback.Entry	2,144 us	16.0 GT/s
Loopback.Active	-	16.0 GT/s

M8000 Setup – PCI Express

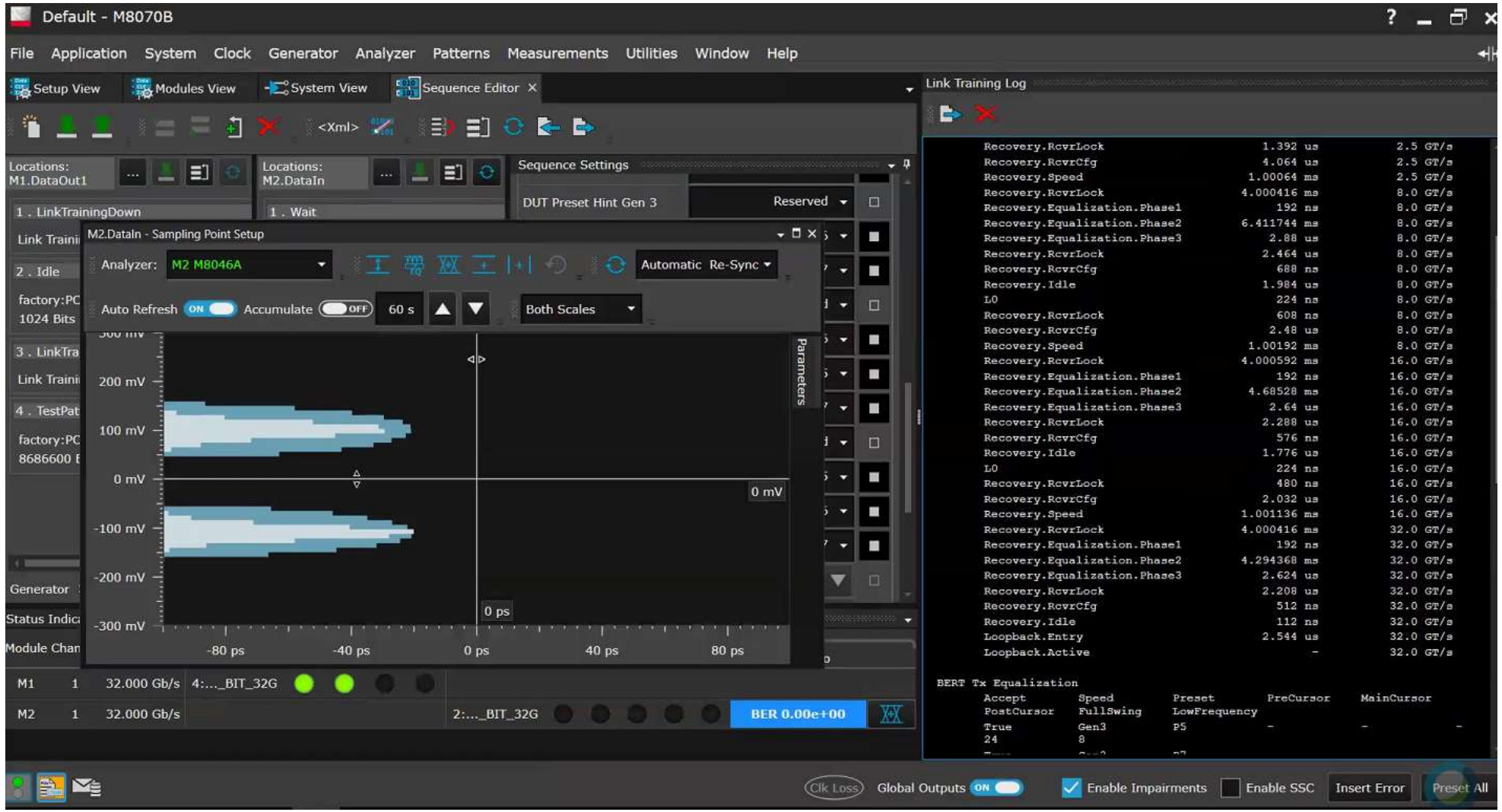
LTSSM LOG – EXAMPLE FOR END POINT – CHANGE REQUESTS TO BERT

BERT Tx Equalization

Accept	Speed	Preset	PreCursor	MainCursor	PostCursor	FullSwing	LowFrequency
True	Gen3	P8	-	-	-	24	8
True	Gen3	P0	-	-	-	24	8
True	Gen3	P1	-	-	-	24	8
True	Gen3	P2	-	-	-	24	8
True	Gen3	P3	-	-	-	24	8
True	Gen3	P4	-	-	-	24	8
True	Gen3	P5	-	-	-	24	8
True	Gen3	P6	-	-	-	24	8
True	Gen3	P7	-	-	-	24	8
True	Gen3	P8	-	-	-	24	8
True	Gen3	P9	-	-	-	24	8
False	Gen3	10	-	-	-	24	8
True	Gen3	P6	-	-	-	24	8
True	Gen3	P8	-	-	-	24	8
True	Gen4	P7	-	-	-	24	8
True	Gen4	P0	-	-	-	24	8
True	Gen4	P1	-	-	-	24	8
True	Gen4	P2	-	-	-	24	8
True	Gen4	P3	-	-	-	24	8
True	Gen4	P4	-	-	-	24	8
True	Gen4	P5	-	-	-	24	8
True	Gen4	P6	-	-	-	24	8
True	Gen4	P7	-	-	-	24	8
True	Gen4	P8	-	-	-	24	8
True	Gen4	P9	-	-	-	24	8
False	Gen4	10	-	-	-	24	8
True	Gen4	P9	-	-	-	24	8

M8040A

PCI EXPRESS 5 32G LTSSM – ENDPOINT – REAL DATA, NO FAKE!



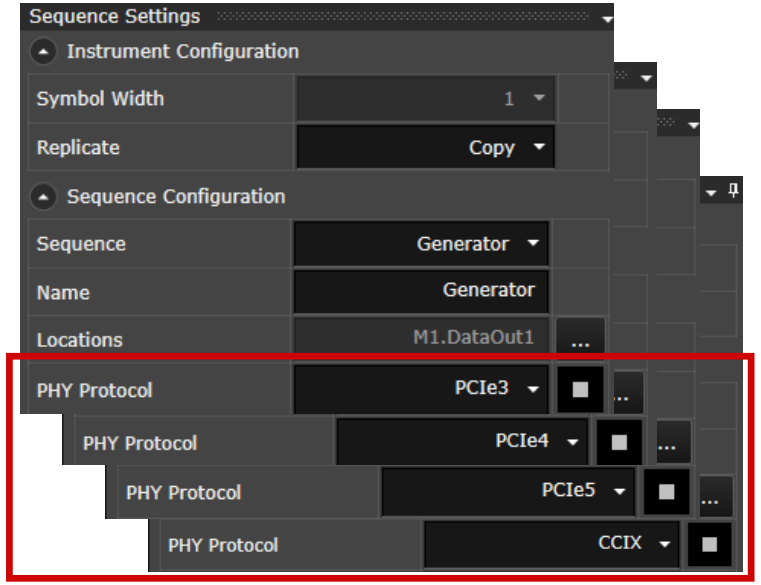
M8040A

PCI EXPRESS 5 32G LTSSM – ENDPOINT – REAL DATA, NO FAKE!

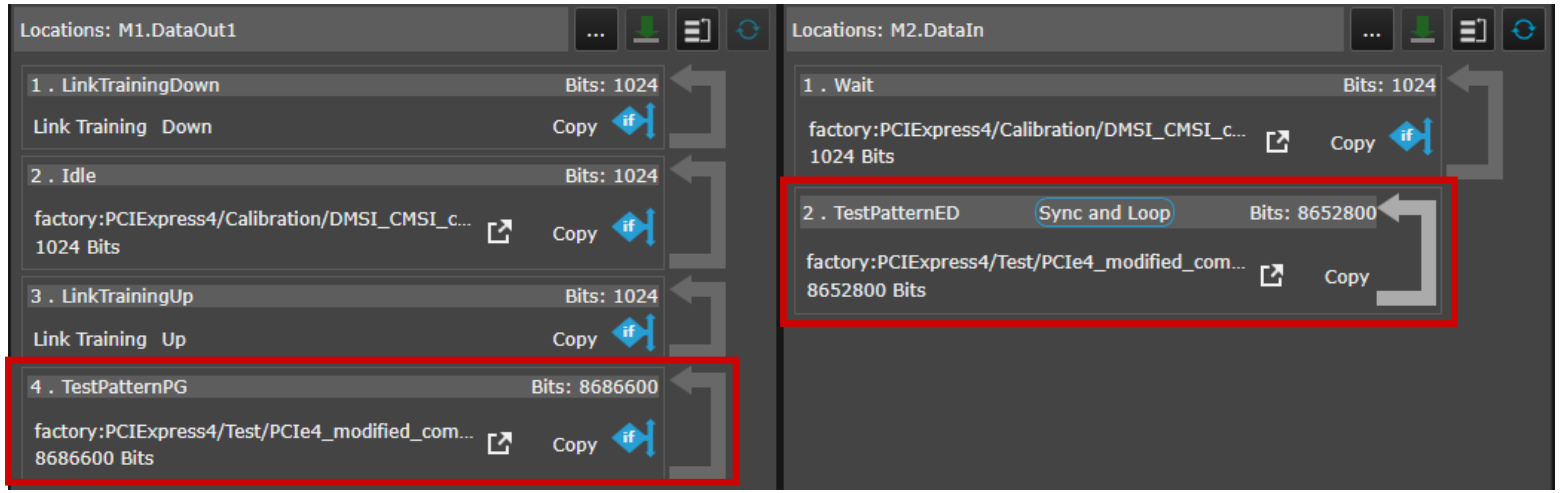
BERT Tx Equalization

Accept	Speed	Preset	PreCursor	MainCursor	PostCursor	FullSwing	LowFrequency
True	Gen3	P5	-	-	-	24	8
True	Gen3	P7	-	-	-	24	8
True	Gen3	P8	-	-	-	24	8
True	Gen3	P0	-	-	-	24	8
True	Gen3	P3	-	-	-	24	8
True	Gen3	-	3	18	3	24	8
True	Gen4	P7	-	-	-	24	8
True	Gen4	P8	-	-	-	24	8
True	Gen4	P0	-	-	-	24	8
True	Gen4	-	3	18	3	24	8
True	Gen4	-	3	18	0	24	8
True	Gen4	P6	-	-	-	24	8
True	Gen5	P5	-	-	-	24	8
True	Gen5	P7	-	-	-	24	8
True	Gen5	P4	-	-	-	24	8
True	Gen5	P8	-	-	-	24	8
True	Gen5	P0	-	-	-	24	8
True	Gen5	-	2	17	5	24	8

M8040 Setup – PCI Express / CCIX – SKP OS Filtering

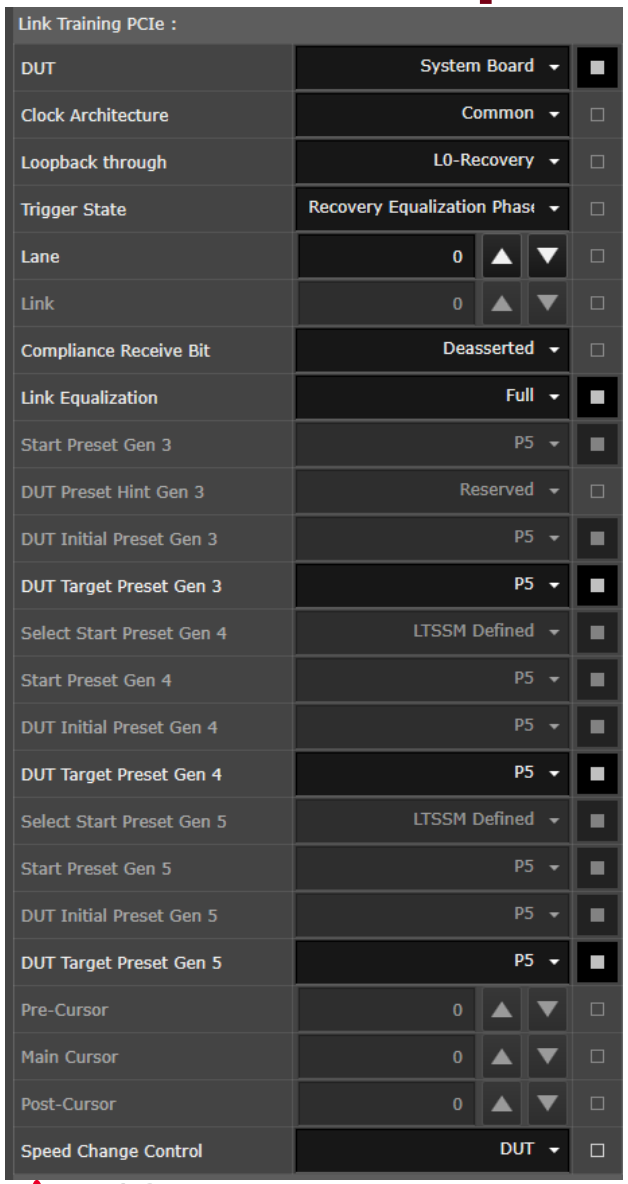


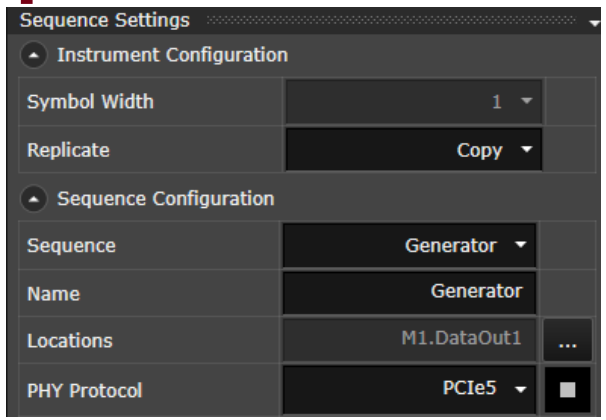
- The PHY Protocol settings defines the protocol applied for SKP OS filtering. Possible choices are
  - PCIe2 – PCI Express 2.0 5 GT/s SKP OS
  - PCIe3 – PCI Express 3.0 8 GT/s SKP OS & EIEOS definition
  - PCIe4 – PCI Express 4.0 16 GT/s SKP OS & EIEOS definition
  - PCIe5 – PCI Express 5.0 32 GT/s SKP OS & EIEOS definition
  - CCIX – CCIX 20 GT/s / 25 GT/s SKP OS & EIEOS definition



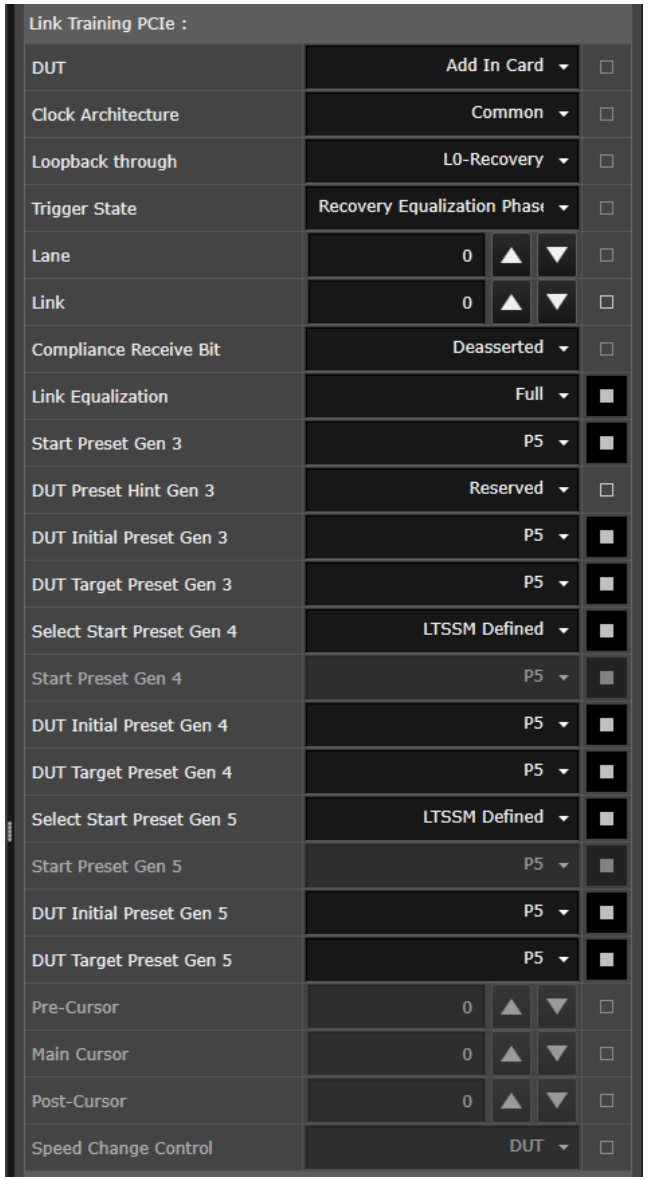
- The test pattern used must be generator in two versions
  - The pattern used for the pattern generator must have the required SKP OS embedded
  - The pattern used as expected pattern for the error detector must not have any SKP OS embedded. The error detector will remove all detected SKP OS from the received data stream and will compare the such filtered incoming pattern against the expected pattern
- The M8000 factory pattern library contains respective modified compliance test patterns for pattern generator and error detector for above PHY protocol selections for CC and IR clocking modes

M8040 Setup – PCI Express LTSSM – 32 GT/s

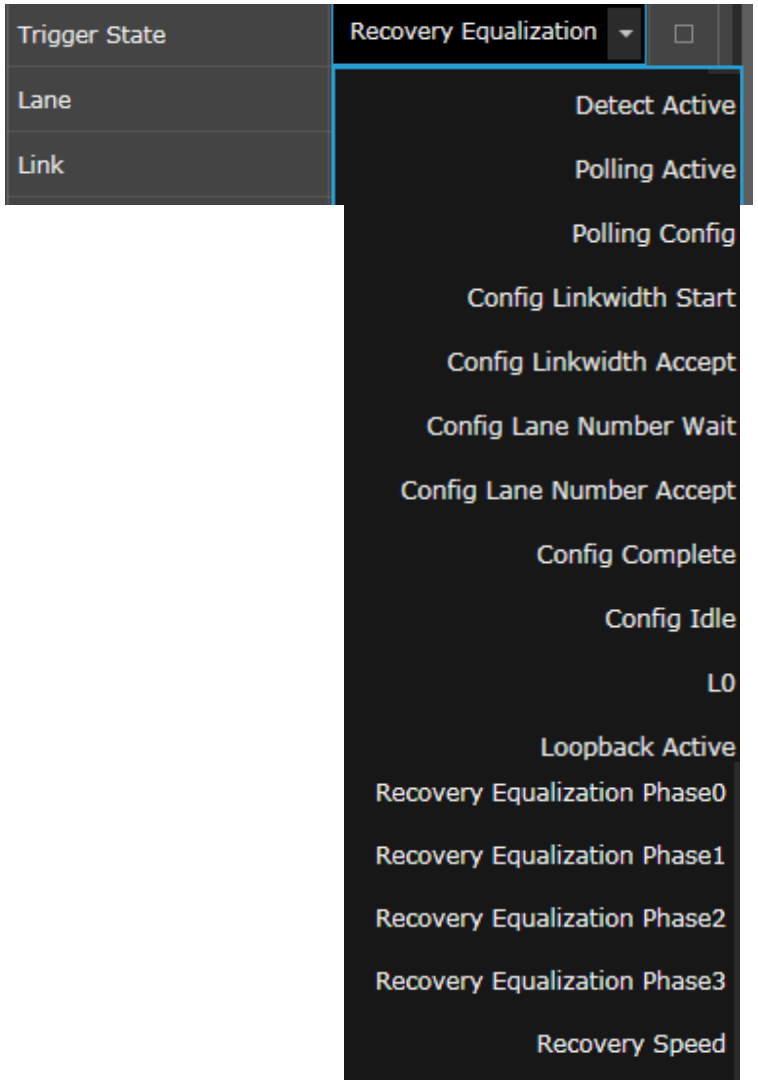




- PHY Protocol needs to be set to PCIe5
- Select DUT type
  - Any endpoint device ➔ Add In Car
  - Any root complex device ➔ System Board
- Two sets of phase 0 through phase 3 parameter
  - 2.5 GT/s to 8 GT/s
    - DUT Target Preset can be presets only
  - 8 GT/s to 16 GT/s
    - DUT Target Preset 4 can be presets or coefficients
- Select Start Preset Gen 4 / Gen 5
  - User Defined
    - User can define the preset which is used for 16 GT/s / 32 GT/s phase 1
  - LTSSM Defined
    - Result of 8 GT/s / 16 GT/s TxEQ negotiation is used for 16 GT/s / 32 GT/s phase 1
- Speed Change Control:
  - While the root complex usually is responsible for initiating the speed change, most root complex today need the RX test equipment to take control of the speed change.
- Speed bypass modes of PCI Express 5 are not supported

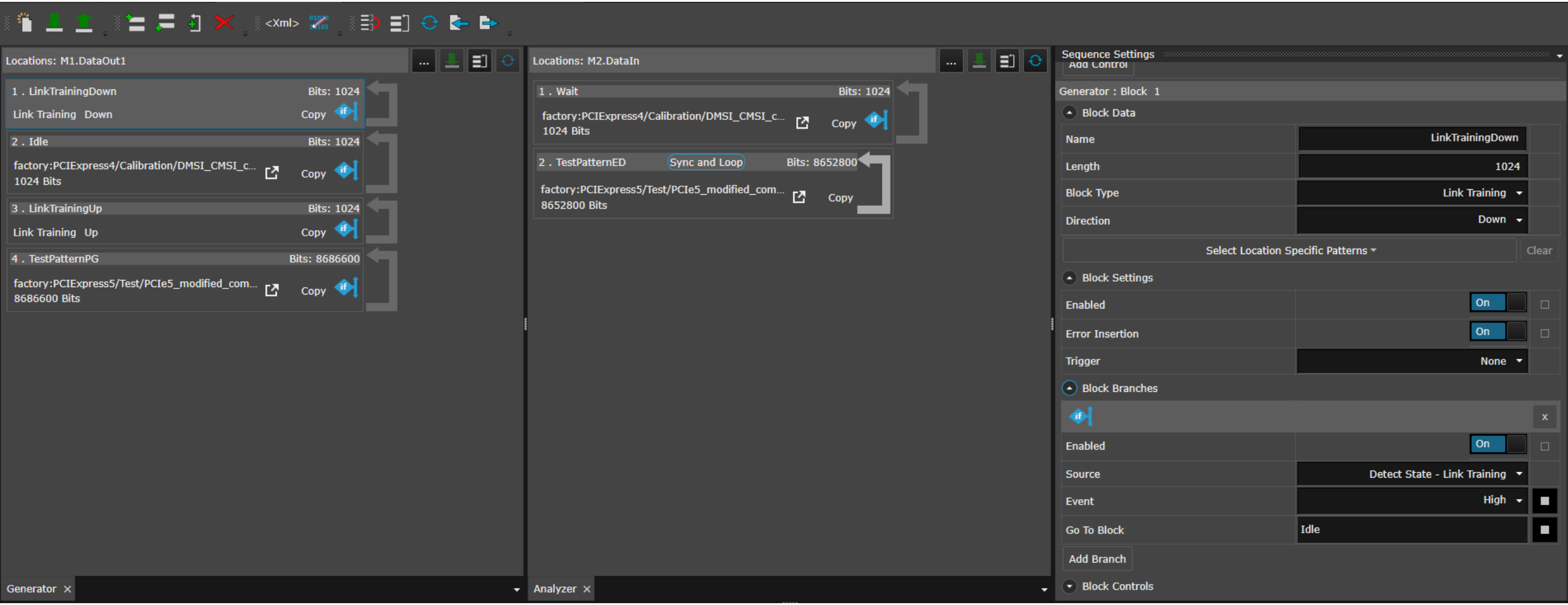


M8040A Setup – PCI Express LTSSM – LTSSM Trigger



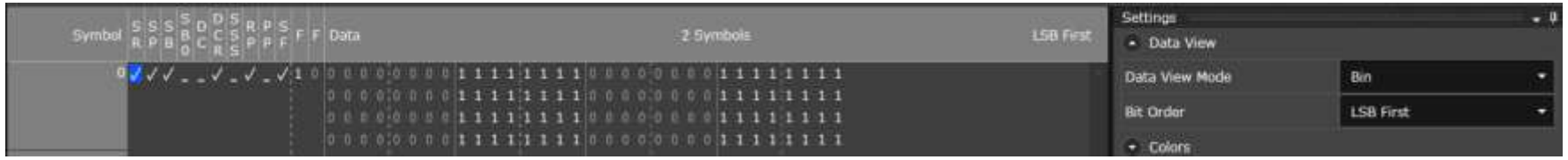
- Extended selection of LTSSM states for trigger signal enable debug in addition to TX link eq tests 1)
- Phase 2 and Phase 3 presets are required for Link EQ tests
- Additional presets can be used to debug training issues by triggering scope captures of respective LTSSM state

M8040A Setup – PCI Express LTSSM – Sequence

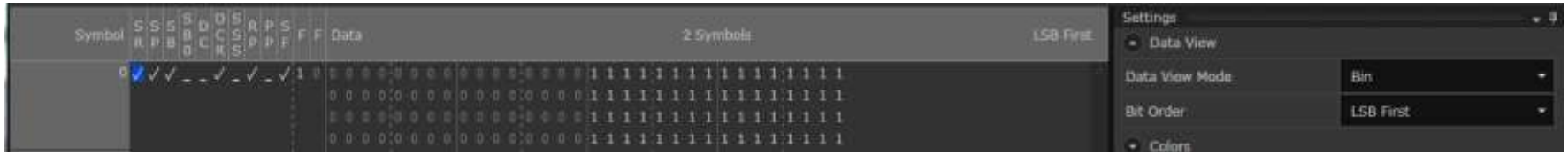


J-BERT M8020A Setup – PCI Express – SKP OS Filtering

EIEOS for 8 GT/s

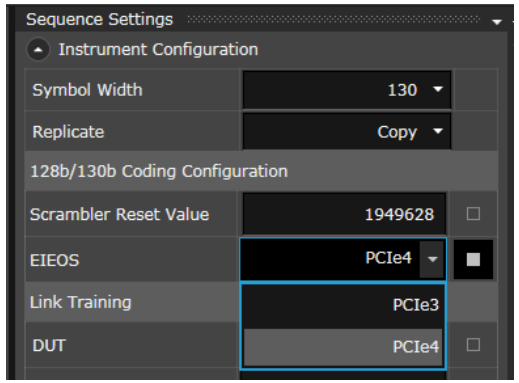


EIEOS for 16 GT/s



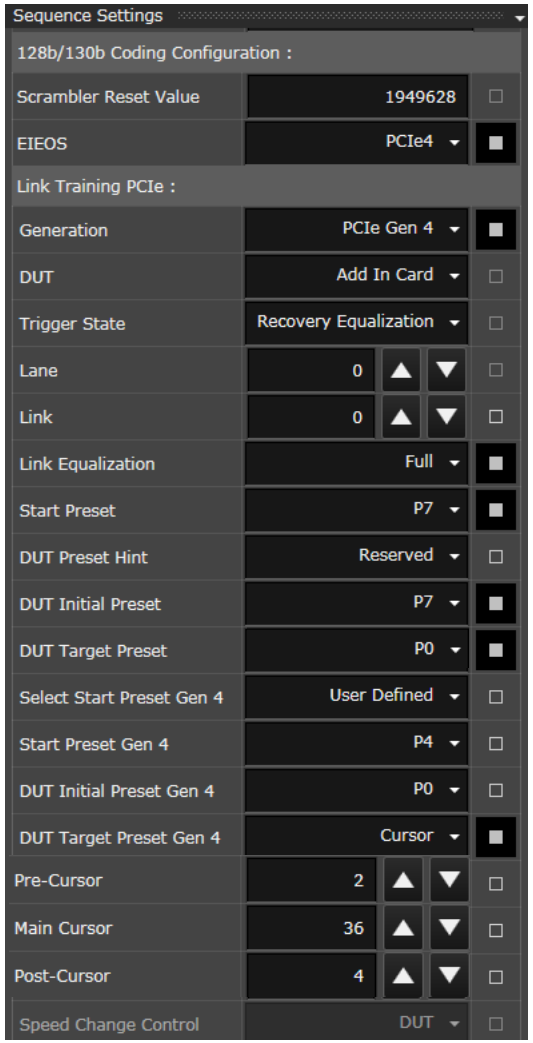
Modified Compliance Pattern

Sequence / Coding Configuration

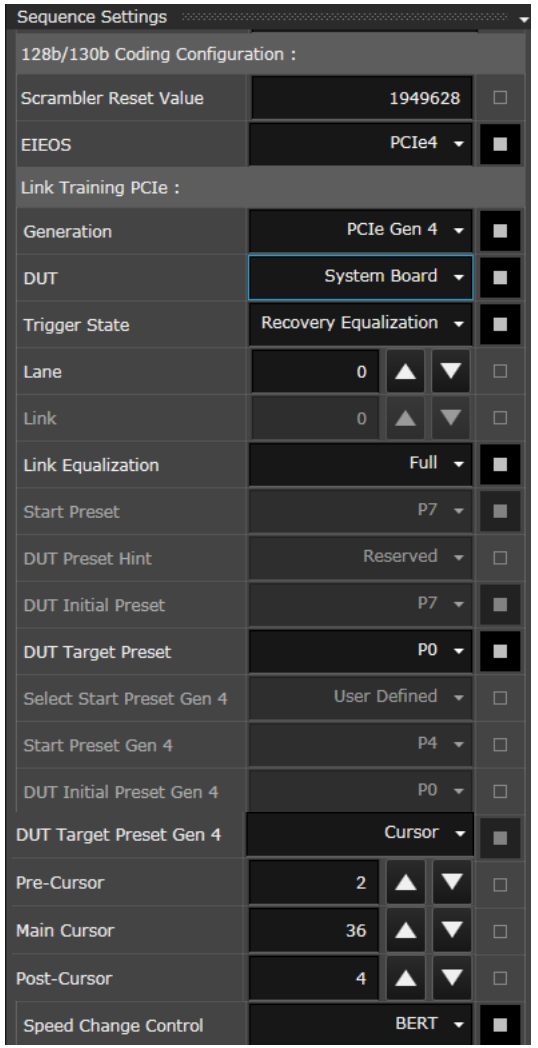


- Memory granularity fits to 128b/130b Coding
- Scrambling and descrambling in HW allows best use of memory
- ED uses EIEOS for block synchronization and descrambler reset
- ED filters SKP OS

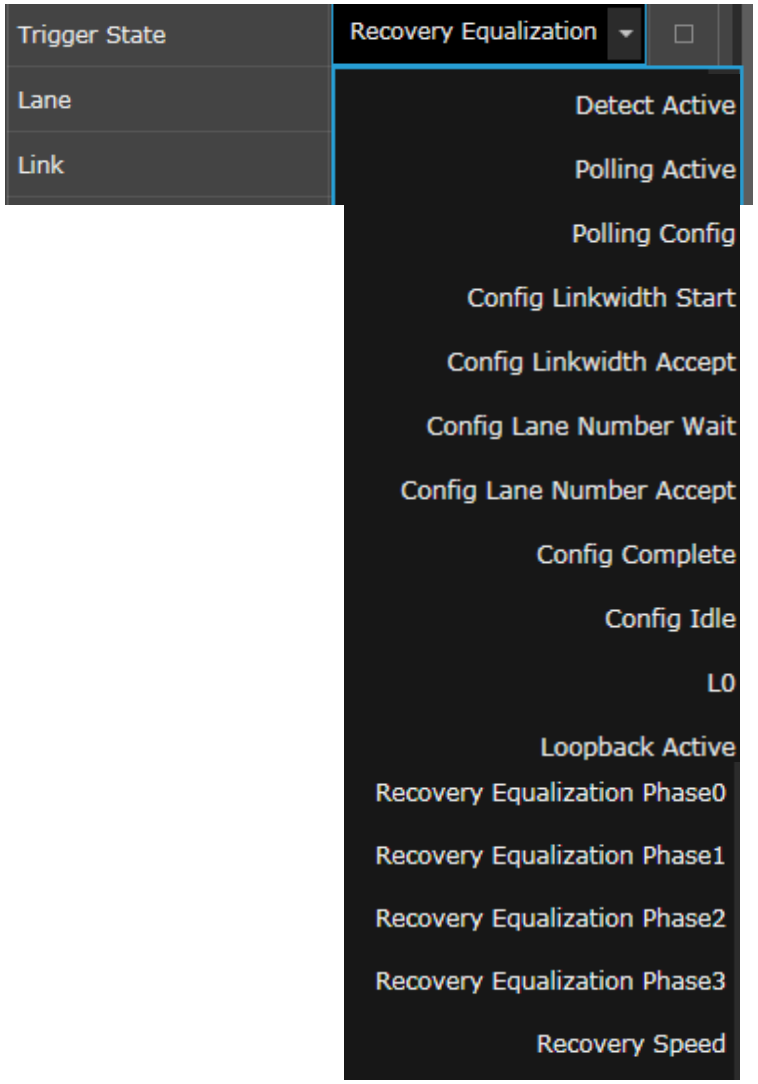
J-BERT M8020A Setup – PCI Express LTSSM – 16 GT/s



- EIEOS needs to be set to PCIe3 for PCI Express Base Specification 4.0 rev 0.5. But for PCI Express Base Specification 4.0 rev 0.7 and higher it needs to be set PCIe4!
- Generation needs to be set to PCIe Gen 4
- Select DUT type
  - Any endpoint device ➔ Add In Car
  - Any root complex device ➔ System Board
- Two sets of phase 0 through phase 3 parameter
  - 2.5GT/s to 8GT/s
    - DUT Target Preset can be presets only
  - 8GT/s to 16GT/s
    - DUT Target Preset 4 can be presets or coefficients
- Speed Change Control:
  - While the root complex usually is responsible for initiating the speed change, most root complex today need the RX test equipment to take control of the speed change.

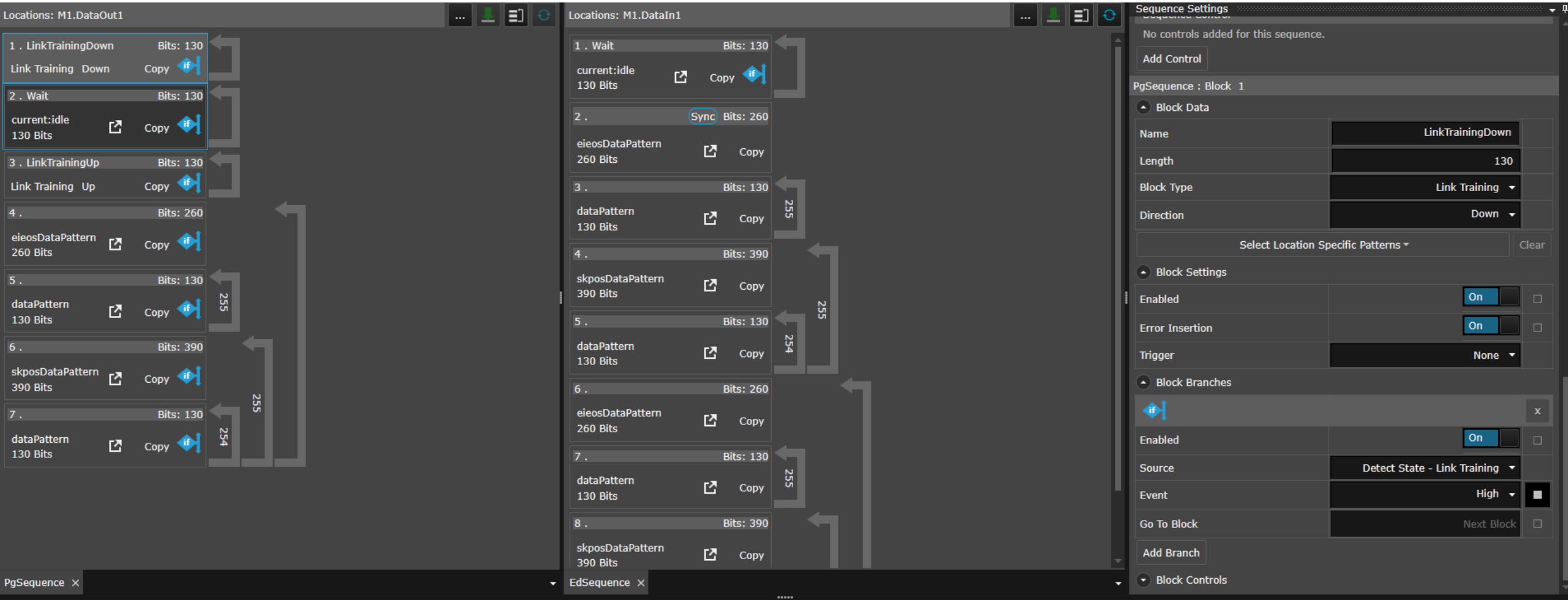


J-BERT M8020A Setup – PCI Express – LTSSM Trigger



- Extended selection of LTSSM states for trigger signal enable debug in addition to TX link eq tests 1)
- Phase 2 and Phase 3 presets are required for Link EQ tests
- Additional presets can be used to debug training issues by triggering scope captures of respective LTSSM state

M8020A Setup – PCI Express LTSSM – Sequence

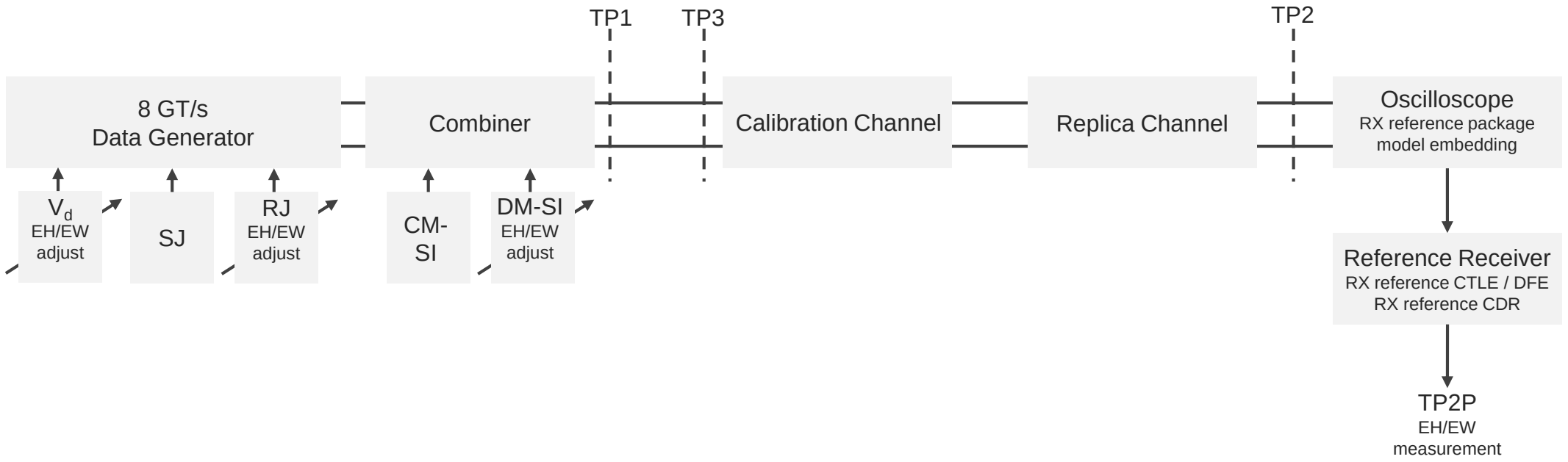


Agenda

- PCI Express Generic
- Challenge 1 – Which Test Setup Do You Need?
- Challenge 2 – PCI Express LTSSM
- Challenge 3 – PCI Express Stress Signal
- Challenge 4 – PCI Express RX and LinkEQ Tests
- Challenge 5 – Calibration / Test Complexity and Time
- Solution Overview
- Appendix

PCI Express 4.0 – Base Specification

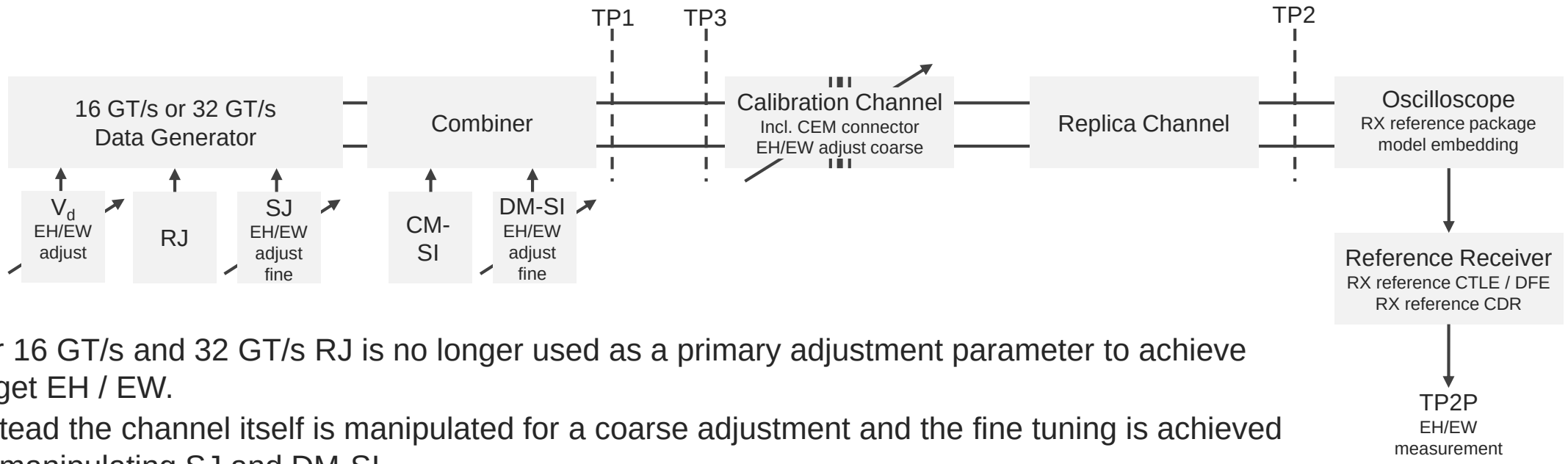
RX STRESS SIGNAL CALIBRATION SETUP FOR 8 GT/s



- In case SIGTEST is used the RX reference package model embedding is not done on the oscilloscope but by SIGTEST. This applies to 8 GT/s only

PCI Express 4.0 – Base Specification

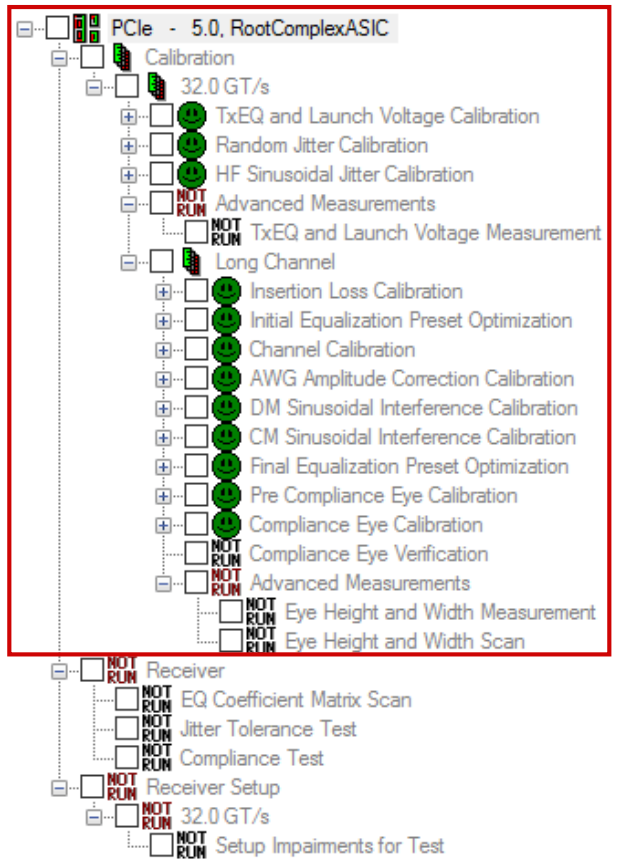
RX STRESS SIGNAL CALIBRATION SETUP FOR 16 GT/s & 32 GT/s



- For 16 GT/s and 32 GT/s RJ is no longer used as a primary adjustment parameter to achieve target EH / EW.
- Instead the channel itself is manipulated for a coarse adjustment and the fine tuning is achieved by manipulating SJ and DM-SI
- The intention was to achieve a more realistic stress signal
- RX reference package model embedding is no longer done in SIGTEST for 16 GT/s and 32 GT/s but on the scope itself

PCI Express 5.0 – Base Specification

CALIBRATION STEPS 32 GT/s RX STRESS SIGNAL



TP3 Calibration Steps

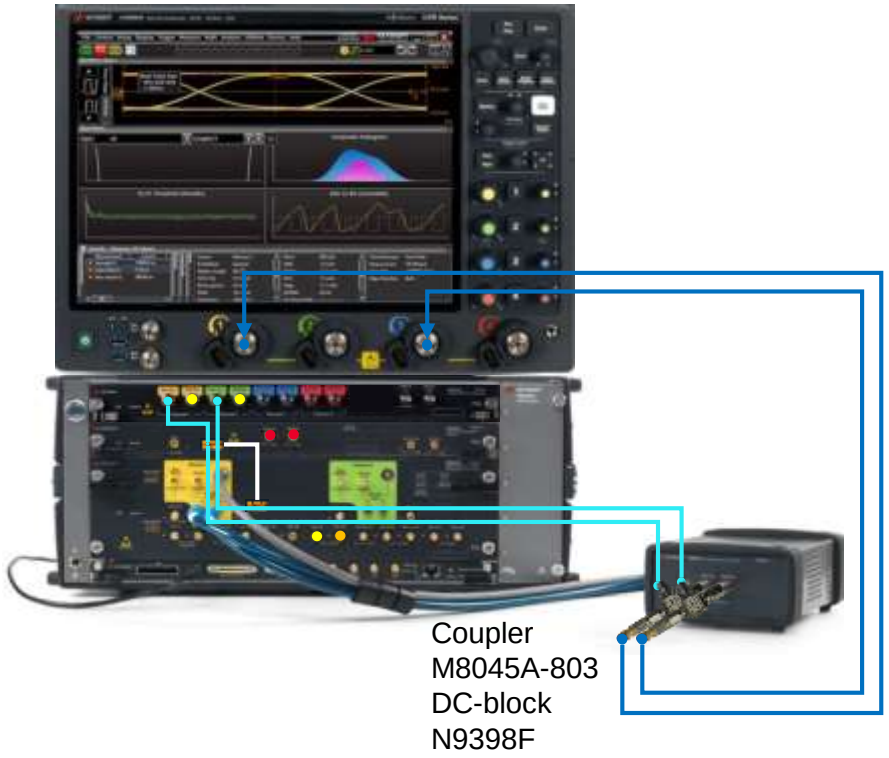
- Launch voltage, preshoot and de-emphasis
- RJ
  - using EZJIT
- SJ
  - using EZJIT

TP2P Calibration Steps

- Insertion loss calibration
  - VNA
- Initial optimal preset selection
  - using SEASIM
- Test channel loss selection
  - using SEASIM
- DM-SI calibration for selected channel
- CM-SI calibration for selected channel
- Final optimal preset selection
  - using SEASIM
- Compliance eye calibration
  - using SEASIM

PCI Express 5.0 32 GT/s – M8040A

BASE SPECIFICATION – TP3 CALIBRATION SETUP



TP3 Calibration Steps

- Launch voltage, preshoot and de-emphasis
- RJ
  - using EZJIT
- SJ
  - using EZJIT

Connection

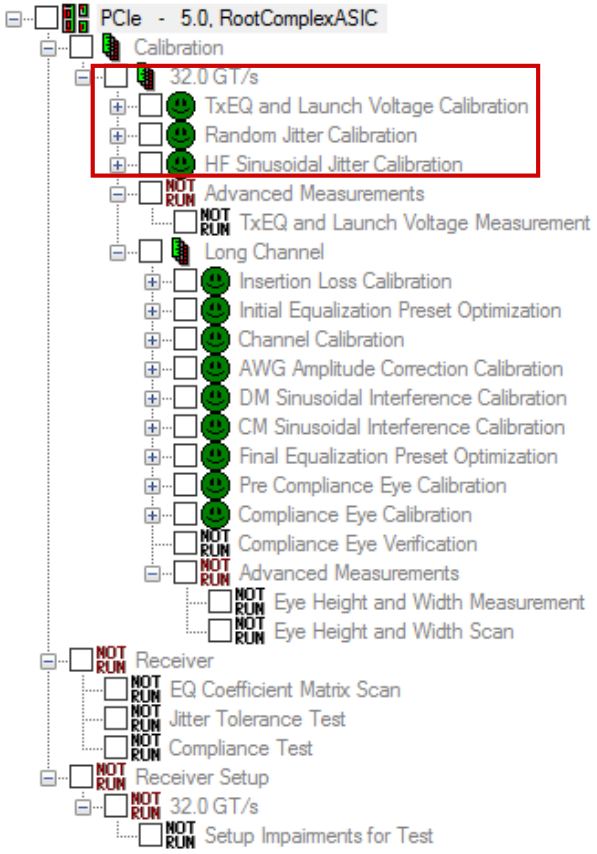
- BERT Data Output ➔ Power Couplers ➔ DC Blocks ➔ high quality matched pair 2.4 mm cables ➔ scope
  Comment: The actual cabling after the DC blocks and the scope is dependent on the connectors used for the ISI traces

Scope BW

- At least 50 GHz of scope BW are required

PCI Express 5.0 – Base Specification

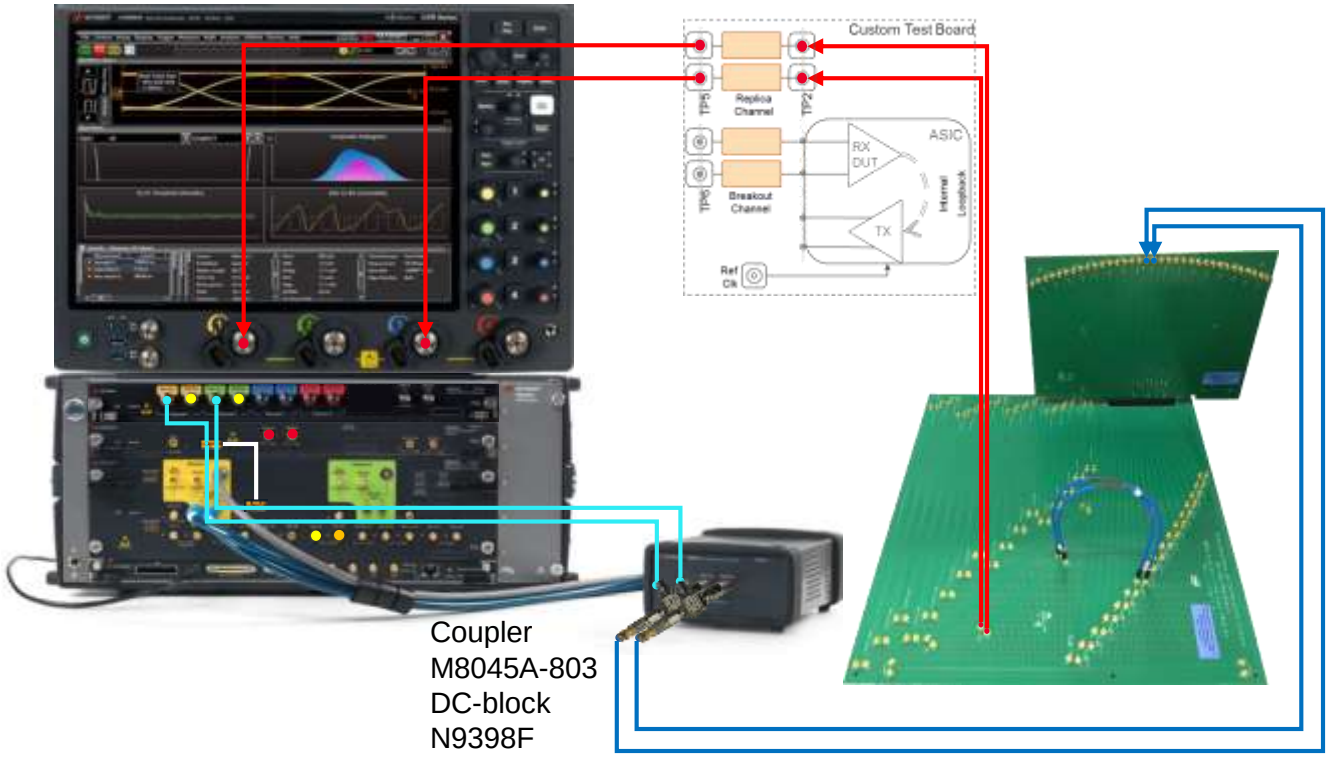
CALIBRATION 32 GT/s RX STRESS SIGNAL – TP3 CALIBRATION SETTINGS



Parameter	Min	Max	Unit	Oscilloscope Settings	
				Q-Series / Z-Series	UXR
Launch Amplitude 800 mV	796	804	mV_{pp}	BW: 50 GHz M8040A Sampling rate: 160 GSa/s Memory depth: 4.096 kpts Averaging: 128	BW: 50 GHz M8040A Sampling rate: 256 GSa/s Memory depth: 6.554 kpts Averaging: 256
Launch Amplitude 720 mV	716	724	mV_{pp}		
Preshoot and de-emphasis for P0 through P9 P5 and P6 are the only presets used for the calibration of the stress signal				BW: 50 GHz M8040A Sampling rate: 160 GSa/s Memory depth: 4.096 kpts Averaging: 128	BW: 50 GHz M8040A Sampling rate: 256 GSa/s Memory depth: 6.554 kpts Averaging: 256
RJ	0.5	0.6	ps_{rms}	BW: 33 GHz Sampling rate: 160 GSa/s Memory depth: 10 Mpts Averaging: off	BW: 33 GHz Sampling rate: 256 GSa/s Memory depth: 16 Mpts Averaging: off
SJ @ 100 MHz 1 ps	0.8	1.0	ps_{pp}	BW: 33 GHz Sampling rate: 160 GSa/s Memory depth: 10 Mpts Averaging: off	BW: 33 GHz Sampling rate: 256 GSa/s Memory depth: 16 Mpts Averaging: off
SJ @ 100 MHz 5 ps	5.0	5.5	ps_{pp}		

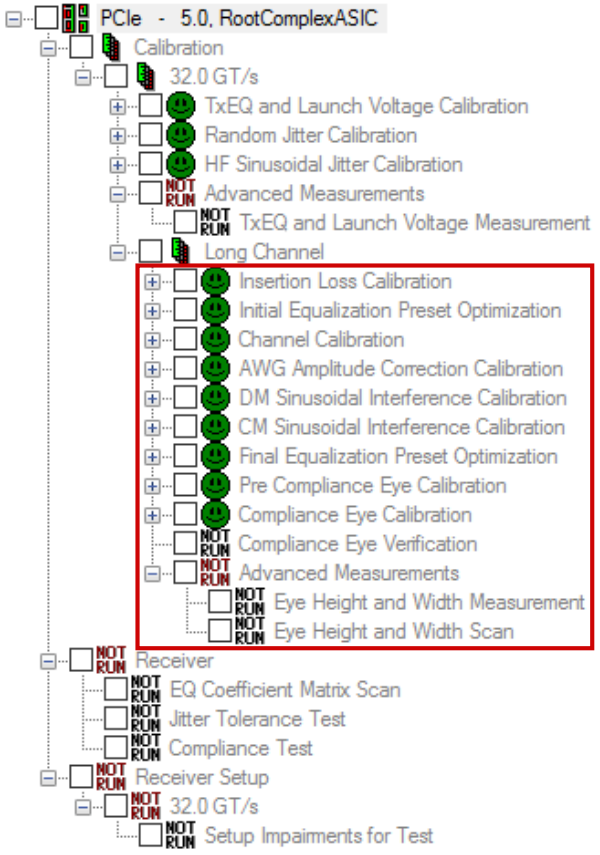
PCI Express 5.0 32 GT/s – M8040A

BASE SPECIFICATION TP2P CALIBRATION SETUP



PCI Express 5.0 – Base Specification

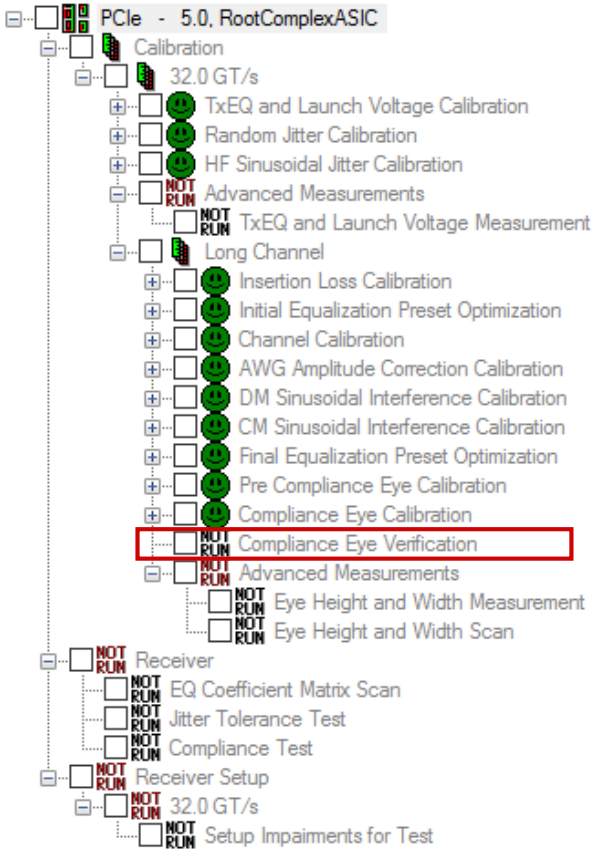
CALIBRATION 32 GT/s RX STRESS SIGNAL – TP2P CALIBRATION SETTINGS



Parameter	Min	Max	Unit	Oscilloscope Settings	
				X-Series / Q-Series V-Series / Z-Series	UXR
Insertion Loss @ 16 GHz	-37	-34	dB	VNA measurements; root and end point reference package models need to be taken into account	
DM-SI @ 2.1 GHz 25 mV	28	30	mV_{pp}	BW: 5 GHz Sampling rate: 160 GSa/s Memory depth: 2 Mpts Averaging: off Reference package model embedding required	BW: 5 GHz Sampling rate: ? GSa/s Memory depth: ? Mpts Averaging: off Reference package model embedding required
DM-SI @ 2.1 GHz 14 mV	8	10	mV_{pp}		
CM-SI @ 120 MHz	148	150	mV_{pp}	BW: 5 GHz Sampling rate: 160 GSa/s Memory depth: 2 Mpts Averaging: off Reference package model embedding required	BW: 5 GHz Sampling rate: ? GSa/s Memory depth: ? kpts Averaging: off Reference package model embedding required
TxEQ Preset selection	Largest eye height * eye width		mVps	BW: 33 GHz Sampling rate: 160 GSa/s Memory depth: 2.05 kpts Averaging: 1024 Reference package model embedding required	BW: 33 GHz Sampling rate: 256 GSa/s Memory depth: 3.278 kpts Averaging: 1024 Reference package model embedding required
$V_{RX-EH-8G}$ Eye Height	AIC & System: 13.5 to 15.5		mV	BW: 33 GHz Sampling rate: 160 GSa/s Memory depth: 2.05 kpts Averaging: 1024 Reference package model embedding required	BW: 33 GHz Sampling rate: 256 GSa/s Memory depth: 3.278 kpts Averaging: 1024 Reference package model embedding required
$T_{RX-EW-8G}$ Eye Width	AIC & System: 18.25 to 19.25		ps		

PCI Express 5.0 – Base Specification

CALIBRATION 32 GT/s RX STRESS SIGNAL – COMPLIANCE EYE VERIFICATION

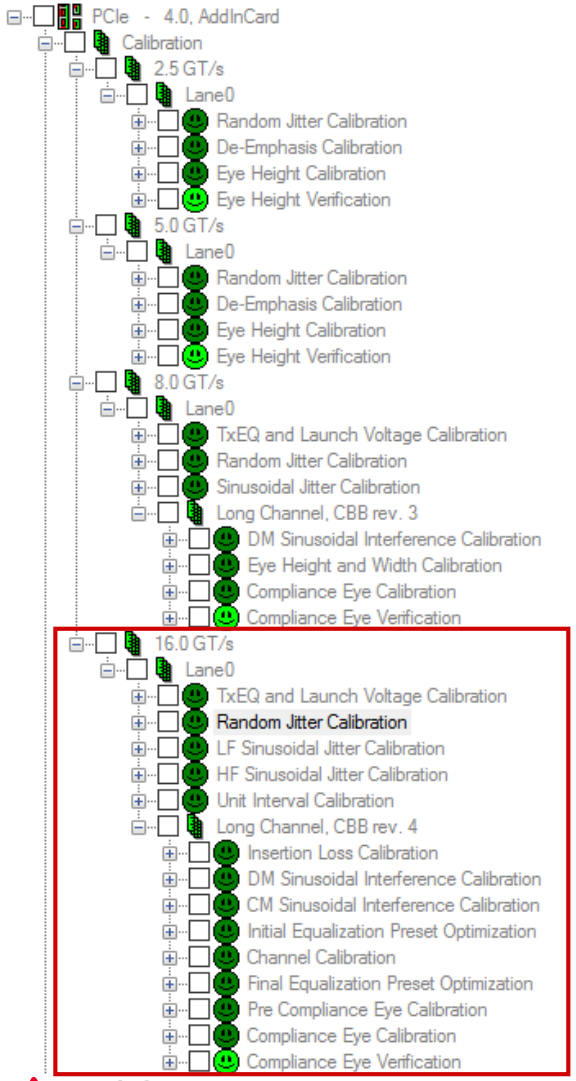


Compliance Eye Verification

- Calibration at TP2P
- Checks if stress impairment set of current calibration leads to EH / EW with target tolerance
- EH / EW Target
  - 13.5 mV ≤ EH ≤ 15.5 mV
  - 8.88 ps ≤ EW ≤ 9.88 ps
- SEASIM is used to measure EH and EW based on waveform captures
- RX reference package model is embedded on the scope

PCI Express 4.0 – PHY Test Specification

CALIBRATION STEPS 16 GT/s RX STRESS SIGNAL



TP3 Calibration Steps

- Launch voltage, preshoot and de-emphasis
- RJ
  - using SIGTEST
- SJ
  - using SIGTEST
- Unit interval measurement
- UI is provided to SIGTEST for TP2P waveform post processing

TP2P Calibration Steps

- Insertion loss calibration
  - VNA or SEASIM
- DM-SI calibration
  - @ 28 dB channel loss
- CM-SI calibration
  - @ 28 dB channel loss
- Initial optimal preset selection
  - using SIGTEST
- Test channel loss selection
  - using SIGTEST
- Final optimal preset selection
  - using SIGTEST
- Compliance eye calibration
  - using SIGTEST

PCI Express 4.0 16 GT/s – M8020A

PHY TEST SPECIFICATION – TP3 CALIBRATION SETUP

TP3 Calibration Steps

- Launch voltage, preshoot and de-emphasis
- RJ
  - using SIGTEST
- SJ
  - using SIGTEST
- Unit interval measurement
- UI is provided to SIGTEST for TP2P waveform post processing

Connection

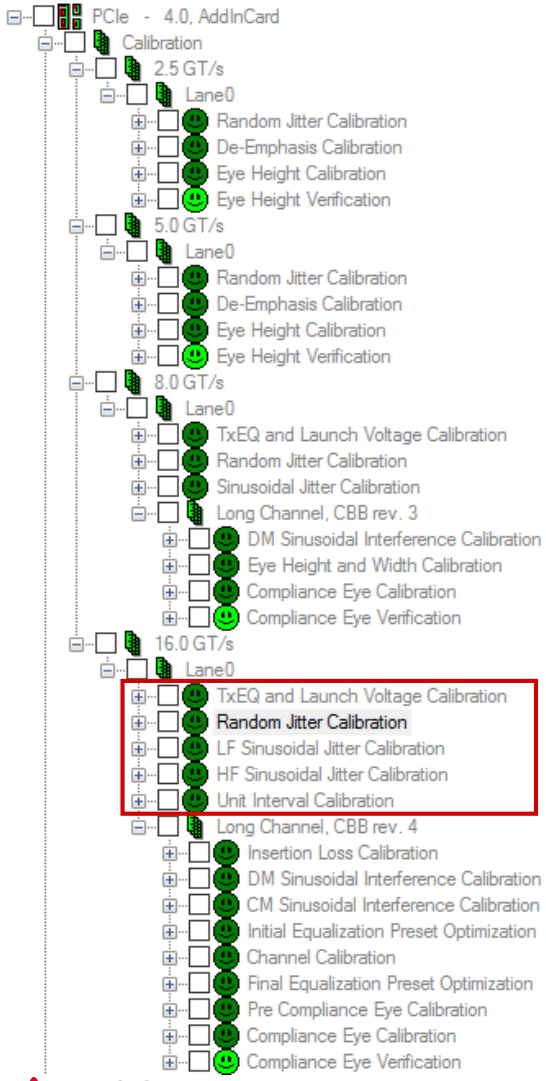
- BERT Data Output ➔ DC Blocks ➔ high quality matched pair 2.92 mm cables ➔ scope
- The short 2.92 mm to SMP cables are considered part of the channel TP3 ➔ TP2P

Scope BW

- At least 25 GHz of scope BW are required

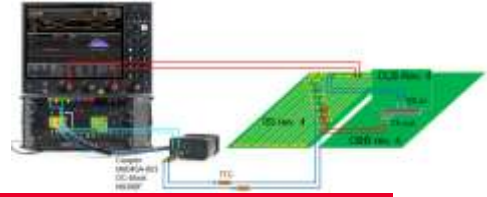
PCI Express 4.0 – PHY Test Specification

CALIBRATION 16 GT/s RX STRESS SIGNAL – TP3 CALIBRATION SETTINGS

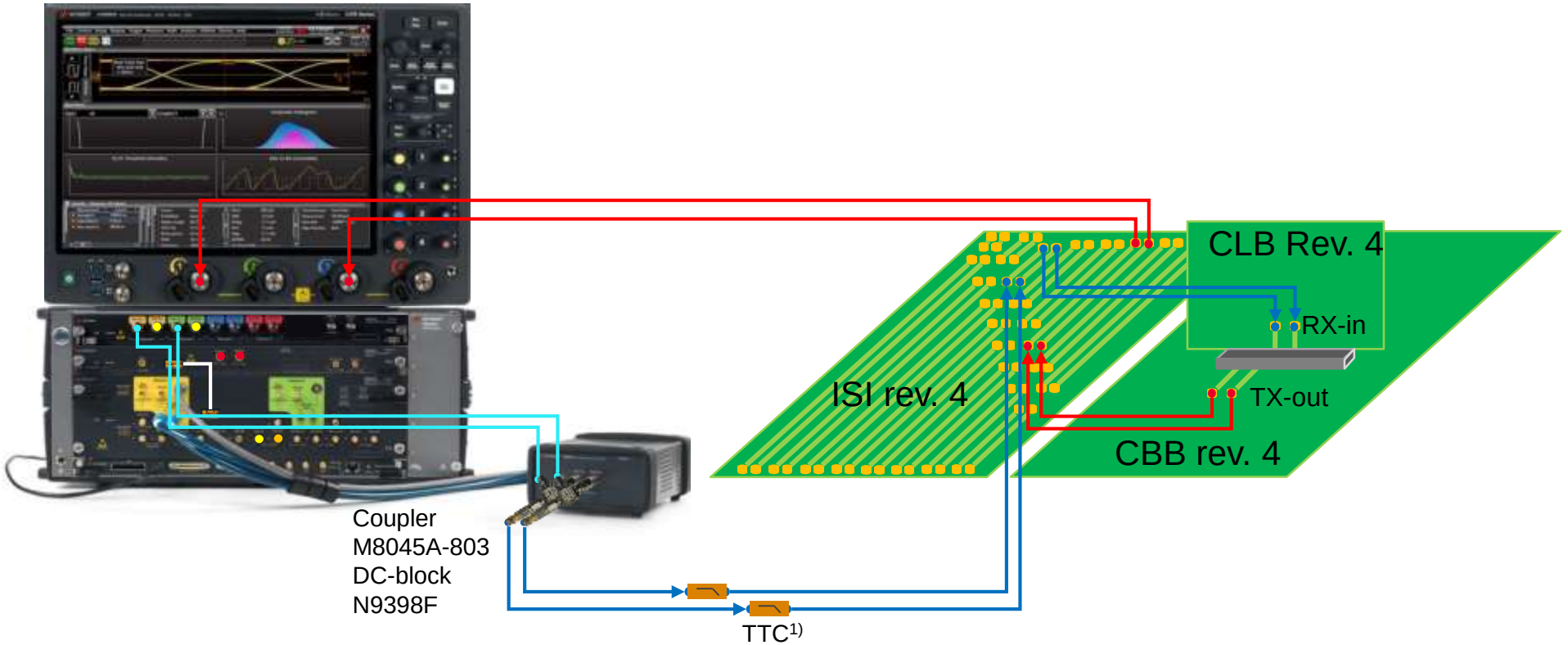


Parameter	Min	Max	Unit	SigTest		Oscilloscope Settings	
				Technology	Template	X-Series / Q-Series V-Series / Z-Series	UXR
Launch Amplitude 800 mV	796	804	mV_{pp}	N/A	N/A	BW: 25 GHz M8020A 50 GHz M8040A w/o TTC Sampling rate: 80 / 160 GSa/s Memory depth: 2048 / 4096 pts Averaging: 128 Low pass filter 30 GHz	BW: 25 GHz M8020A 50 GHz M8040A w/o TTC Sampling rate: 128 GSa/s Memory depth: 3277 pts Averaging: 256 Low pass filter 30 GHz
Launch Amplitude 720 mV	716	724	mV_{pp}				
Preshoot and de-emphasis for P0 through P9 P5 and P6 are the only presets used for the calibration of the stress signal				N/A	N/A	BW: 25 GHz M8020A 50 GHz M8040A w/o TTC Sampling rate: 80 /160 GSa/s Memory depth: 2048 / 4096 pts Averaging: 128 Low pass filter 30 GHz	BW: 25 GHz M8020A 50 GHz M8040A w/o TTC Sampling rate: 128 GSa/s Memory depth: 3277 pts Averaging: 256 Low pass filter 30 GHz
RJ	1.0	1.1	ps_{rms}	PCIE_4_0_RX_CAL	PCIE_4_16GB_CEM_Rj_Sj_CAL	BW: 25 GHz Sampling rate: 80 GSa/s Memory depth: 10 Mpts Averaging: off	BW: 25 GHz Sampling rate: 64 GSa/s Memory depth: 8 Mpts Averaging: off
SJ @ 100 MHz 10 ps	9.5	10.0	ps_{pp}	PCIE_4_0_RX_CAL	PCIE_4_16GB_CEM_Rj_Sj_CAL	BW: 25 GHz Sampling rate: 80 GSa/s Memory depth: 10 Mpts Averaging: off	BW: 25 GHz Sampling rate: 64 GSa/s Memory depth: 8 Mpts Averaging: off
SJ @ 100 MHz 5 ps	5.0	5.5	ps_{pp}				

PCI Express 4.0 16 GT/s – M8040A



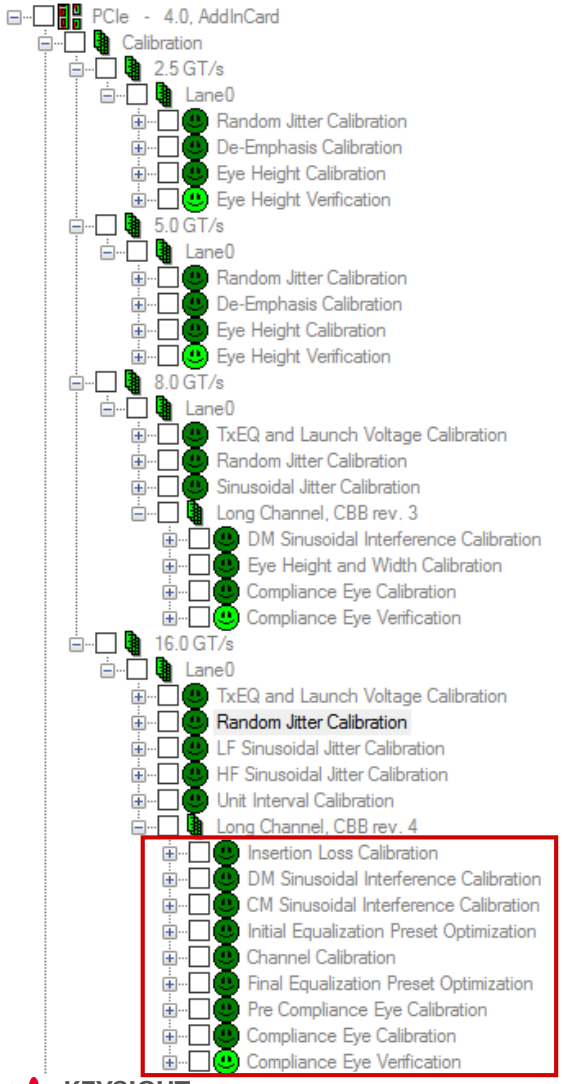
SYSTEM TP2P CALIBRATION SETUP



1)TTC not required if a scope BW is at least 50 GHz

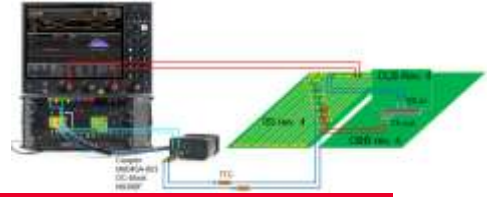
PCI Express 4.0 – PHY Test Specification

CALIBRATION 16 GT/s RX STRESS SIGNAL – TP2P CALIBRATION SETTINGS

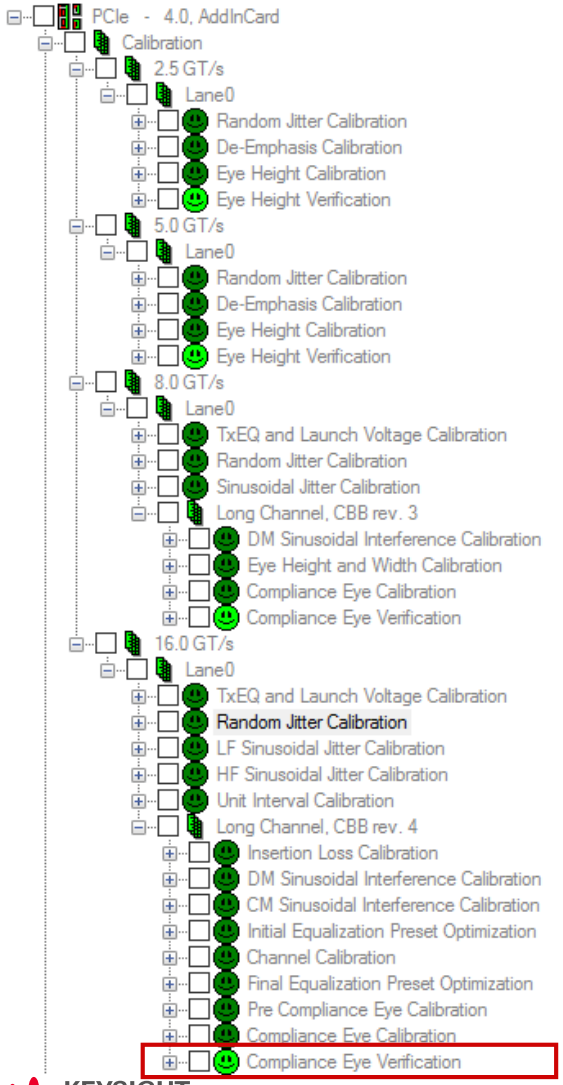


Parameter	Min	Max	Unit	SigTest		Oscilloscope Settings	
				Technology	Template	X-Series / Q-Series V-Series / Z-Series	UXR
Insertion Loss @ 8 GHz	-30	-27	dB	VNA measurement or step response method using SEASIM for PCI Express 4.0 16 GT/s the matched cable from the BERT PG outputs to TP3 is included in this measurement although it is compensated for in the launch amplitude, preshoot and de-emphasis calibration		BW: 25 GHz Sampling rate: 80 GSa/s Memory depth: 2.048 kpts Averaging: 1024 Reference package model embedding required	BW: 25 GHz Sampling rate: 128 GSa/s Memory depth: 3.278 kpts Averaging: 1024 Reference package model embedding required
DM-SI @ 2.1 GHz 25 mV	23	25	mV_{pp}	DM-SI amplitude = ACV_{rms} * 2 * sqrt(2)		BW: 25 GHz Sampling rate: 80 GSa/s Memory depth: 1 Mpts Averaging: 128 Reference package model embedding required	BW: 25 GHz Sampling rate: 64 GSa/s Memory depth: 800 kpts Averaging: 128 Reference package model embedding required
DM-SI @ 2.1 GHz 14 mV	12	14	mV_{pp}				
DM-SI @ 2.1 GHz 10 mV	8	10	mV_{pp}				
CM-SI @ 120 MHz	148	150	mV_{pp}	N/A	N/A	BW: 25 GHz Sampling rate: 80 GSa/s Memory depth: 1 Mpts Averaging: 128 Reference package model embedding required	BW: 25 GHz Sampling rate: 64 GSa/s Memory depth: 800 kpts Averaging: 128 Reference package model embedding required
TxEQ Preset selection between P5 & P6	Largest eye height * eye width		mVps	PCIE_4_0_RX_CAL	PCIe_4_16G_Rx_CAL_CTLE_xdB xdB...8 dB to 10 dB in ¼ dB steps	BW: 25 GHz Sampling rate: 80 GSa/s Memory depth: 10 Mpts Averaging: off Reference package model embedding required	BW: 25 GHz Sampling rate: 64 GSa/s Memory depth: 8 Mpts Averaging: off Reference package model embedding required
$V_{RX-EH-8G}$ Eye Height	AIC & System: 13.5 to 15.5		mV	PCIE_4_0_RX_CAL	PCIe_4_16G_Rx_CAL_CTLE_xdB xdB...8 dB to 10 dB in ¼ dB steps	BW: 25 GHz Sampling rate: 80 GSa/s Memory depth: 10 Mpts Averaging: off Reference package model embedding required	BW: 25 GHz Sampling rate: 64 GSa/s Memory depth: 8 Mpts Averaging: off Reference package model embedding required
$T_{RX-EW-8G}$ Eye Width	AIC & System: 18.25 to 19.25		ps				

PCI Express 4.0 – PHY Test Specification



CALIBRATION 16 GT/s RX STRESS SIGNAL – COMPLIANCE EYE VERIFICATION



Compliance Eye Verification

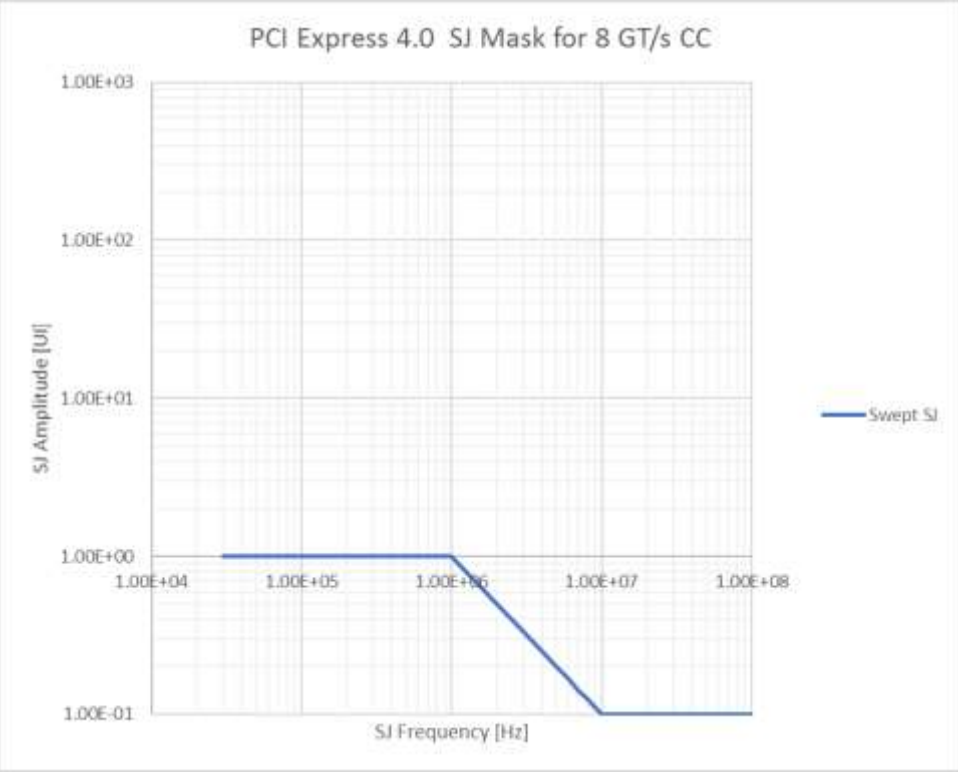
- Calibration at TP2P
- Checks if stress impairment set of current calibration leads to EH / EW with target tolerance
- EH / EW Target
  - 13.5 mV ≤ EH ≤ 15.5 mV
  - 18.25 ps ≤ EW ≤ 19.25 ps
- SIGTEST is used to measure EH and EW based on waveform captures
- RX reference package model is embedded on the scope

Agenda

PCI Express 4.0 – Base Specification

8 GT/s BASE SPECIFICATION – RX SJ MASK

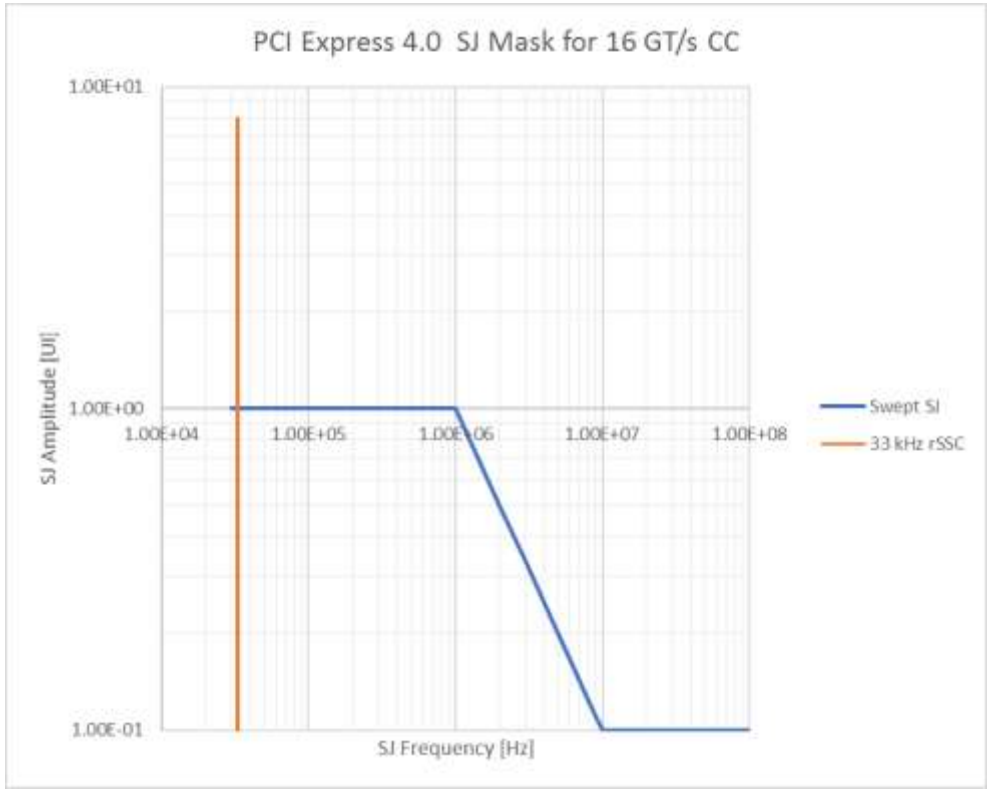
- No differences compared to PCI Express 3.1
- Different swept SJ jitter tolerance curves for CC and SRIS.
- Fixed 33 kHz SJ spur with amplitude of 25 ns for IR. BERT PG data rate needs to be 8 Gb/s -2500 ppm for IR.
- No fixed 33 kHz SJ spur or rSSC for CC

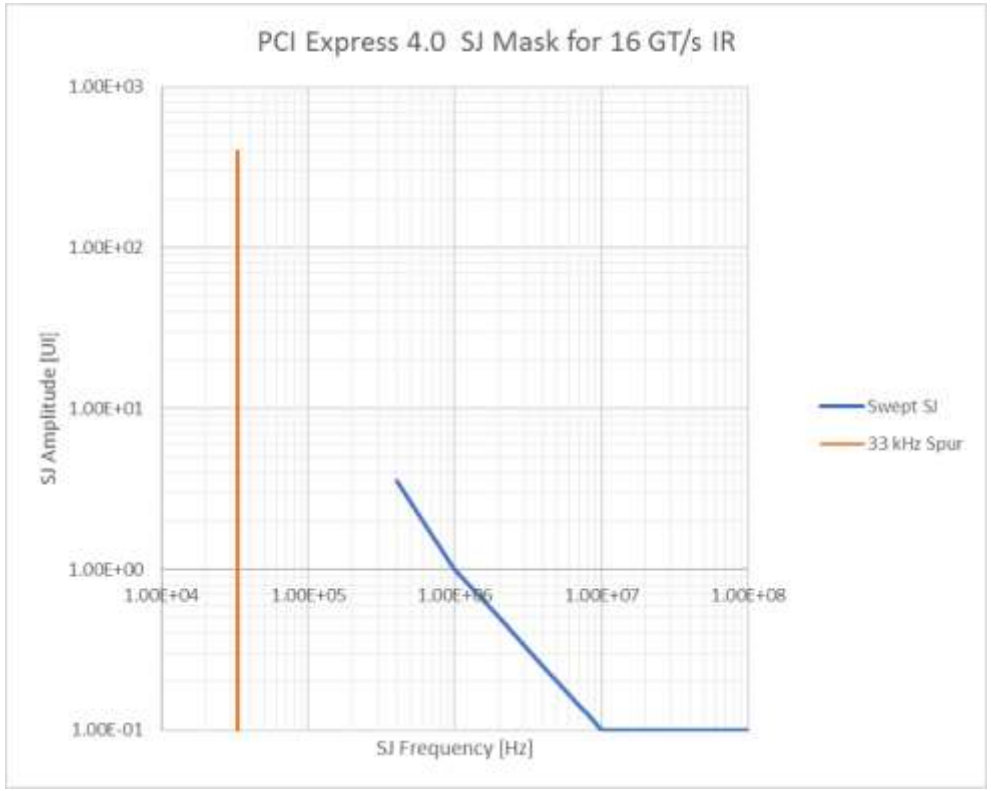


PCIe 4.0 RX Tests

16 GT/s BASE SPECIFICATION – RX SJ MASK

- Different jitter tolerance curves for CC and IR
- rSSC @ 33 kHz for CC only
- Constant 33 kHz SJ tone with 25ns in addition to jitter tolerance curve and 210 MHz SJ tone for IR only. BERT PG data rate needs to be 16 Gb/s -2500 ppm for IR.

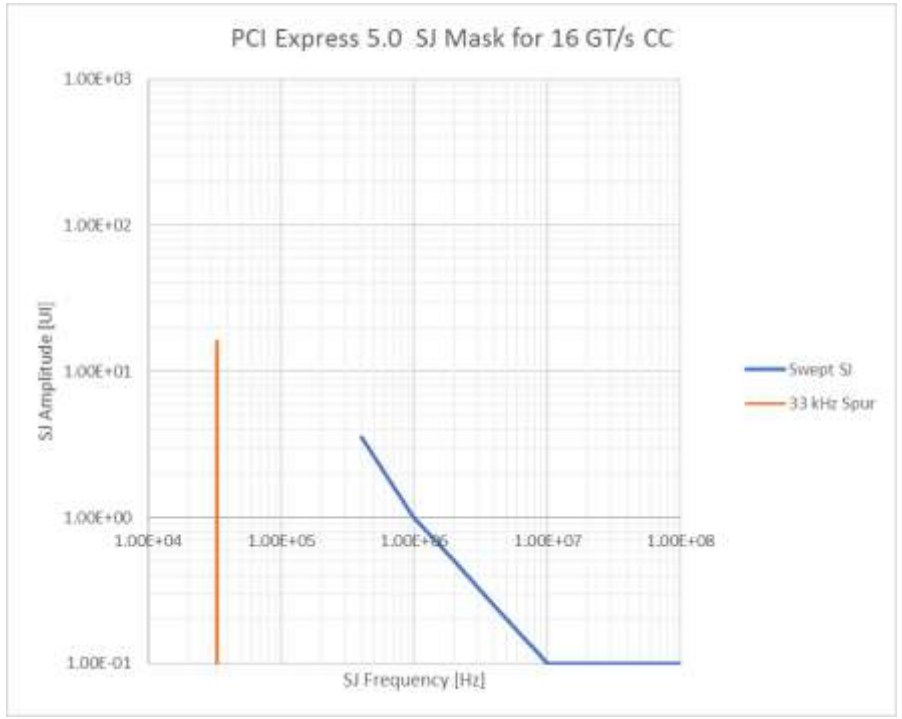


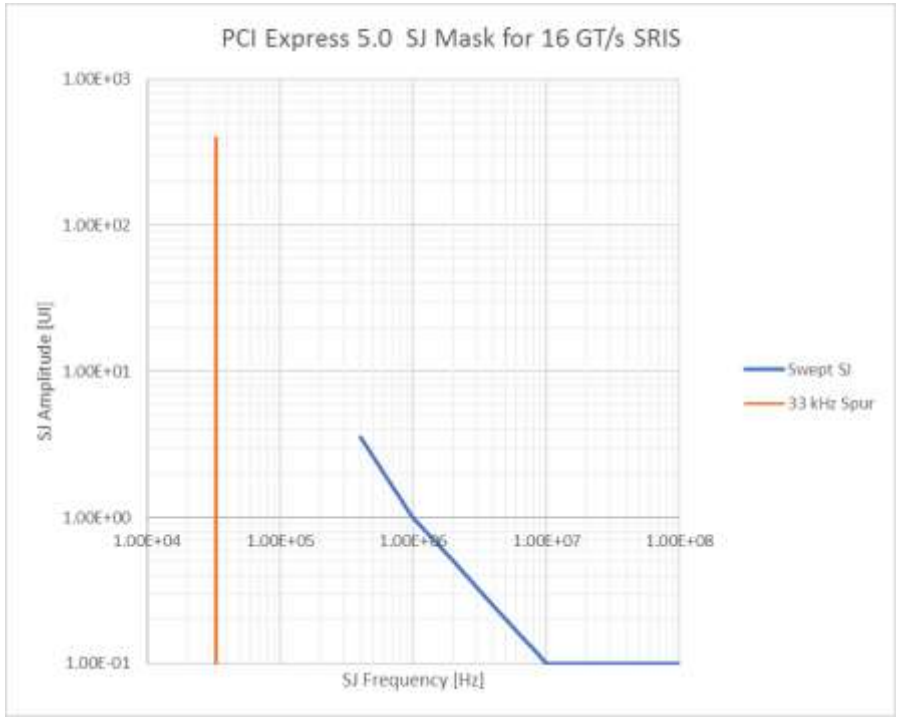


PCI Express 5.0 – Base Specification

16 GT/s – RX SJ MASK

- No longer different jitter tolerance curves for CC and SRIS. Only difference is in the fixed 33 kHz SJ spur which is in addition to the swept SJ jitter tolerance curve and 210 MHz SJ tone
- rSSC for CC substituted by fixed 33 kHz SJ spur similar to SRIS
- Fixed 33 kHz SJ spur with amplitude of 1 ns for CC and 25 ns for SRIS.
- In case of SRIS the BERT PG data rate needs to be 16 Gb/s -2500 ppm.

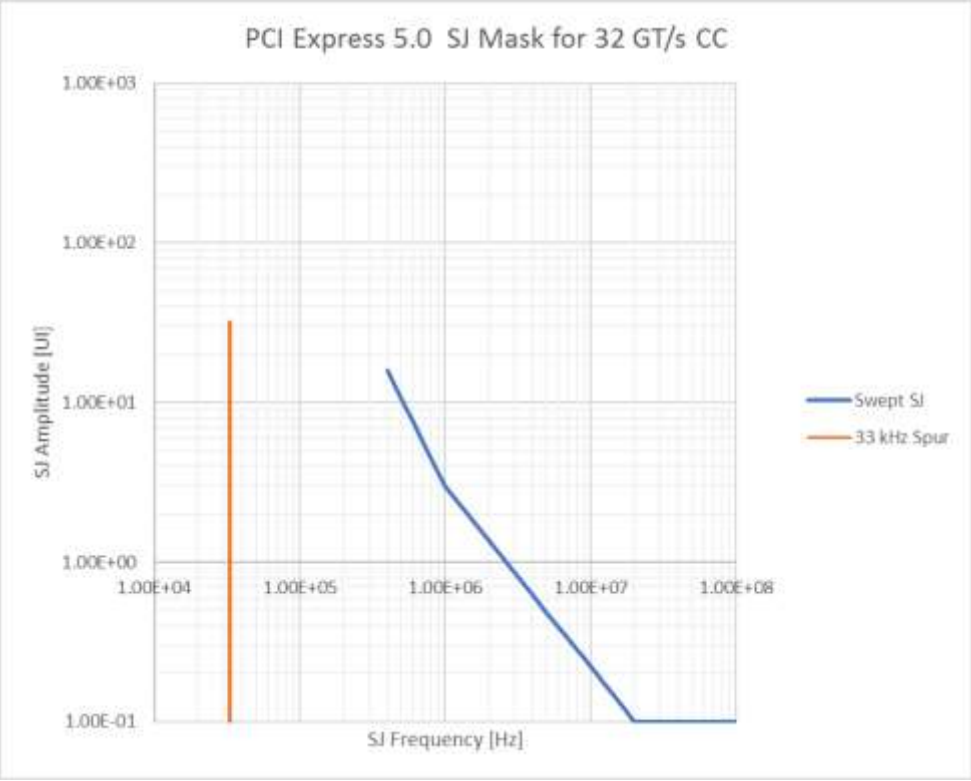


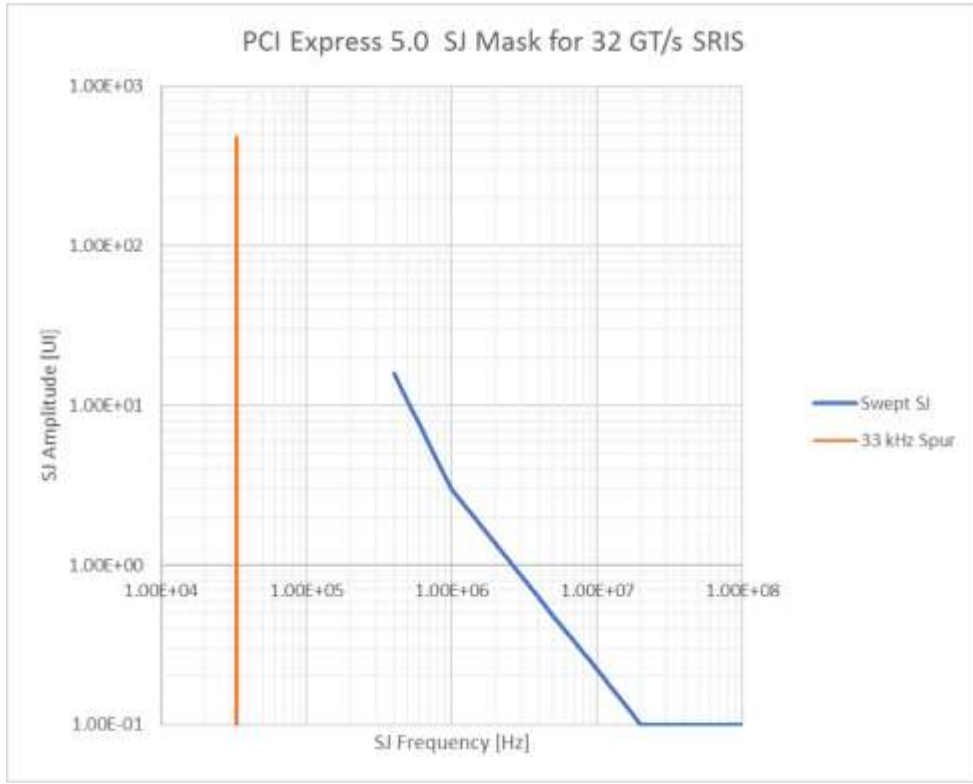


PCIe 5.0 RX Tests

32 GT/s BASE SPECIFICATION – RX SJ MASK

- Similar swept SJ jitter tolerance curves for CC and SRIS. Only difference is in the fixed 33 kHz SJ spur which is in addition to the swept SJ jitter tolerance curve and 210 MHz SJ tone
- Fixed 33 kHz SJ spur with amplitude of 1 ns for CC and 15 ns for SRIS.
- In case of SRIS BERT PG data rate needs to be 32 Gb/s -1500 ppm.





PCI Express 5.0 SJ Sources– M8040A & M8020A

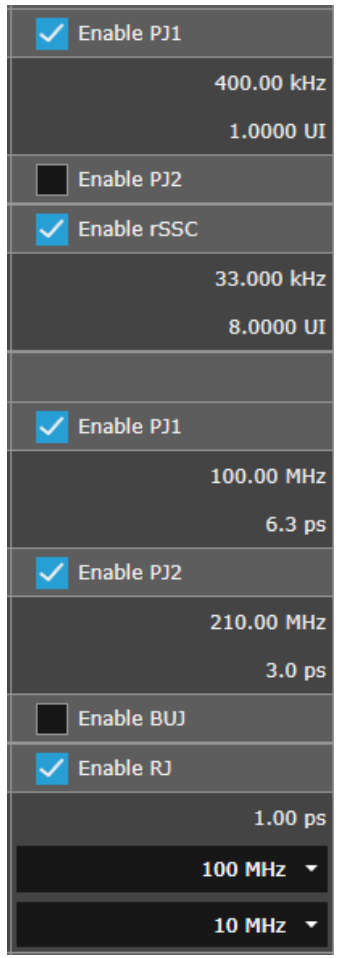
NEW SECOND TONE LF-PJ2

PCI Express Base Specification 5.0 replaced rSSC, which was used for common clock architecture to emulate the worst case effect of SSC on the receiver by, a 33 kHz SJ tone of 1ns which is applied in addition to the SJ mask and the fixed 210 MHz SJ tone, which is used to keep SJ mask fixed.

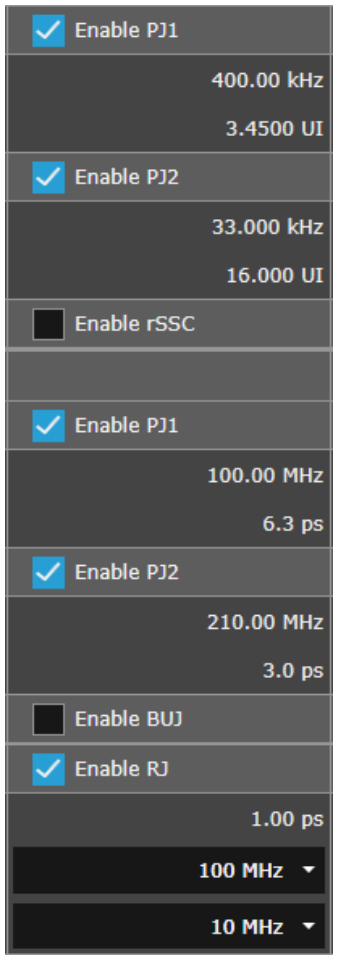
This mix of a SJ mask plus a 210 MHz fixed SJ tone plus a 33 kHz fixed SJ tone was not possible on the M8020A and M8040A until M8070B S6.5 release.

Starting with M8070B S6.5 release a second low frequency SJ tone, LF-PJ2, is available on all M8020A and M8040A systems equipped with jitter sources.

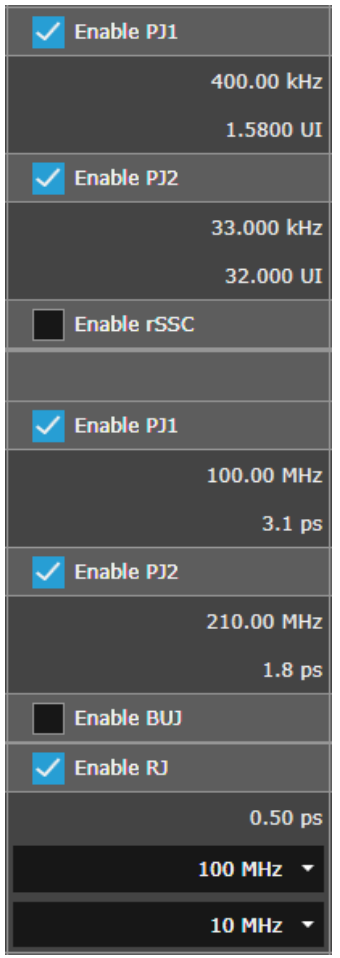
PCIe 4.0 16G:



PCIe 5.0 16G:



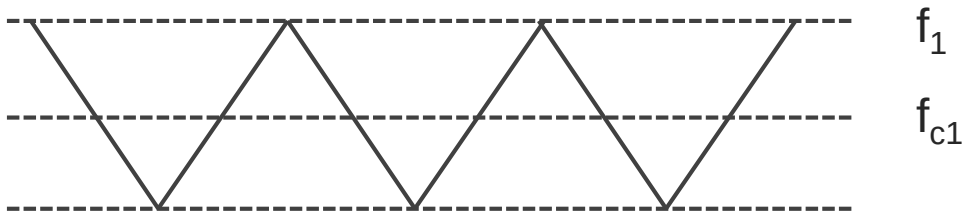
PCIe 5.0 32G:



PCIe 4.0 / 5.0 RX Tests

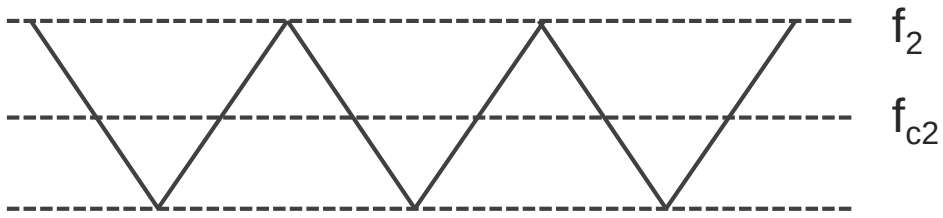
SRIS

BERT Pattern Generator



f_1 = BERT PG transfer rate +/- 300 ppm
f_{c1} = BERT PG center frequency averaged over multiple SSC cycles

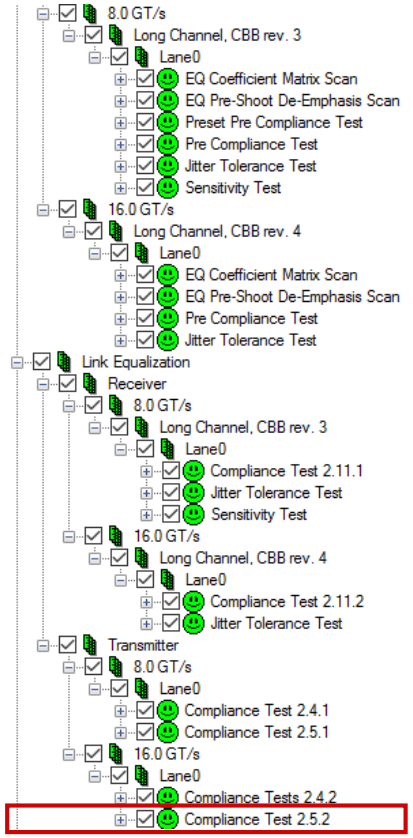
DUT TX



f_2 = DUT TX transfer rate +/- 300 ppm
f_{c2} = DUT TX center frequency averaged over multiple SSC cycles Maximum allowed difference between f_{c1} and f_{c2} is 600 ppm

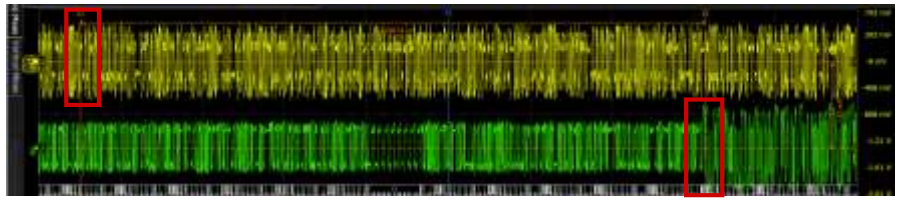
PCI Express 4.0 – PHY Test Specification

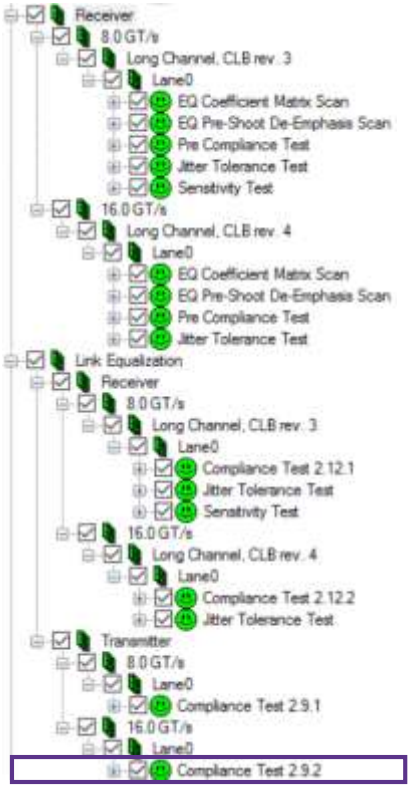
16 GT/s LINK EQUALIZATION PRESET & RESPONSE TIME TEST



Link Equalization Tests

- This test checks if the preset and coefficient requests during phase 2/3 are set physically and if the electrical and protocol response happens fast enough. This test applies to AICs and systems
- Test is performed for P0 through P9 as preset request and again as coefficient request
- DUT is trained into loopback through L0/Recovery with phase 2 and phase 3 active
- The compliance pattern is used
- Response Time Measurement
  - The BERT PG and DUT TX waveforms are captured around the change request
  - BERT PG waveform is decoded to determine the time of the initial preset request
  - DUT TX waveform is decoded to determine the time of the acknowledgment for the protocol response time
  - DUT TX waveform is analyzed for time of the waveform change for the electrical response time
- Preset Measurement
  - Waveforms are captured and analyzed by SIGTEST for de-emphasis and preshoot
- PHY Test Specification Number
  - 2.5.2 for add-in cards
  - 2.9.2 for systems





PCI Express 4.0 – PHY Test Specification

16 GT/s LINK EQUALIZATION PRESET & RESPONSE TIME TEST EXAMPLE RESULTS

Result	DUT Target Preset	Electrical response time [ns]	Protocol response time [ns]	Pre-Shoot [dB]	Min Spec PS [dB]	Max Spec PS [dB]	De-Emphasis [dB]	Min Spec DE [dB]	Max Spec DE [dB]	Comment
pass	P0	169.69	113.00	0.00	0.00	0.00	-5.65	-7.50	-4.50	DUT reported cursors: (0, 35, 12)
pass	P1	174.06	112.19	0.00	0.00	0.00	-3.24	-4.50	-2.50	DUT reported cursors: (0, 39, 8)
pass	P2	173.81	117.44	0.00	0.00	0.00	-4.07	-5.90	-2.90	DUT reported cursors: (0, 38, 9)
pass	P3	169.69	123.13	0.00	0.00	0.00	-2.30	-3.50	-1.50	DUT reported cursors: (0, 41, 6)
pass	P4	169.75	115.94	0.00	0.00	0.00	0.00	0.00	0.00	DUT reported cursors: (0, 47, 0)
pass	P5	165.69	112.75	1.76	0.90	2.90	0.00	0.00	0.00	DUT reported cursors: (5, 42, 0)
pass	P6	169.81	108.13	2.15	1.50	3.50	0.00	0.00	0.00	DUT reported cursors: (6, 41, 0)
pass	P7	165.69	107.25	3.37	2.50	4.50	-5.69	-7.50	-4.50	DUT reported cursors: (5, 33, 9)
pass	P8	173.56	111.06	3.18	2.50	4.50	-3.33	-4.50	-2.50	DUT reported cursors: (6, 35, 6)
pass	P9	171.81	107.19	3.07	2.50	4.50	0.00	0.00	0.00	DUT reported cursors: (8, 39, 0)
pass	P0' (0, 35, 12)	129.81	72.25	0.00	0.00	0.00	-5.48	-7.50	-4.50	
pass	P1' (0, 39, 8)	131.75	67.44	0.00	0.00	0.00	-3.06	-4.50	-2.50	
pass	P2' (0, 38, 9)	125.69	67.88	0.00	0.00	0.00	-3.61	-5.90	-2.90	
pass	P3' (0, 41, 6)	129.94	76.13	0.00	0.00	0.00	-2.37	-3.50	-1.50	
pass	P4' (0, 47, 0)	129.88	71.63	0.00	0.00	0.00	0.00	0.00	0.00	
pass	P5' (5, 42, 0)	125.81	68.00	1.81	0.90	2.90	0.00	0.00	0.00	
pass	P6' (6, 41, 0)	127.81	69.56	2.22	1.50	3.50	0.00	0.00	0.00	
pass	P7' (5, 33, 9)	131.75	73.75	3.22	2.50	4.50	-5.02	-7.50	-4.50	
pass	P8' (6, 35, 6)	129.69	73.38	2.93	2.50	4.50	-3.08	-4.50	-2.50	
pass	P9' (8, 39, 0)	127.88	69.00	3.16	2.50	4.50	0.00	0.00	0.00	
pass	Overall Result	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	

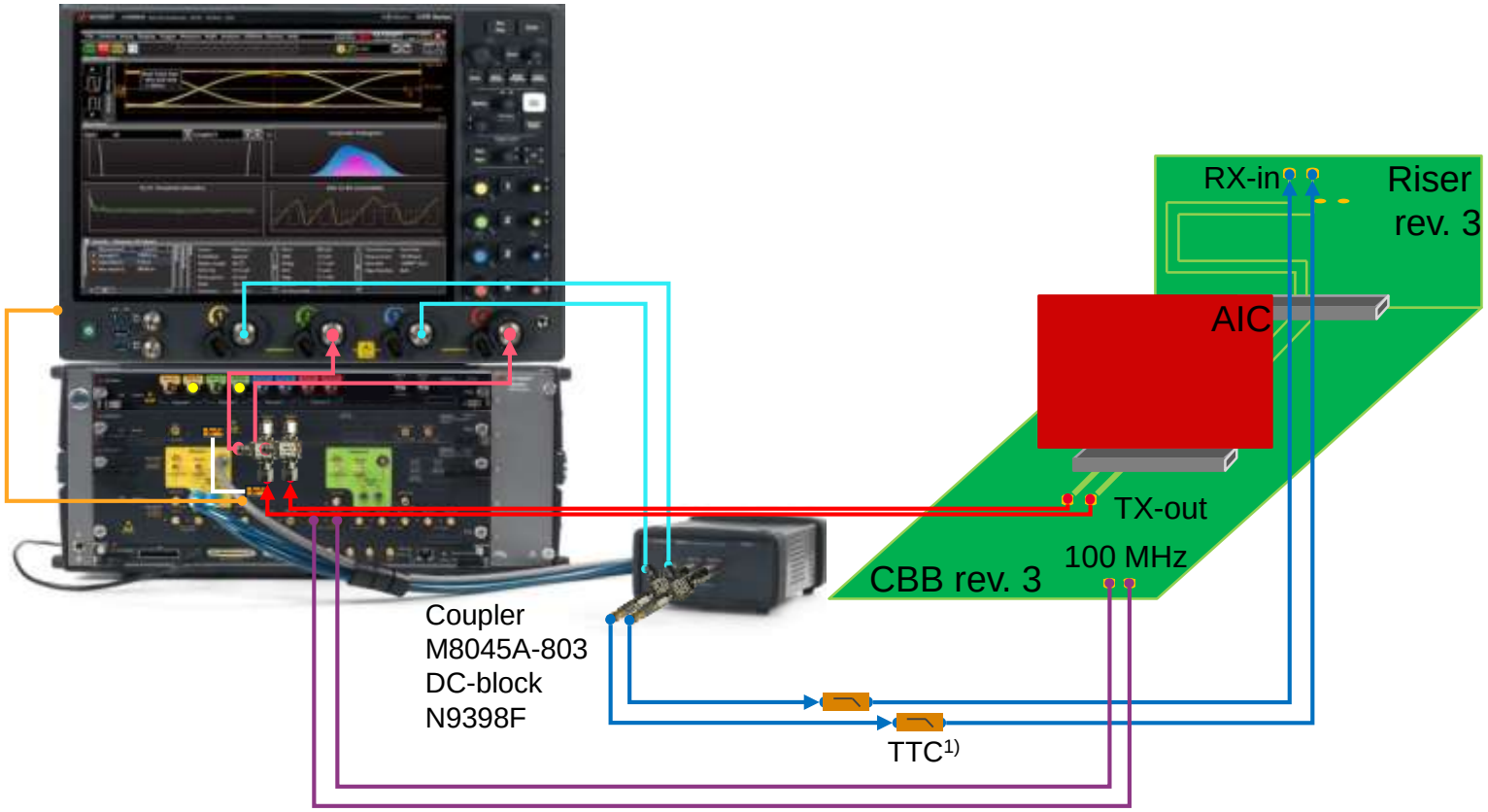
Add-In Card 2.5.2

System 2.9.2

Result	DUT Target Preset	Electrical response time [ns]	Protocol response time [ns]	Pre-Shoot [dB]	Min Spec PS [dB]	Max Spec PS [dB]	De-Emphasis [dB]	Min Spec DE [dB]	Max Spec DE [dB]	Comment
pass	P0	274.90	136.99	0.00	0.00	0.00	-5.92	-7.50	-4.50	DUT reported cursors: (0, 24, 8)
pass	P1	281.08	190.93	0.00	0.00	0.00	-3.89	-4.50	-2.50	DUT reported cursors: (0, 26, 6)
pass	P2	289.08	187.12	0.00	0.00	0.00	-4.70	-5.90	-2.90	DUT reported cursors: (0, 25, 7)
pass	P3	n/a	n/a	0.00	0.00	0.00	-2.46	-3.50	-1.50	DUT reported cursors: (0, 28, 6) No preset change response found. No preset change found on the waveform.
pass	P4	282.90	136.93	0.00	0.00	0.00	0.00	0.00	0.00	DUT reported cursors: (0, 32, 0)
pass	P5	287.14	132.93	1.62	0.90	2.90	0.00	0.00	0.00	DUT reported cursors: (3, 29, 0)
pass	P6	279.08	137.05	2.31	1.50	3.50	0.00	0.00	0.00	DUT reported cursors: (4, 28, 0)
pass	P7	279.14	128.99	2.96	2.50	4.50	-6.13	-7.50	-4.50	DUT reported cursors: (3, 22, 7)
pass	P8	270.96	130.74	3.32	2.50	4.50	-3.46	-4.50	-2.50	DUT reported cursors: (4, 24, 6)
pass	P9	267.08	130.80	3.62	2.50	4.50	0.00	0.00	0.00	DUT reported cursors: (6, 26, 0)
pass	P0' (0, 24, 8)	245.14	129.99	0.00	0.00	0.00	-5.95	-7.50	-4.50	
pass	P1' (0, 26, 6)	269.08	131.87	0.00	0.00	0.00	-3.88	-4.50	-2.50	
pass	P2' (0, 25, 7)	281.14	137.99	0.00	0.00	0.00	-4.70	-5.90	-2.90	
pass	P3' (0, 28, 6)	n/a	n/a	0.00	0.00	0.00	-2.46	-3.50	-1.50	Found response before request. No preset change found on the waveform.
pass	P4' (0, 32, 0)	280.96	130.93	0.00	0.00	0.00	0.00	0.00	0.00	
pass	P5' (3, 29, 0)	302.96	134.05	1.64	0.90	2.90	0.00	0.00	0.00	
pass	P6' (4, 28, 0)	298.27	131.99	2.31	1.50	3.50	0.00	0.00	0.00	
pass	P7' (3, 22, 7)	277.21	136.99	2.97	2.50	4.50	-6.12	-7.50	-4.50	
pass	P8' (4, 24, 6)	277.14	131.93	3.31	2.50	4.50	-3.45	-4.50	-2.50	
pass	P9' (6, 26, 0)	333.08	131.87	3.62	2.50	4.50	0.00	0.00	0.00	
pass	Overall Result	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	

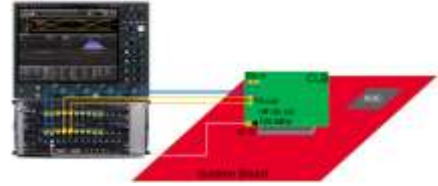
PCI Express 4.0 16 GT/s – M8040A

LinkEQ TX AIC SETUP – MOSTLY 1.85 mm / 2.4 mm

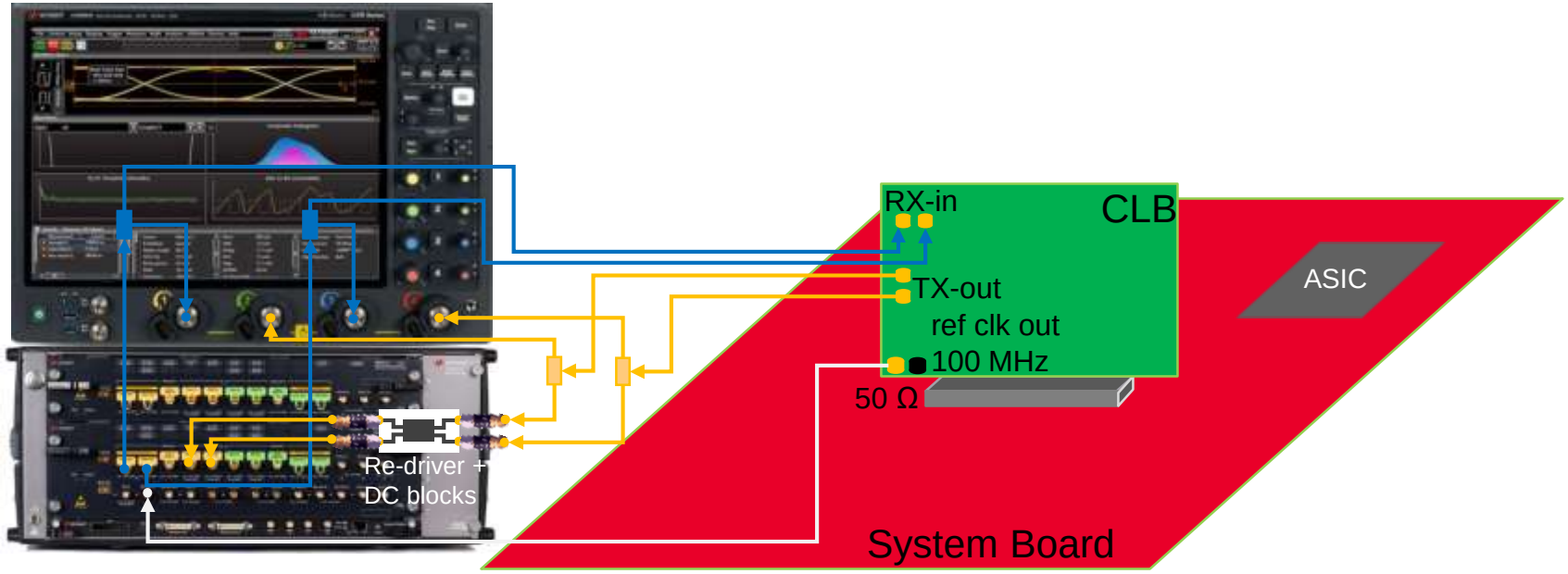


1)TTC not required if a scope BW is at least 50 GHz

PCI Express 4.0 16 GT/s – M8020A



LinkEQ TX TEST FOR SYSTEMS – LONG BACKCHANNEL

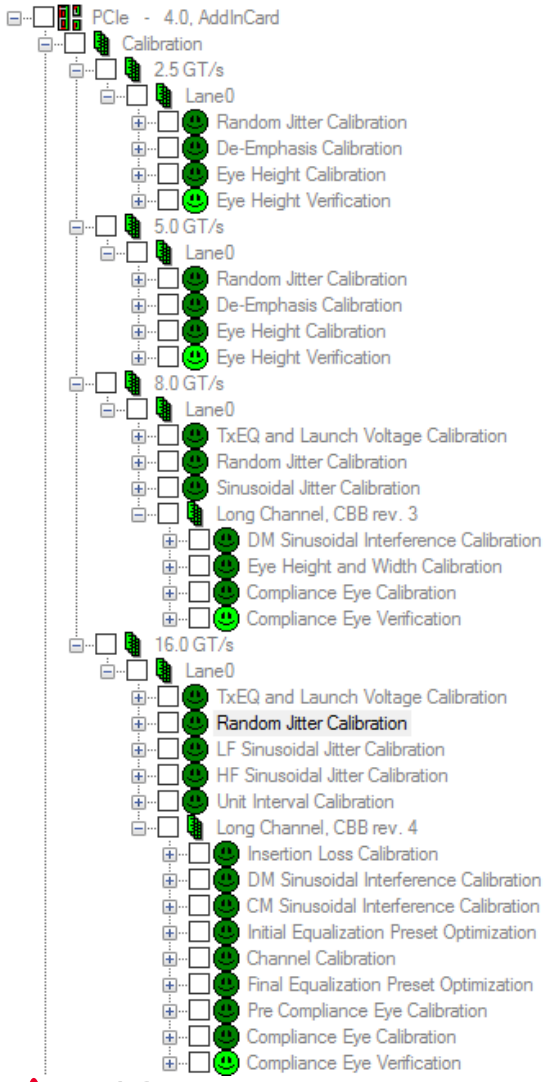


- 6 dB power dividers on PG data out to SUT RX path
- 10 dB to 14 dB pick-off z matched on SUT TX to ED data in path. Pick-off towards scope. Pick-off examples N1027A-2P2 or M8045A-803.
- Re-driver between ED data in and pick-off. Re-driver needs to be AC coupled on inputs as well as outputs
- Re-driver examples
  - Diodes PIEQX16904GL eval board
  - Texas Instruments DS280BR820EVM
- A re-driver is recommended with the M8040A test setup when testing a SUT for LinkEQ RX as well as LinkEQ TX

Agenda

- PCI Express Generic
- Challenge 1 – Which Test Setup Do You Need?
- Challenge 2 – PCI Express LTSSM
- Challenge 3 – PCI Express Stress Signal
- Challenge 4 – PCI Express RX and LinkEQ Tests
- Challenge 5 – Calibration / Test Complexity and Time
- Solution Overview
- Appendix

Calibration / Test Complexity and Time



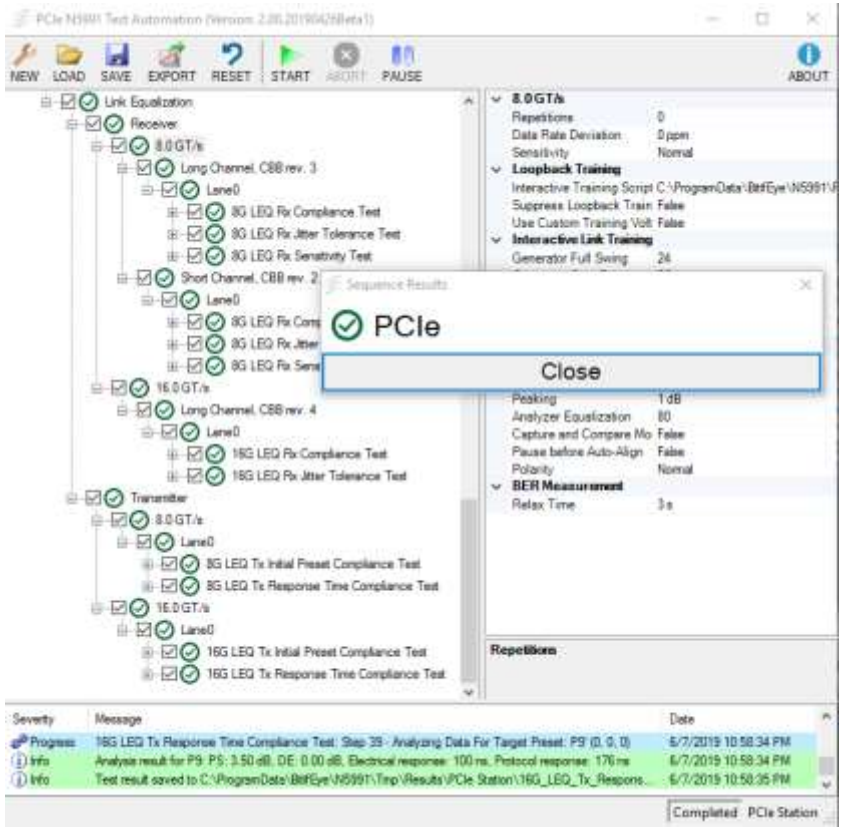
- The PCI Express RX stress signal calibration is
  - very complex, and
  - time intensive due to many steps requiring averaging of results of a lot of measurements with post processing
- LinkEQ transmitter testing required for compliance is tedious, especially the LinkEQ phase 2/3 preset, coefficient and response time test which requires 20 measurement steps
- RX characterization measurements like JTOL and TxEQ matrix scans are running a long time

➔ An RX and LinkEQ test automation plus a PC with 12 logical processors or more is highly recommended

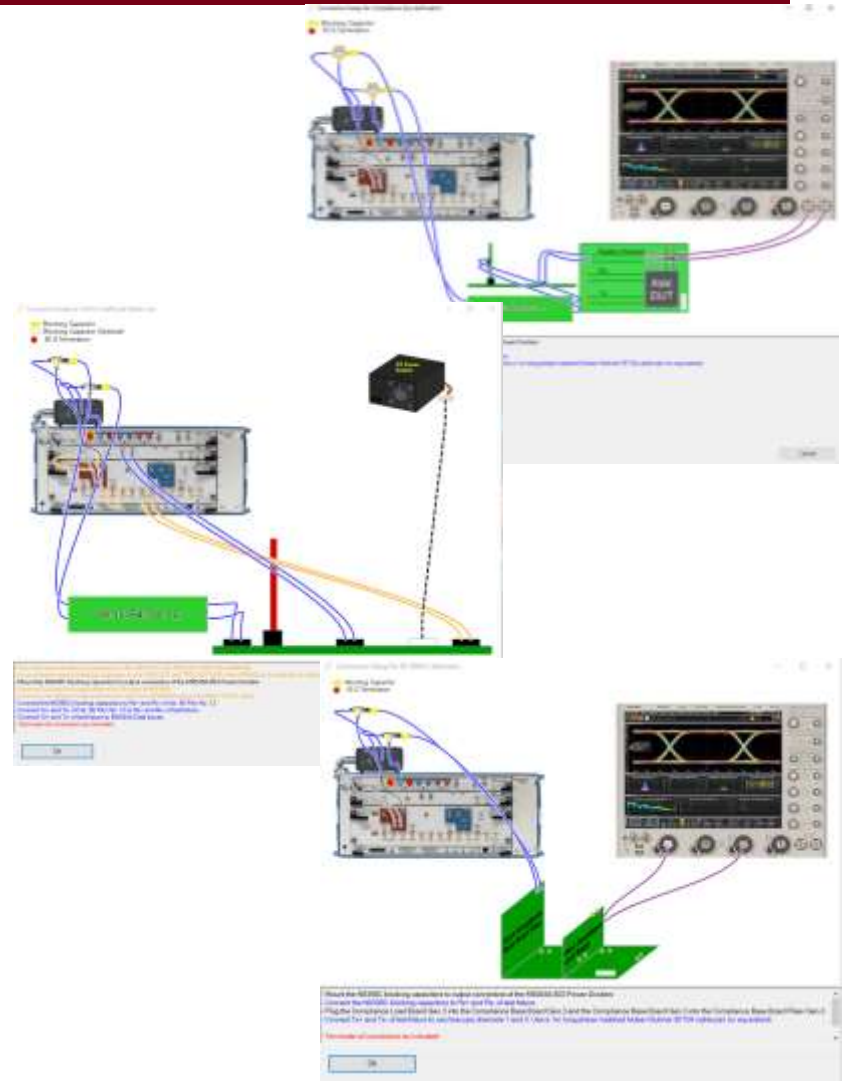
Result	DUT Target Preset	Electrical response time [ns]	Protocol response time [ns]	Pre-Shoot [dB]	Min Spec PS [dB]	Max Spec PS [dB]	De-Emphasis [dB]	Min Spec DE [dB]	Max Spec DE [dB]	Comment
pass	P0	274.90	136.99	0.00	0.00	0.00	-5.92	-7.50	-4.50	DUT reported cursors: (0, 24, 8)
pass	P1	281.08	190.93	0.00	0.00	0.00	-3.99	-4.50	-2.50	DUT reported cursors: (0, 26, 6)
pass	P2	289.08	137.12	0.00	0.00	0.00	-4.70	-5.90	-2.90	DUT reported cursors: (0, 25, 7)
pass	P3	n/a	n/a	0.00	0.00	0.00	-2.46	-3.50	-1.50	DUT reported cursors: (0, 28, 4) No preset change response found. No preset change found on the waveform.
pass	P4	282.90	136.93	0.00	0.00	0.00	0.00	0.00	0.00	DUT reported cursors: (0, 32, 0)
pass	P5	287.14	132.93	1.52	0.90	2.90	0.00	0.00	0.00	DUT reported cursors: (3, 29, 0)
pass	P6	279.08	137.05	2.31	1.50	3.50	0.00	0.00	0.00	DUT reported cursors: (4, 28, 0)
pass	P7	273.14	128.99	2.96	2.50	4.50	-6.13	-7.50	-4.50	DUT reported cursors: (3, 22, 7)
pass	P8	270.96	130.74	3.32	2.50	4.50	-3.46	-4.50	-2.50	DUT reported cursors: (4, 24, 4)
pass	P9	247.08	130.80	3.62	2.50	4.50	0.00	0.00	0.00	DUT reported cursors: (6, 26, 0)
pass	P0' (0, 24, 8)	245.14	129.99	0.00	0.00	0.00	-5.95	-7.50	-4.50	
pass	P1' (0, 26, 6)	269.08	131.87	0.00	0.00	0.00	-3.88	-4.50	-2.50	
pass	P2' (0, 25, 7)	281.14	137.98	0.00	0.00	0.00	-4.70	-5.90	-2.90	
pass	P3' (0, 28, 4)	n/a	n/a	0.00	0.00	0.00	-2.46	-3.50	-1.50	Found response before request. No preset change found on the waveform.
pass	P4' (0, 32, 0)	280.96	130.93	0.00	0.00	0.00	0.00	0.00	0.00	
pass	P5' (3, 29, 0)	302.96	134.05	1.54	0.90	2.90	0.00	0.00	0.00	
pass	P6' (4, 28, 0)	295.27	131.99	2.31	1.50	3.50	0.00	0.00	0.00	
pass	P7' (3, 22, 7)	277.21	136.99	2.97	2.50	4.50	-6.12	-7.50	-4.50	
pass	P8' (4, 24, 4)	277.14	131.93	3.31	2.50	4.50	-3.45	-4.50	-2.50	
pass	P9' (6, 26, 0)	333.08	131.87	3.62	2.50	4.50	0.00	0.00	0.00	
pass	Overall Result	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	

N5991PxxA

RX TEST AUTOMATION SOFTWARE

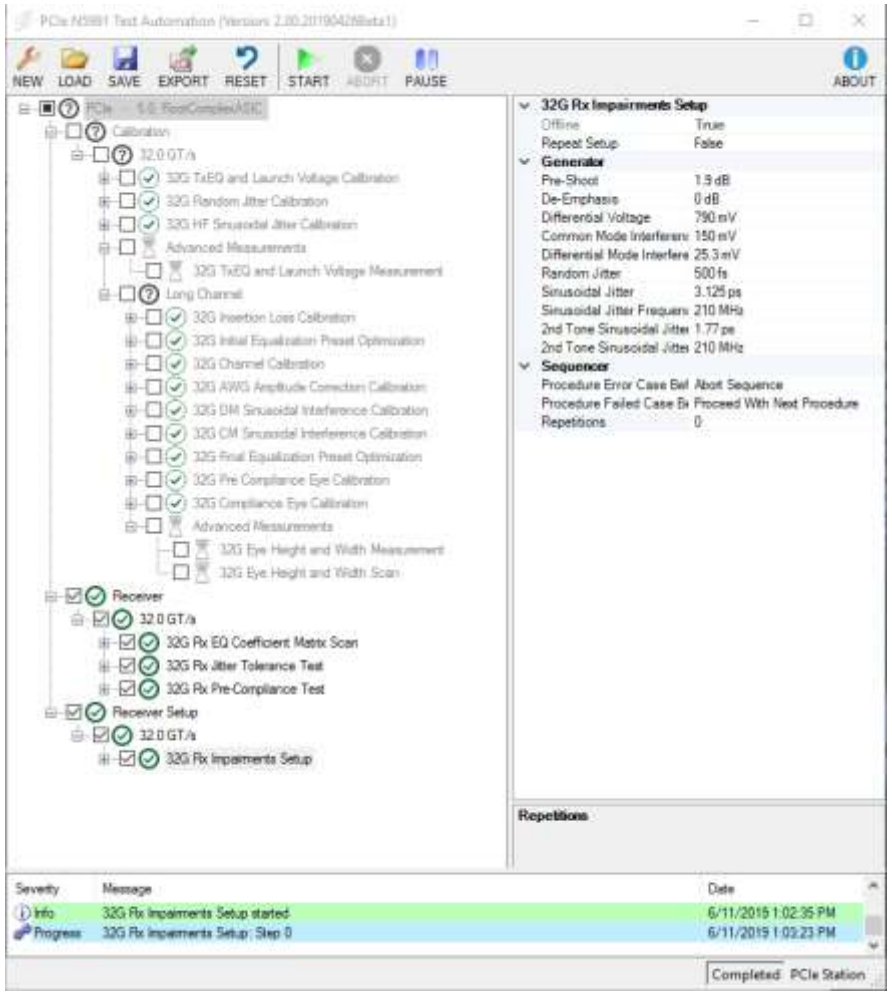


- Guided and automated stress signal calibration minimize user interaction and help to reduce errors
- LinkEQ tests require add-on option N5991PA3-ADD
- Test beyond compliance
  - TxEQ matrix scan for 32 GT/s, 16 GT/s and 8 GT/s
  - JTOL test for 32 GT/s, 16 GT/s and 8 GT/s
  - Sensitivity Test for 8 GT/s
- “Setup Impairment for Test” function sets the M8040A/M8020A system to user defined impairments. This function supports generator only systems as well as full RX test systems
- N5991PxxA offers test automation software products per PCI Express Specification type and revision
  - N5991PB5A – PCI Express 5.0 Base Spec
  - N5991PB4A – PCI Express 4.0 Base Spec
  - N5991PC4A – PCI Express 4.0 CEM / PHY Test Spec
  - N5991PU4A – PCI Express 4.0 U.2 Test Spec, currently 8 GT/s only
  - N5991PM4A – PCI Express 4.0 M.2 Test Spec, currently 8 GT/s only



N5991PB5A

BASE SPEC RX TEST & CHARACTERIZATION FOR PCI EXPRESS 5.0 32 GT/s



- Guided and automated stress signal calibration and test for PCI Express 5.0 32 GT/s*)
- “Setup Impairment for Test” function sets the M8040A/M8020A system to user defined impairments. This function supports generator only systems as well as full RX test systems
- Test beyond compliance
  - TxEQ matrix scan
  - JTOL test
- LinkEQ tests will be released in CY19H2 (requires add-on option N5991PA3-ADD)

*)16 GT/s, 8 GT/s, 5 GT/s and 2.5 GT/s support for M8040A will be added to the released N5991PB5A PCI Express 5.0 Base Specification RX Test product in CY19H2. 2.5 GT/s support using a M8040A based setups requires M8046A L4 HW.


L0_Cal_32GTps_CompEye

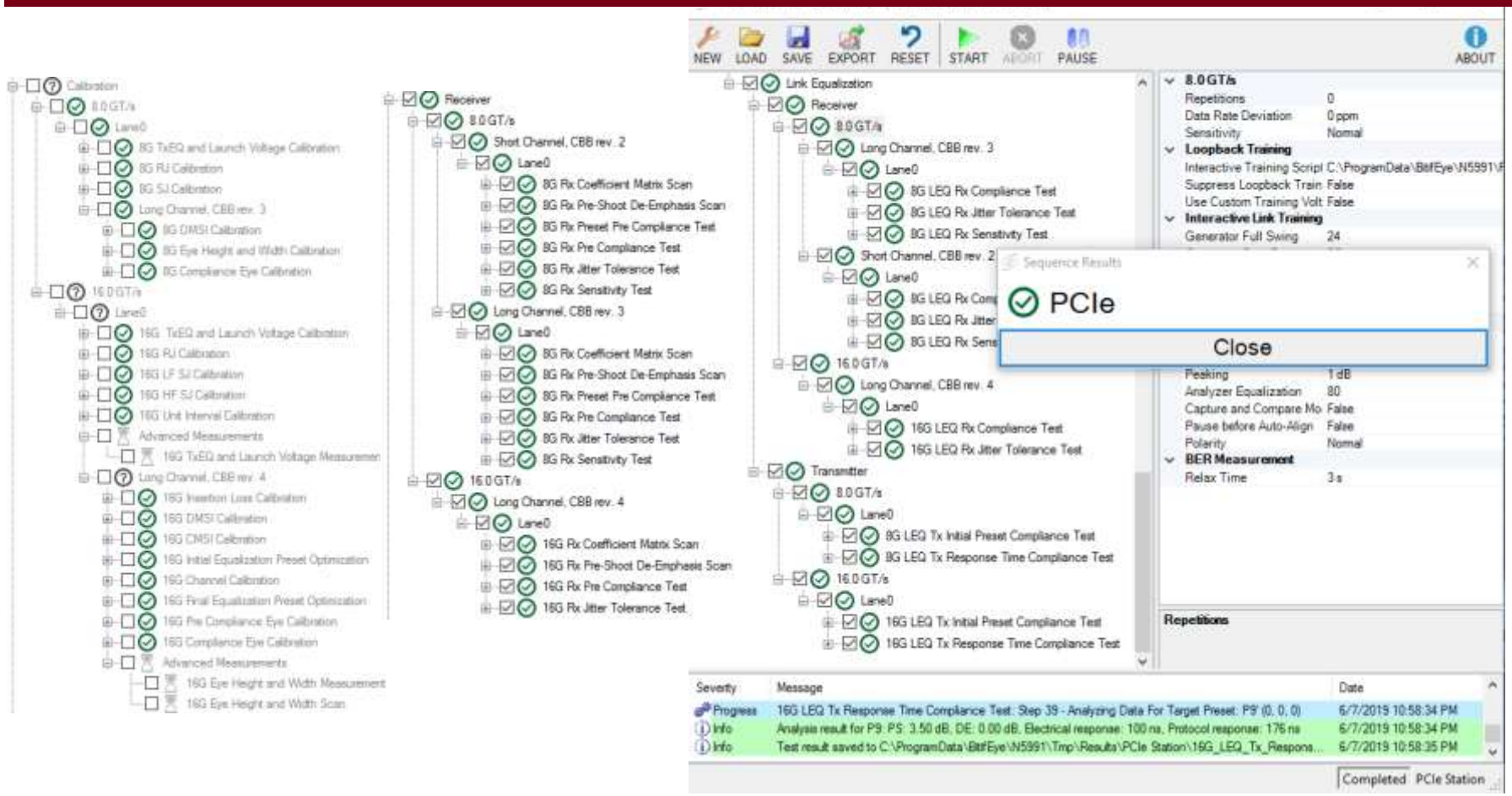
for PCIe 5.0 RootComplex ASIC

Oscilloscope	DSOZ334A, SN: MY57220108, FW rev.: 06.20.00701
BERT System	Keysight M8040A J-BERT, M8070B, SN: DE54C00245
Generator Channel Channel	M1.DataOut1
Offline	False
Scope Bandwidth	33 GHz
Number of Averages	21
Number of Waveform Averages	1024
Optimize CTLE	True
Trace Number	8
Total Channel Loss	-36.554 dB
Pre-Shoot	1.9 dB
De-Emphasis	0 dB
Max Number of Search Steps	7
Use nominal EH/EW results from Pre Comp Cal	True
Sinusoidal Jitter Frequency	100 MHz
Common Mode Interference	0 V
Random Jitter	500 fs
Gen5 Transfer Function File for Package Model on Scope	PCIe5RxPackageModel_RootComplex.tf4
Scope Connection for Calibration	RealEdge
Target Eye Height	15 mV
Target Eye Width	9.375 ps

DMST (mV)	BJ (ps)	VAIEF (mV)	Eye Height (mV)	Eye Width (ps)
25.3	6.90	790	14.46	9.35

N5991PC4A

TESTING LIKE AT A PCI-SIG COMPLIANCE WORKSHOP

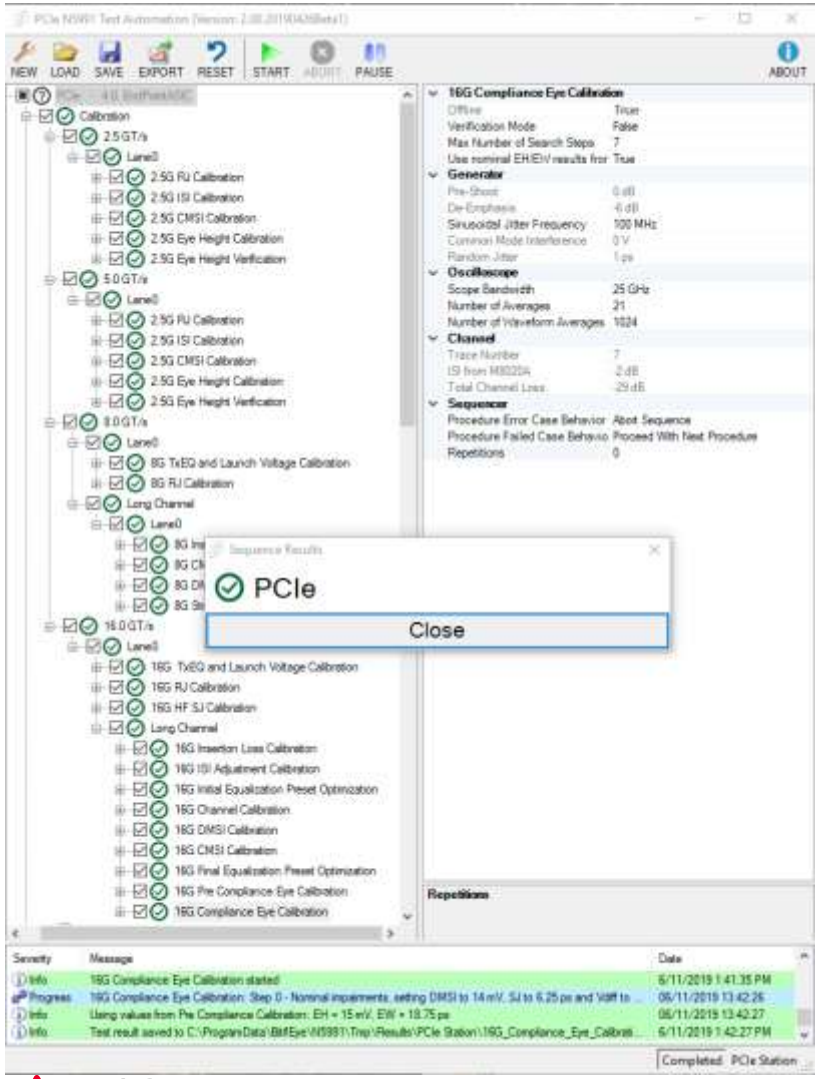


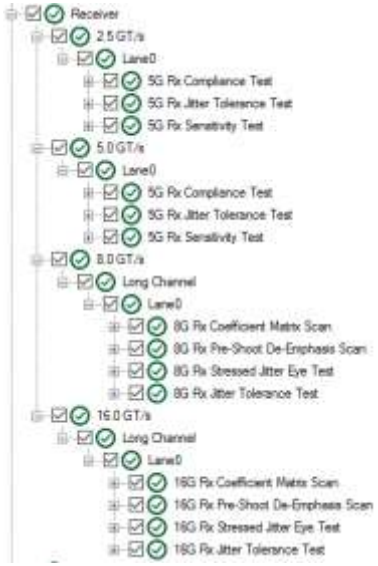
- Guided and automated stress signal calibration, RX test, RX LinkEQ and TX LinkEQ for PCI Express 8 GT/s and 16 GT/s*) according to the integrators list compliance testing at PCI-SIG Compliance Workshops for CEM formfactor
- LinkEQ tests require add-on option N5991PA3-ADD
- “Setup Impairment for Test” function sets the M8040A/M8020A system to user defined impairments. This function supports generator only systems as well as full RX test systems
- Test beyond compliance
  - TxEQ matrix scan for 16 GT/s and 8 GT/s
  - JTOL test for 16 GT/s and 8 GT/s
  - Sensitivity Test for 8 GT/s
- Supports M8040A as well as M8020A

*)5 GT/s and 2.5 GT/s stress signal calibration will be added to the released N5991PC4A PCI Express 4.0 CEM Specification RX Test product in CY20H1.

N5991PB4A

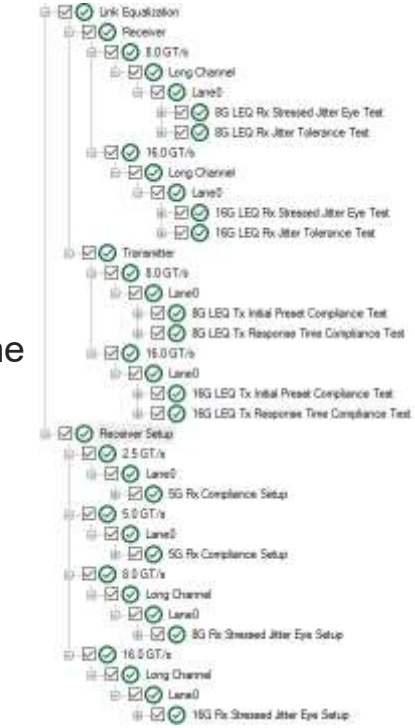
ALL TRANSFER RATES, CC/IR RX TESTING FOR PCI EXPRESS BASE SPEC 4.0





- Guided and automated stress signal calibration, RX test, RX LinkEQ and TX LinkEQ according to PCI Express Base Specification 4.0)*
- LinkEQ tests require add-on option N5991PA3-ADD
- “Setup Impairment for Test” function sets the M8040A/M8020A system to user defined impairments. This function supports generator only systems as well as full RX test systems
- Test beyond compliance
  - TxEQ matrix scan for 16 GT/s and 8 GT/s)*
  - JTOL test for 16 GT/s, 8 GT/s, 5 GT/s and 2.5 GT/s)*
  - Sensitivity Test for 8 GT/s, 5 GT/s and 2.5 GT/s)*
- Supports M8040A as well as M8020A

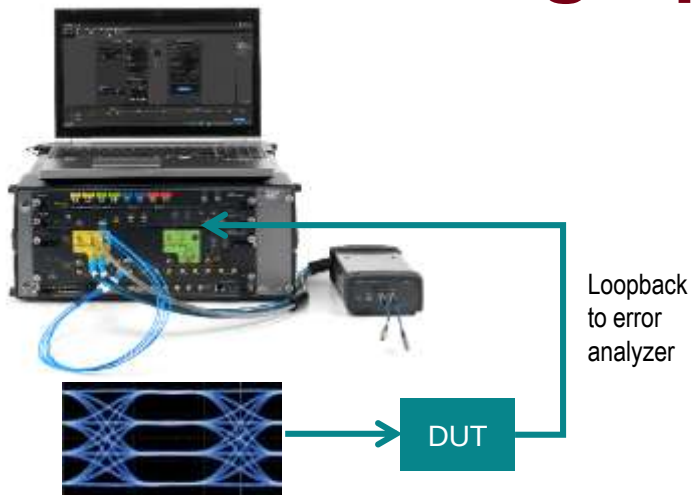
*)5 GT/s and 2.5 GT/s support for M8040A will be added to the released N5991PB4A PCI Express 4.0 Base Specification RX Test product in CY20H1.



Agenda

- PCI Express Generic
- Challenge 1 – Which Test Setup Do You Need?
- Challenge 2 – PCI Express LTSSM
- Challenge 3 – PCI Express Stress Signal
- Challenge 4 – PCI Express RX and LinkEQ Tests
- Challenge 5 – Calibration / Test Complexity and Time
- Solution Overview
- Appendix

M8040A 64 Gbaud High-performance BERT



PAM4 and NRZ
1 and 2 channel pattern generator
with remote heads, de-emphasis, jitter
injection and FEC

Where used:

- 400GbE, 200GbE, CEI-56G
- New: PCI Express, TBT 3, CCIX, SAS
- Input (RX) characterization and compliance test
- For PAM4 and NRZ signals up to 64 Gbaud

Key Capabilities:

- Highly integrated BERT, AXIe based
- Accurate physical layer characterization and compliance test of next generation digital high- speed I/Os with NRZ and PAM4 data formats
- Control via M8070B system software for M8000

Pattern Generator (M8045A)

- Single or dual 32/64 Gbaud NRZ/PAM4
- Built-in de-emphasis (5 taps)
- Clean and jittered data patterns and clocks
- Remote head M8057B: 1.8 Vpp diff. for close connection to DUT
- NRZ and PAM4 is switchable by software
- FEC encoding on 1 lane
- ISI channels and interference source

Error Analyzer (M8046A)

- 32/58Gbaud error detector for PAM4 and NRZ
- Built-in equalization
- Built-in clock recovery
- Supports up to 64Gb/s NRZ, 30GBd PAM4
- Burst error distribution and FLR extrapolation
- Filtering of SKP OS symbols
- Interactive link training 8/16/32 GT/s PCIe

Interference Source M8054A with Coupler

M8054A Interference Source (prelim. outline)

Emulate level interference for RX stress test

- Only usable with M8070A/B or other Keysight RX test automation SW
- BW 32 GHz
- 4 ch
- Random Interference (RI), Sinusoidal Interference (SI)
- Common mode and differential mode
- Near-end and far-end channel injection possible by use of couplers
- Specs similar to today‘s M8196A when used as RI/SI source in M8070A
- Control via M8070A/B

Applications

- PCI Express
- SAS
- OIF-CEI & IEEE 802.3 10G / 100G / 200G / 400G

Interference source

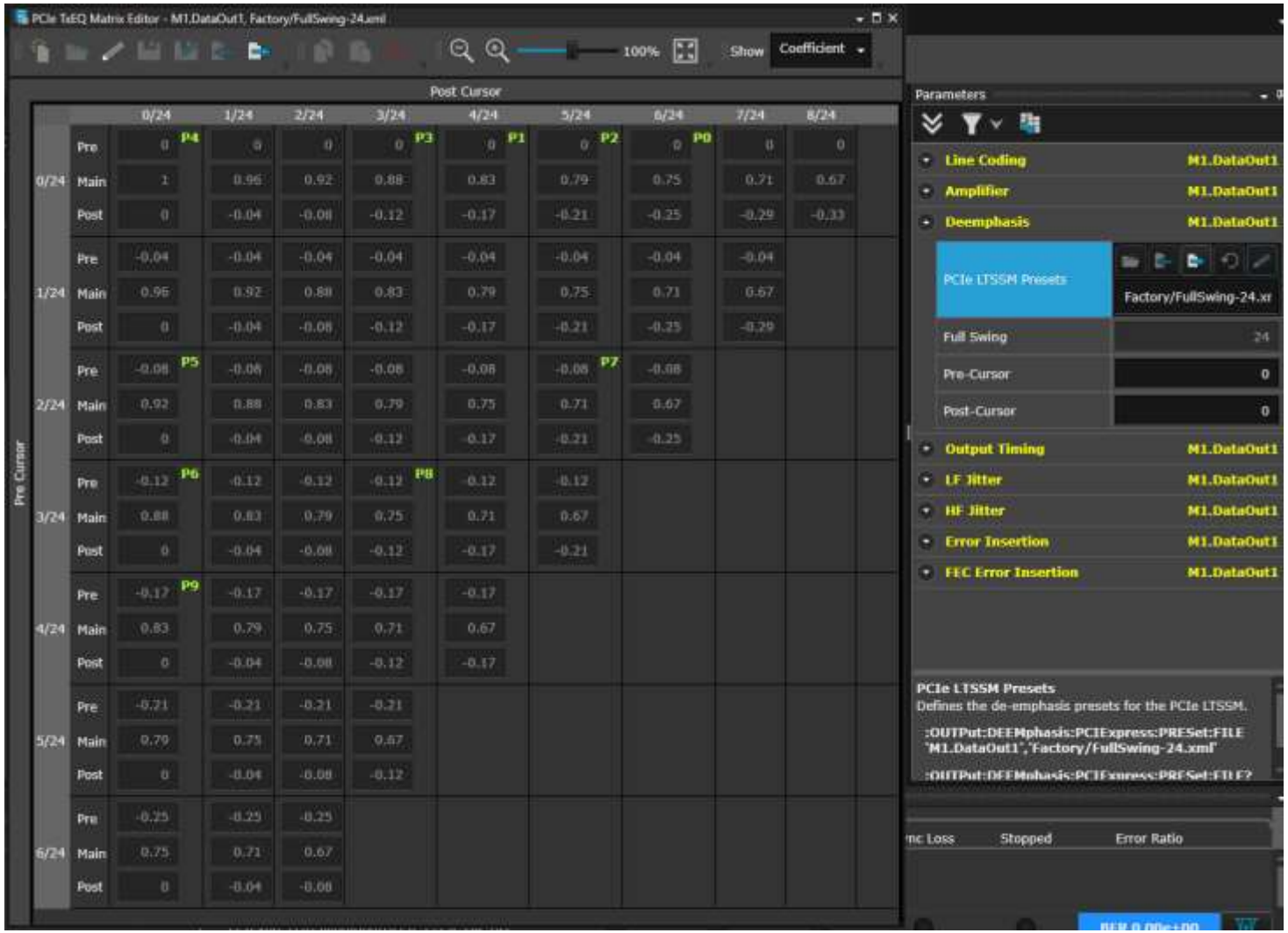
PG

M8045A-803 coupler

PCI Express Interactive Link Training – M8040A

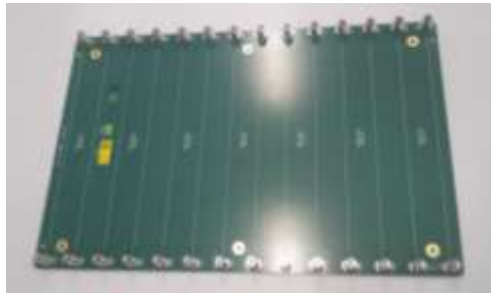
M8046A-0S1 INTERACTIVE LINK TRAINING FOR PCIE 32G/16G/8G – 2

- Coefficient resolution between 1/24 and 1/63. Available on M8040A only.
- PCIe TxEQ Matrix editor to change M8040A's coefficient sets per possible coefficient and preset request. Available on M8040A only

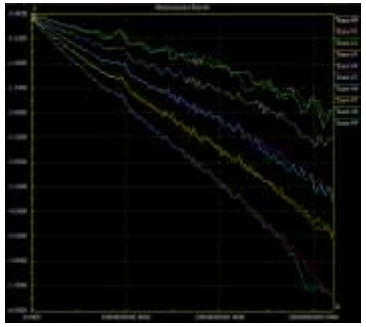


ISI Channels for High-Speed Receiver Test

M8049A



	M8049A-001	M8049A-002	M8049A-003
Description	ISI Channel Board with 5 traces from 1.4 to 5.5 inches	ISI Channel Board with 9 traces from 0.8 to 8.0 inches	ISI Channel Board with 7 traces from 9.1 to 22.3 inches
Traces dB	1.5, 2, 2.5, 3, 3.5 (estimated)	2.5, 3, 3.5, 4, 5, 6, 7, 8, 9 (estimated)	10, 12, 14, 16, 18, 20, 22 (estimated)



Preliminary S21 (Sep 2018)

Key features of ISI Channel boards

- Emulate channel loss with fine granularity -> 3 separately orderable & cascadable boards
- Lower loss needed for 32 Gbd signals
  Applications: PCIe 5, CCIX, SATA, IEEE 802.3, OIF-CEI-56G, Fibre Channel, other >20Gbd applications
- Recommended cables for cascading: M8046A-802 (1m matched cable pair 2.4mm)

Ordering

M8049A-001, -002, -003
Cascading of boards possible

Data Center – Electrical RX Test Applications

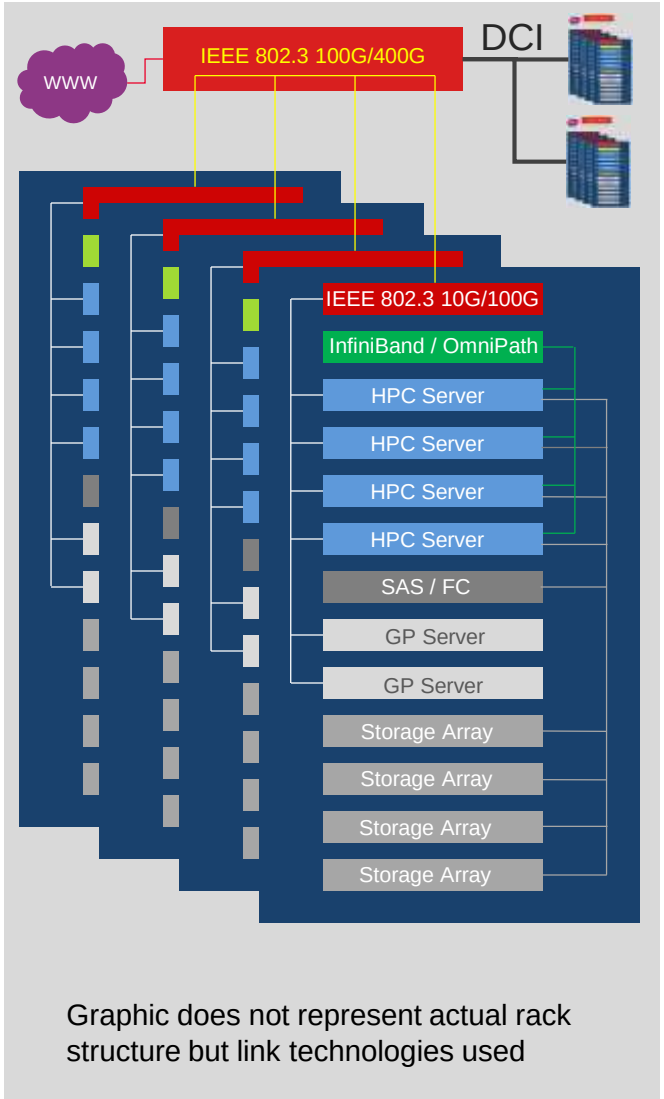
Data Center Network Coverage

Electrical TRX:

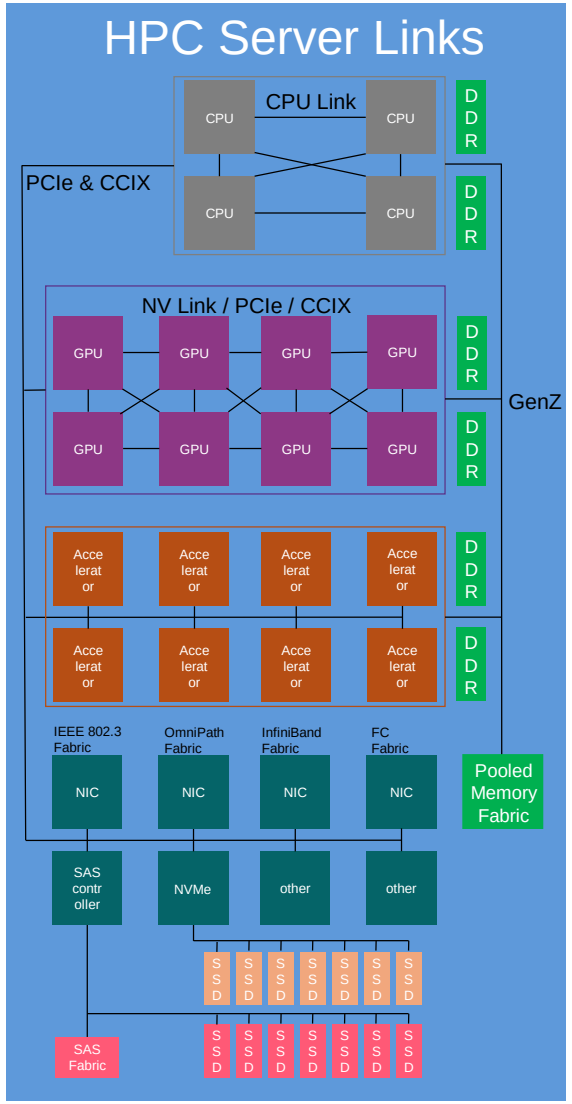
- OIF-CEI CEI-04.0
  - CEI-56G-VSR PAM4 (M8040A only)
- OIF-CEI CEI-03.1
  - CEI-28G-VSR[3)]
- IEEE 802.3
  - 200GAUI-4 PAM4 C2M (M8040A only)
  - 400GAUI-8 PAM4 C2M (M8040A only)

Optical TRX:

- IEEE 802.3
  - 10GBASE-LR/ER (M8020A only)
  - 25GBASE-LR/-ER/-SR (M8040A only)
  - 40GBASE-LR4/ER4 (M8020A only)
  - 100GBASE-LR4/-ER4/-SR4
  - 200GBASE-FR4/-LR4/-DR4 (M8040A only)
  - 400GBASE-FR8/-LR8 (M8040A only)
  - 400GBASE-DR4 (M8040A only)
- MSA
  - 100G-CLR4 MSA
  - 100G CWDM4 MSA
  - 100G 4WDM-10/-20/-40 MSA
  - 400G-FR4 100G lambda MSA



Graphic does not represent actual rack structure but link technologies used



Data Center Server Coverage

- PCI Express®
  - PCI Express Base Spec 5.0
    - 32 GT/s[5)], 16 GT/s, 8 GT/s, 5 GT/s[1)], 2.5 GT/s[1)2)]
  - PCI Express Base Spec 4.0
    - 16 GT/s, 8 GT/s, 5 GT/s[1)], 2.5 GT/s[1)2)]
  - PCI Express Architecture PHY Test Spec for CEM rev. 4.0
    - 16 GT/s, 8 GT/s, 5 GT/s[4)], 2.5 GT/s[4)2)]
  - PCI Express Architecture PHY Test Spec for CEM rev. 3.0
    - 8 GT/s, 5 GT/s[4)], 2.5 GT/s[4)2]
  - PCI Express U.2
    - 8 GT/s
  - PCI Express M.2
    - 8 GT/s
- CCIX 20G/25G
- SAS-3/SAS-4
  - 22.5G, 12G
- OIF-CEI CEI-04.0
  - CEI-56G-MR/-LR PAM4 (M8040A only)
- OIF-CEI CEI-03.1
  - CEI-28G-SR/-MR
  - CEI-25G-LR
- IEEE 802.3
  - 200GAUI-4 PAM4 C2C (M8040A only)
  - 400GAUI-8 PAM4 C2C (M8040A only)
- DDR5 (M8020A only)

RX test automation is available

[1)]M8040A: currently planned for end of CY19

[3)]Test automation available for host only

[4)]According to CEM specification

[5)]M8020A: no LTSSM for 32 GT/s

Server Standard Coverage – M8040A

CCIX
25G/20G

PCI Express 5.0/4.0
32G/16G/8G/5G[1)]/2.5G[1)2)]

CEI-03.1
- CEI-28G-SR/-MR
- CEI-25G-LR

SAS-4/SAS-3
22.5G/12G

IEEE 802.3
- 200GAUI-4 PAM4 C2C
- 400GAUI-8 PAM4 C2C

CEI-04.0
- CEI-56G-MR/-LR PAM4

Optical TRX:
- IEEE 802.3
  - 25GBASE-LR/-ER/-SR
  - 100GBASE-LR4/-ER4/-SR4
  - 200GBASE-FR4/-LR4/-DR4
  - 400GBASE-FR8/-LR8
  - 400GBASE-DR4
- MSA
  - 100G-CLR4 MSA
  - 100G CWDM4 MSA
  - 100G 4WDM-10/-20/-40 MSA
  - 400G-FR4 100G lambda MSA

Electrical TRX:
- CEI-04.0
  - CEI-56G-VSR PAM4
- CEI-03.1
  - CEI-28G-VSR[3)]
- IEEE 802.3
  - 200GAUI-4 PAM4 C2M
  - 400GAUI-8 PAM4 C2M

Consumer/Computer:
TBT 3.0 20G

RX test automation is available
[1)]Currently planned for end of CY19
[2)]2.5G requires M8046A L4 hardware which is not shipping as of May 2019
[3)]Test automation available for host only

Consumer / Computer Standard Coverage – M8020A

TBT 3.0
20G

DDR5

USB 3.0/3.1/3.2
5G/10G

DisplayPort
RBR/HBR/HBR2/HBR3

PCI Express 5.0/4.0/3.0
16G/8G/5G/2.5G

CEI-03.1
- CEI-28G-SR/-MR
- CEI-25G-LR

SAS-4/SAS-3
22.5G/12G

MIPI M-PHY

SATA-1/-2/-3
1.5G/3G/6G

UHS-II
1.5G/3G

Optical TRX:
- IEEE 802.3
  - 10GBASE-LR/ER
  - 40GBASE-LR4/ER4
  - 100GBASE-LR4/-ER4/-SR4
- MSA
  - 100G-CLR4 MSA
  - 100G CWDM4 MSA
  - 100G 4WDM-10/-20/-40 MSA

RX test automation is available

M8040A vs J-BERT M8020A

QUICK COMPARISON

Feature	M8040A	J-BERT M8020A 16G/32G
Data rate range	2- 64.8 GBaud	1-32.4 Gb/s
Data formats	PAM-4, NRZ	NRZ
Adjustable ISI	No	Yes, internal
De-emphasis taps	4	8
De-emphasis resolution	1% in GUI	0.1 dB
Channels per 5-slot chassis	1-2 w/ adj. delay	M8041A+ 51A: 4x 16G M8062A, 1x 32G
x-point adjust	No	Yes
Level interference	Yes, using M8054A or M8195A/96A + couplers	Yes, SI (internal source for M8041A, superposition for M8062A)
Equalizer	Yes (FFE)	Yes (CTLE)
Clock recovery	Yes	Yes
BER Scan	Yes(NRZ), no (PAM4)	Yes
Eye diagram	No, but sampling point view with level histogram	M8041A: Yes M8062A: only with external clock
Capture	Yes (raw data)	Yes
Filtering of filler symbols	Yes, for PCI Express 8G/16G/32G and CCIX 20G/25G. Planned for PCIe 2.5G[1)2)] and 5G[2)], USB 3.0/3.1 5G[2)]/10G[2)], SATA 3G[1)2)]/6G[2)] and SAS 12G[2)]	M8041A/51A: Yes, 8b/10b, PCIe 8G/16G, USB 3.1 10G M8062A: No
Burst mode	Only masking	No
Interactive link training	Yes, for PCIe 8G/16G/32G, planned for USB 3.0/3.1 5G[3)]/10G[3)]	Yes, for PCIe 8G/16G and USB 3.1/3.0 5G/10G
FEC encoding	Yes, 50GBASE-R	No
ED- only	Yes	No

[1)]Planned for CY20H1
[2)]Planned for CY19Q4

M8070EDAB – Error Distribution Analysis

ERROR DISTRIBUTION & FRAME LOSS RATIO

- Analyzes symbol error occurrences in a FEC frame
  - Provides a histogram view symbol errors per FEC frame
  - Consecutive error occurrences
  - Error map
- Measures and estimates FLR
- User definable
  - Bits per symbol
  - Symbols per FEC frame
  - Correctable symbols per FEC frame
  - Number of frames per capture

Investigate effectiveness of different FEC algorithms for a NRZ or PAM4 transmission line

PCI Express RX and Link EQ Test

Questions?

Thanks a lot for your time!

Further information available on

Keysight's overall PCI Express solution offering

PCI Express RX and LinkEQ Test

PCI Express 4.0 TX Test

PCI Express 5.0 TX Test

SAS RX Test

SAS TX Test

J-BERT M8020A

M8040A 64 Gbaud High-performance BERT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