PCI Express 5.0 Full Speed Ahead

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2019 OCT

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Agenda

- PCI Express 5.0 Motivation to 32 GT/s
- PCIe 5.0 Development Timeline
- PCIe 5.0 Goals
- PCIe 5.0 Electrical Details
- PCIe 5.0 TX Test Tools
- PCIe 4.0 System board Dual Port test & Appendix D
- PCIe 5.0 RX Test Tools



Motivation for PCIe Gen5 at 32 GT/s NRZ

PCIE 5.0 SPEC W/ 32 GT/S BANDWIDTH IDEAL FOR:)

- High-end networking solutions (400 Gb Ethernet and dual 200 Gb/s InfiniBand technologies)
- Accelerator and GPU attachments for high bandwidth applications
- Constricted form factors that cannot increase lane width but need higher bandwidth



Drivers of PCIe 5.0 Performance

- High-end networking
 - 400 Gb Ethernet
 - Dual 200 Gb/s InfiniBand
- Storage networking
 - NVM Express (NVMe)
 - Big Data
- Increased IC I/O speeds
 - Co-Processors (FPGA, GPU)
 - ASIC

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- IP
- Artificial intelligence engines

Coherent Bandwidth by Speed



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Industry Drives Higher PCIe Bandwidth Requirements

- PCIe 5.0 = 32 Gb/s
- Required for 400 Gb Ethernet
 - This equates to 50 GB bidirectionally
 - 16 lanes gives up to 64 GB/s
 - Total full duplex BW = 128 GB/s
- CEM connector for PCIe 5 is planned to be backward compatible with earlier PCIe technologies.
- Tentative schedule for spec release in 2019

	Raw Bit Rate/Lane	Link BW	BW/Lane	Total x16 Bi- Directional Bandwidth
PCIe 1.x	2.5 GT/s	2 Gb/s	250 MB/s	8 GB/s
PCIe 2.x	5.0 GT/s	4 Gb/s	500 MB/s	16 GB/s
PCIe 3.x	8.0 GT/s	8 Gb/s	~1 GB/s	~32 GB/s
PCIe 4.x	16.0 GT/s	16 Gb/s	~2 GB/s	~64 GB/s
PCle 5.x	32.0 GT/s	32 Gb/s	~4 GB/s	~128 GB/s



PCI Express Technology Roadmap



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PCI Express Standards Development



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PCI Express Specifications and Scope

PCI Express" Architecture PCI Express* PCI Express² **Base Specification PHY Test Specification Card Electromechanical** Specification PCI PCI> PCI **Base Specification Phy Test Specification** Card Electromechanical (CEM) Spec Contains all the Defines compliance Applies to Add-In Cards and system knowledge tests of CEM spec in Mother Boards Can directly be detail ٠ Mitigates card manufacturer's applied to Chip need to study the base Test specification Increases reproducibility through PCI-SIG supplied test tools CBB and CLB (compliance base and PCIe 5.0 BASE load board) Currently in review v0.9

Select the specifications that relate to your specific need



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PCIe 5.0 – Goals

DELIVERING THE FASTEST PCIE SPEED YET

- PCIe 5.0 is backwards compatible with prior generations.
 - Enhanced SMT connector
 - Same pinout
- Signaling is doubled (vGen4) to 32 GT/s
 - Minimal spec changes only ones needed to enable speed bump.
 - EIEOS changed to maintain frequency
 - Data rate bit defined
 - Encoding remains 128/130
 - Loss budget: Goal 35-36 dB
 - Equalization: 8 GT->16 GT-> 32 GT/s
- Scaled flow control & extended tags from PCIe 4.0 sufficient for 32 GT/s.



PCIe Gen5

GOALS

- BER target is 10e-12
- TX Presets P0-P10 to remain the same
- Backward compatibility with previous PCIe Gen1/2/3/4
- Same approach for TX and RX testing used for Gen4
 - Similar method for TX testing via de-embedding of breakout board traces
 - Similar method for calibrating the eye width and eye height as used with PCIe 4.0 (ISI based, fixed RJ)
- Same TX Voltage and Jitter parameters as Gen4



PCI Express 5.0 Channel Topology

RETIMER REQUIRED WHEN LOSS EXCEEDS -36 DB OR >1 CONNECTOR



Longer Channel

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- Estimated allowable loss: ~= -36 dB @ 16 GHz
- Root complex pkg loss allowance ~= -9 dB @ 16 GHz
- Add-in Card pkg loss allowance ~= -4 dB @ 16 GHz
- Total AIC loss budget estimate = ~9 dB @ 16 GHz
- PCIe 5.0 CEM Connector loss budget ~= 1.5 dB @ 16 GHz



PCIe 5.0 Reference Clock and PLL Bandwidth Requirements

HIGHER SPEEDS = TIGHTER PHASE JITTER LIMITS

Data Rate	CC Jitter Limit
2.5 GT/s	86 ps (pk-pk)
5 GT/s	3.1p s (RMS)
8 GT/s	1.0 ps (RMS)
16 GT/s	0.5 ps (RMS)
32 GT/s	0.15 ps (RMS)

- PCIe 5.0 specifies a short channel and a 50 ohm termination (100 ohm differential termination) for reference clock phase jitter measurements only.
- Lower PLL bandwidth limit for 8.0 and 16.0 GT/s reduced to 0.5 MHz
 - Revised model CDR at 16GT/s for backward compatibility
 Reduced TX UTJ limit at 8GT/s for backward compatibility

	0.01 dB peaking	2.0 dB peaking	32.0 G1/s CC	CDR	
BW _{PLL} (min) = 0.5 MHz	ω_{n1} = .112 Mrad/s ζ_1 = 14	ω_{n1} = 1.51 Mrad/s ζ_1 = 0.73		4	
BW _{pu} (max) = 1.8	ω_{n1} = .403 Mrad/s	ω _{n1} = 5.42 Mrad/s			
3W _{pu} (max) = 1.8	ω_{n1} = .403 Mrad/s	ω_{n1} = 5.42 Mrad/s			



PCIe 5.0 32GT/s RX Calibration (BASE)

15 MV EYE HEIGHT POST EQ (0.3 UI EYE WIDTH) TARGET





PCIe 5.0 32GT/s RX Calibration (BASE) Example

TARGET TEST CHANNEL BOARD W/ NEW CEM SMT CONNECTOR



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PCIe 5.0 TX Test Tools



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PCIe 5.0 32 GT/s TX Testing

BREAKOUT CHANNEL FOR ASIC REQUIRED



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D9050PCIC New Features

MASTER YOUR BEST DESIGN

- Supports PCIe 5.0 BASE TX testing at 32 GT/s as well as 2.5G, 5G, 8G and 16GT/s (v0.9 BASE)
- Supports PCIe 5.0 reference clock tests (2.5G, 5G, 8G, 16G)
- Will support CEM tests for endpoints and root complexes (2.5G, 5G, 8G, 16G, 32G).
- Integrated De-embedding of break-out channel with optional InfiniiSim
- Automated DUT control using an 81150/60A pulse generator ARB.
- Enhanced switch matrix supporting arbitrary lane mapping
- Minimum oscilloscope BW: 50 GHz



Keysight D9050PCIC PCIe 5 (Gen5) TX Test Application

5.0 BASE SPEC TESTS

₹	PCI-	Expres	s Gen5	Test Applica	tion Nev	/ Devi	:e1					
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PCIe 4.0 Dual Port Testing

EXCERPTS FROM PCIE 4.0 TEST SPEC V1.0

Results of the Board Election

PCI

o 2019-2020 PCI-SIG Board of Directors

- Gord Caruk
- Dong Wei
- Greg Casey
- Al Yanes
- Debendra Das Sharma (intel)
- Rick Eads
- Michael Diamond
- Rick Wietfeldt
- Richard Solomon

IBM.

Qualcom

SYNOPSYS'

Silican to Software

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PCI Express Specifications and Scope

SELECT THE SPECIFICATIONS THAT RELATE TO YOUR SPECIFIC NEED





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PCIe 4.0 Test Spec

PCIE 4.0 OFFICIAL INTEGRATORS LIST NOW OPEN

- PCIe 4.0 Test Spec v1.0 now approved
 - Some typos and minor corrections still linger
- Phy layer integrators list required testing:
 - System Board (16G)
 - TX signal quality (Preset tests, signal quality via dual port method)
 - RX: LinkEQ Response Test.
 - RX Link Equalization test
 - Add-in card (16G)
 - TX Signal quality (Preset tests, signal quality)
 - TX PLL
 - TX Pulse width jitter
 - RX: Initial TX EQ test
 - RX: LinkEQ Response Test.
 - RX Link Equalization test



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PCIE 4.0 CEM Fixture Setup

PHY TX MEASUREMENTS



Add-in Card (end point)





PCIE 4.0 CEM Motherboard Tests

DUAL PORT TESTING IS THE REQUIRED METHOD



System Board (root port)

Appendix D. Alternate Method of System TX Signal Quality Test at 16GT/s

An alternate method of performing 16GT/s System Signal Quality test is provided in this note. The data and 100 MHz reference clock can be captured and post-processed separately. The data will be processed with SigTest using the 16GT/s Add-in Card Signal Quality template file (PCIe_4_16G_CEM.dat). The pass/fail limits for Eye Width at 1E-12 and Eye Height at 1E-12 will remain unchanged for 16 GT/s System Signal Quality Test. The reference clock will be post-processed with a separate clock tool to ensure the Random Jitter is less than or equal to 0.7 ps RMS as defined in the *PCI Express Base Specification*.

The signal quality test described in Section 2.7.5 is the required test method for System Tx Signal Quality testing at 16 GT/s. This alternate method is only to be used when the signal quality test described in Section 2.7.5 fails.

2.7.5 System Board Transmitter Electrical Compliance Test for 16.0 GT/s

1. Connect the Tx lane under test ...

2. Connect the Reference Clock (REF CLK) on the CLB to a high-speed oscilloscope ...

3. ...push the compliance toggle button on the CLB until the correct Tx EQ is selected...

4. Measure transmitted clock and data waveforms simultaneously with a high-speed oscilloscope or equivalent data capture instrument with the maximum bandwidth set to 25GHz



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PCIE 4.0 CEM Motherboard Tests

WHY HAVE TWO METHODS?



- Dual Port testing was always the POR for PCIe 4.0
- Appendix D was added as a contingency.
 - Initially Sigtest showed issues if max SSC was enabled.
 - New Intel developer resolved the Sigtest SSC issue with a novel approach.
 - All System Boards tested at WS#110 were tested using the dual port approach.
- Dual Port uses both clock and data and represents the AIC view of root port signal quality.
- System board vendors can trade off ref clock jitter for better TX jitter and still be compliant.

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PCIe 5.0 RX Test Tools



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M8040A 64 GBaud High-Performance BERT



Master your next generation PCIe design

- Highly integrated for simplified RX test setup for 400G and PCIe5
- Upgrade paths towards 32 Gbaud PAM4 and 64 Gb/S NRZ
- Most complete solution with test automation
- PCI-SIG gold-suite approved vendor



New: PCI Express Interactive Link Training 8/16/32 GT/s

M8046A-0S1 INTERACTIVE LINK TRAINING FOR PCIE 32G/16G/8G

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PCIe 32G/16G/8G RX Test Setup

SETUP USING M8040A 64G HIGH-PERFORMANCE BERT





New: Interference Source M8054A with Coupler



M8054A interference source module

Emulate level interference for RX stress test

- Designed specifically for M8070A or other dedicated Keysight RX test automation SW
- BW 32 GHz
- 4 ch outputs
- Drives combined Random Interference (RI) and Sinusoidal Interference (SI)
- Common mode and differential mode
- Near-end and far-end channel injection possible by use of couplers
- Specs similar to today's M8196A when used as RI/SI source in M8070A
- Control via M8070A/B

Interference source





M8045A-803 coupler



ISI Channels for High-Speed Receiver Test

M8049A





Preliminary S21 (Sep 2018)

Key features of ISI channel boards

- Emulate channel loss with fine granularity -> 3 separately orderable & cascadable boards
- Lower loss needed for 32 Gbaud signals Applications: PCIe 5, CCIX, IEEE 802.3, OIF-CEI-56G, Fibre Channel, other >20 Gbd applications
- Recommended cables for cascading: M8046A-802 (1 m matched cable pair 2.4 mm)



N5991PxxA

RX TEST AUTOMATION - CALIBRATION

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- Guided and automated stress signal calibration for PCI Express 5.0 32 GT/s^{*})
- "Setup Impairment for Test" function sets the M8040A/M8020A system to user defined impairments. This function supports generator only systems as well as full RX test systems
- TxEQ matrix scan, JTOL test, sensitivity test and RX test
- Contact Keysight representative for latest release timing.

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L0_Cal_32GTps_CompEye

for PCIe 5.0 RootComplex ASIC

SERT System	Keysight N8040A J-852T, H8070A, SH: DE560002						
Generator Channel Channel	M1.DstwDut1						
Offline	False						
Scope Bandwidth	33 GHz						
Number of Averages	21						
Number of Waveform Averages	1024						
Optimize CTLE	True						
Trace Number	1						
Total Channel Logs	-38.695 dB						
Fre-Shoot	3.5 dB						
De-Emphasis	0 dB						
Man Number of Search Steps	7						
Use nominal EN/EW results from Fre Comp Cal	True						
Sinusoidal Jitter Frequency	100 MHz						
Common Hode Interference	0 V						
Random Jitter	500 fe						
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PCI Express® 5.0 – Keysight Total Solution





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