PCI Express 5.0 Full Speed Ahead

Francis Liu / Jacky Yu	***2019 OCT***
Sr. Program Manager / Keysight Technologies	

Agenda

- PCI Express 5.0 Motivation to 32 GT/s
- PCIe 5.0 Development Timeline
- PCIe 5.0 Goals
- PCIe 5.0 Electrical Details
- PCIe 5.0 TX Test Tools
- PCIe 4.0 System board Dual Port test & Appendix D
- PCIe 5.0 RX Test Tools

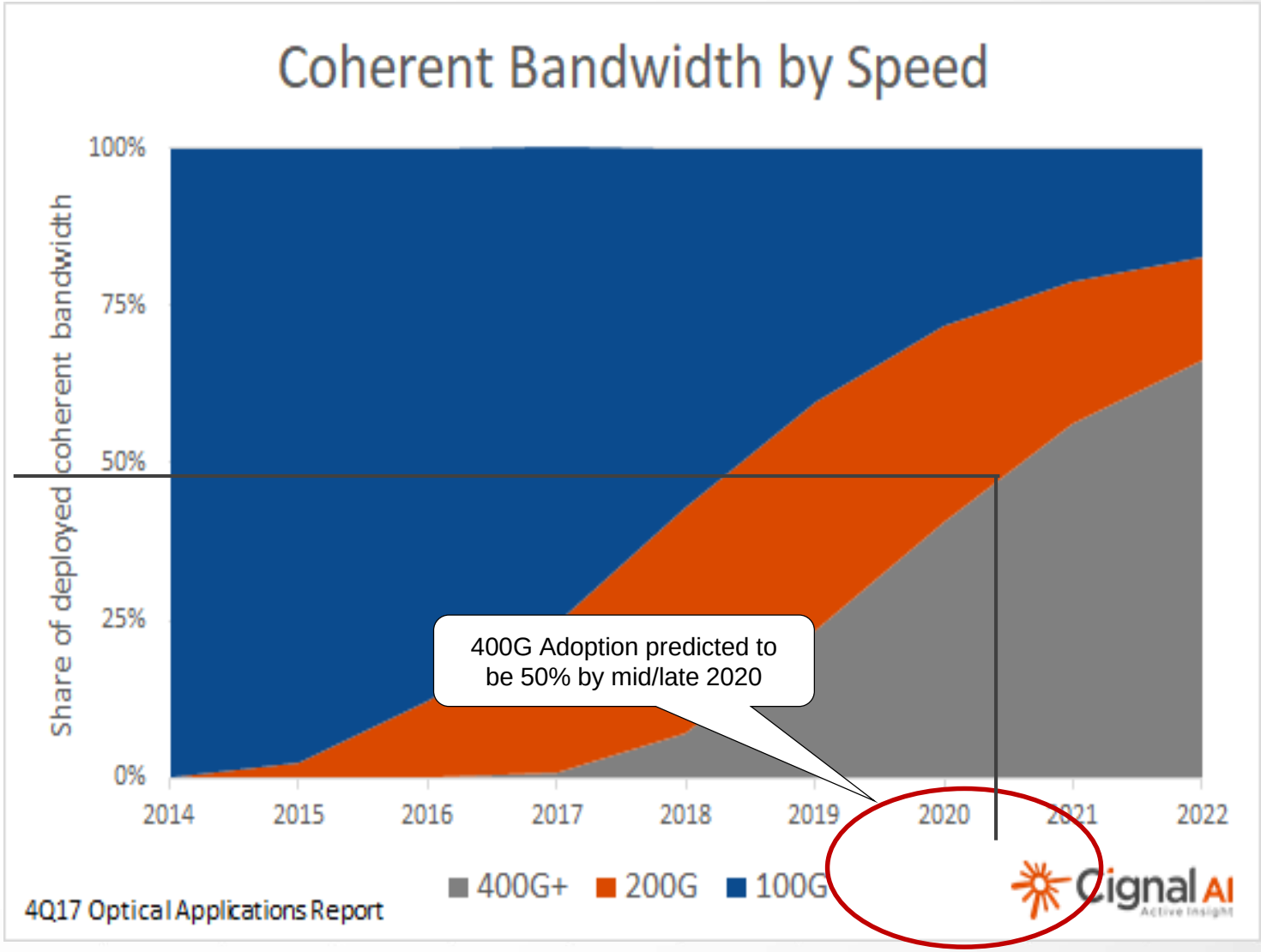
Motivation for PCIe Gen5 at 32 GT/s NRZ

PCIE 5.0 SPEC W/ 32 GT/S BANDWIDTH IDEAL FOR:)

- High-end networking solutions (400 Gb Ethernet and dual 200 Gb/s InfiniBand technologies)
- Accelerator and GPU attachments for high bandwidth applications
- Constricted form factors that cannot increase lane width but need higher bandwidth

Drivers of PCIe 5.0 Performance

- High-end networking
  - 400 Gb Ethernet
  - Dual 200 Gb/s InfiniBand
- Storage networking
  - NVM Express (NVMe)
  - Big Data
- Increased IC I/O speeds
  - Co-Processors (FPGA, GPU)
  - ASIC
  - IP
  - Artificial intelligence engines

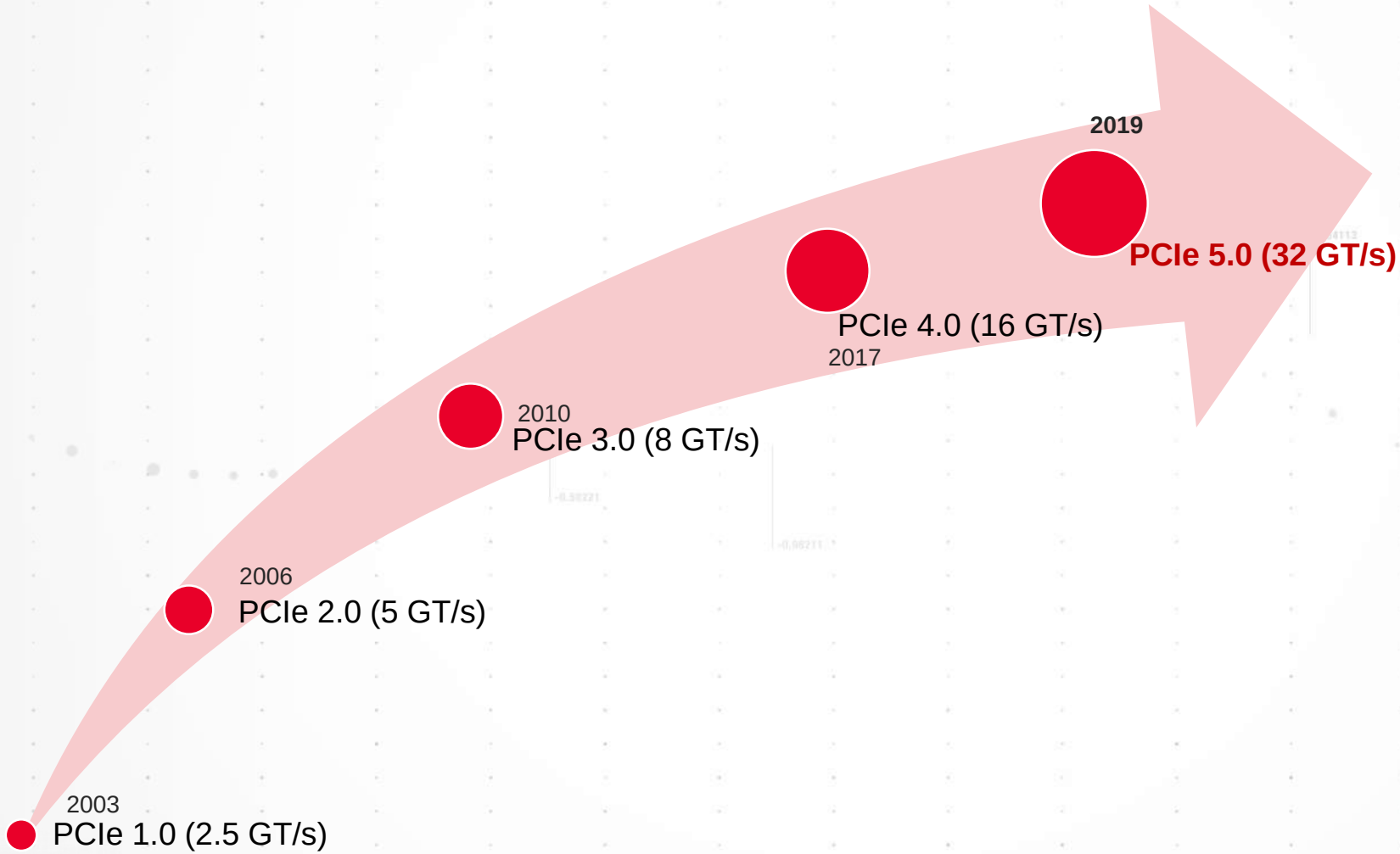


Industry Drives Higher PCIe Bandwidth Requirements

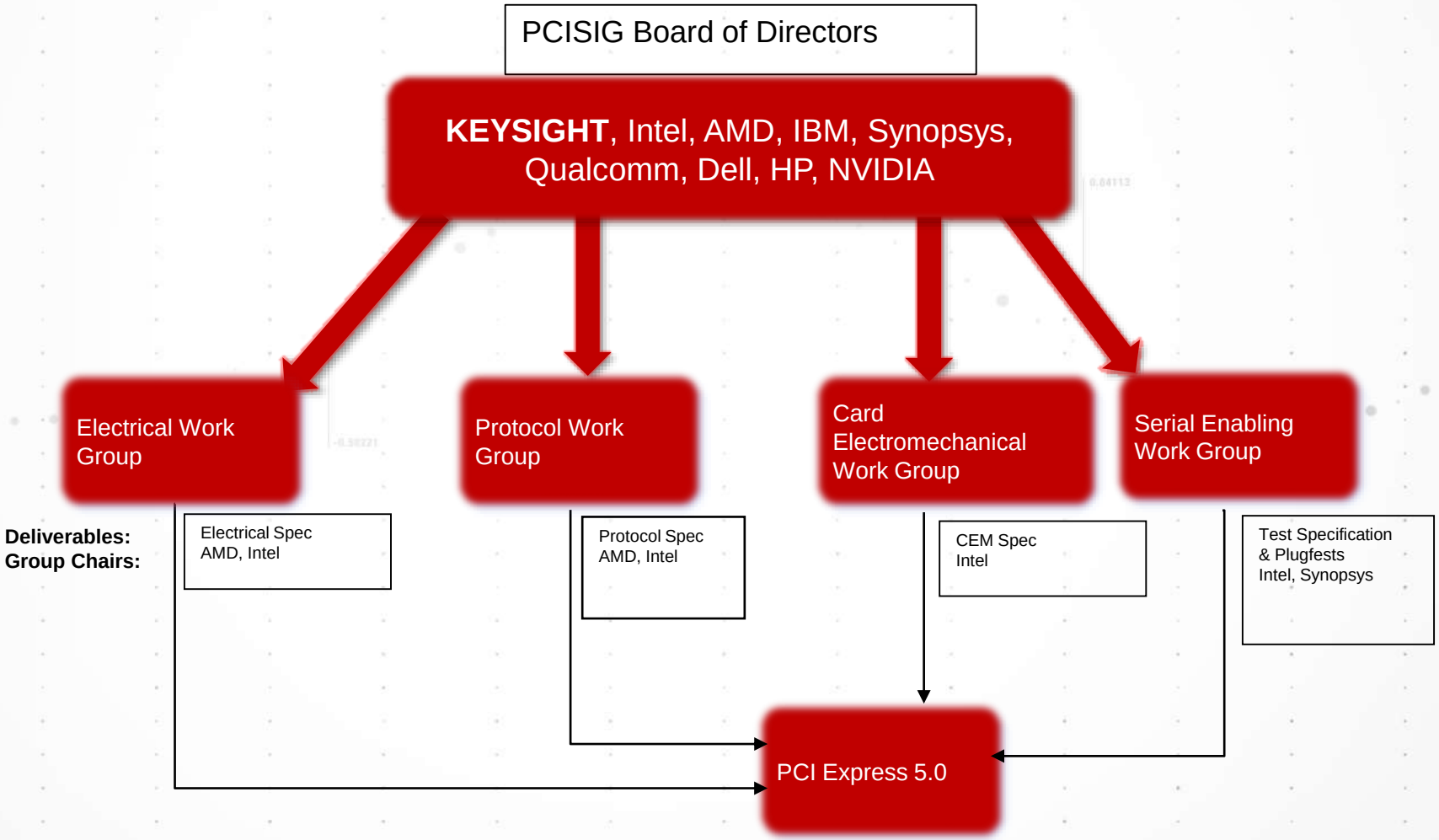
- PCIe 5.0 = 32 Gb/s
- Required for 400 Gb Ethernet
  - This equates to 50 GB bidirectionally
  - 16 lanes gives up to 64 GB/s
  - Total full duplex BW = 128 GB/s
- CEM connector for PCIe 5 is planned to be backward compatible with earlier PCIe technologies.
- Tentative schedule for spec release in 2019

	Raw Bit Rate/Lane	Link BW	BW/Lane	Total x16 Bi-Directional Bandwidth
PCIe 1.x	2.5 GT/s	2 Gb/s	250 MB/s	8 GB/s
PCIe 2.x	5.0 GT/s	4 Gb/s	500 MB/s	16 GB/s
PCIe 3.x	8.0 GT/s	8 Gb/s	~1 GB/s	~32 GB/s
PCIe 4.x	16.0 GT/s	16 Gb/s	~2 GB/s	~64 GB/s
PCIe 5.x	32.0 GT/s	32 Gb/s	~4 GB/s	~128 GB/s

PCI Express Technology Roadmap

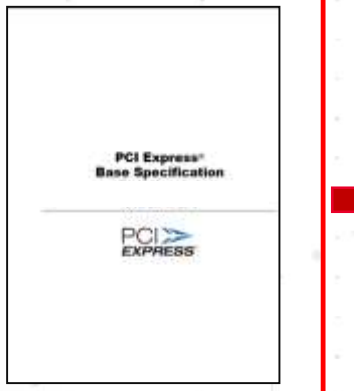


PCI Express Standards Development



PCI Express Specifications and Scope

Select the specifications that relate to your specific need



Base Specification
- Contains all the system knowledge
- Can directly be applied to Chip Test

PCIe 5.0 BASE
Currently in review v0.9

Card Electromechanical (CEM) Spec
- Applies to Add-In Cards and Mother Boards
- Mitigates card manufacturer's need to study the base specification
- Increases reproducibility through PCI-SIG supplied test tools CBB and CLB (compliance base and load board)

Phy Test Specification
- Defines compliance tests of CEM spec in detail

PCIe 5.0 – Goals

DELIVERING THE FASTEST PCIE SPEED YET

- PCIe 5.0 is backwards compatible with prior generations.
  - Enhanced SMT connector
  - Same pinout
- Signaling is doubled (vGen4) to 32 GT/s
  - Minimal spec changes – only ones needed to enable speed bump.
  - EIEOS changed to maintain frequency
  - Data rate bit defined
  - Encoding remains 128/130
  - Loss budget: Goal 35-36 dB
  - Equalization: 8 GT->16 GT-> 32 GT/s
- Scaled flow control & extended tags from PCIe 4.0 sufficient for 32 GT/s.

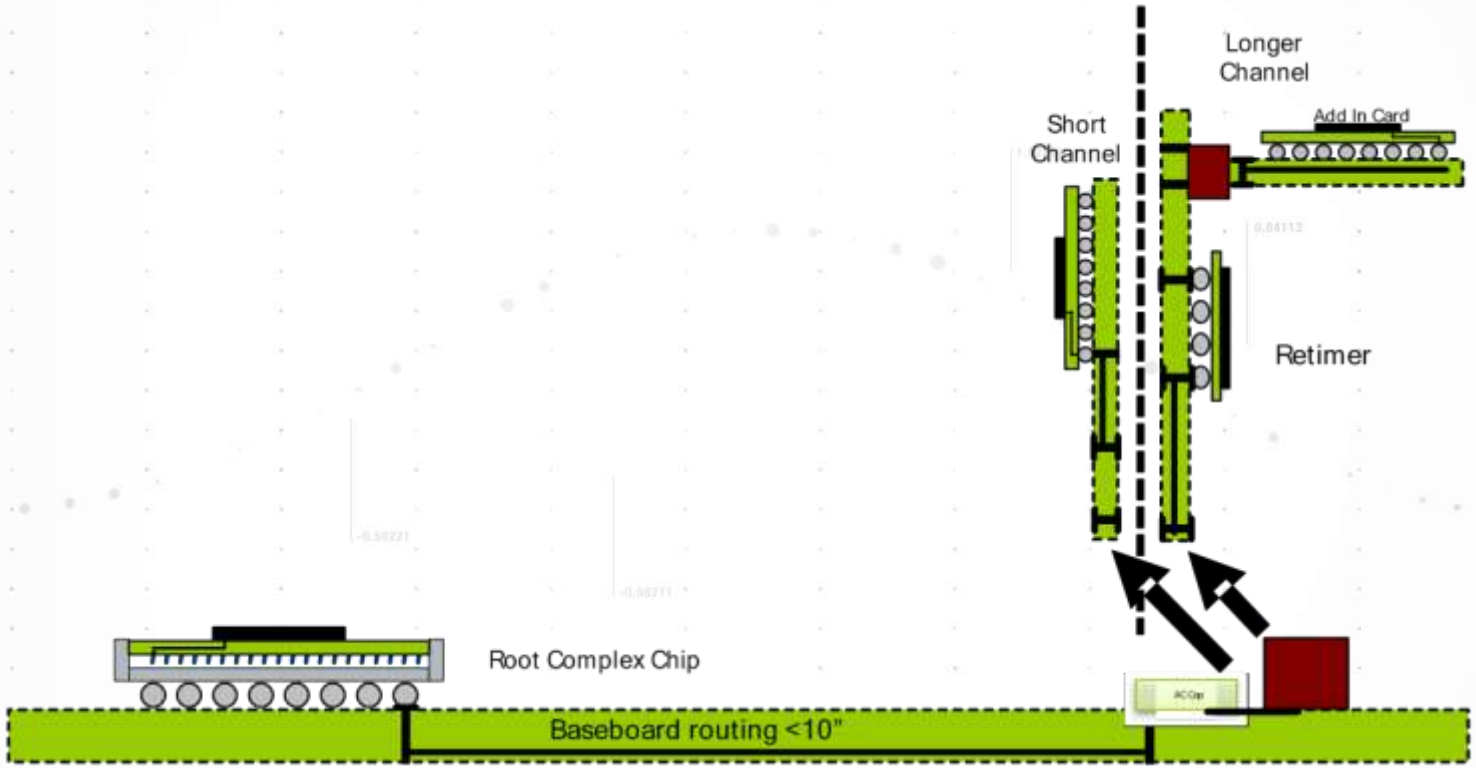
PCIe Gen5

GOALS

- BER target is 10e-12
- TX Presets P0-P10 to remain the same
- Backward compatibility with previous PCIe Gen1/2/3/4
- Same approach for TX and RX testing used for Gen4
  - Similar method for TX testing via de-embedding of breakout board traces
  - Similar method for calibrating the eye width and eye height as used with PCIe 4.0 (ISI based, fixed RJ)
- Same TX Voltage and Jitter parameters as Gen4

PCI Express 5.0 Channel Topology

RETIMER REQUIRED WHEN LOSS EXCEEDS -36 DB OR >1 CONNECTOR



- Estimated allowable loss: ~= -36 dB @ 16 GHz
- Root complex pkg loss allowance ~= -9 dB @ 16 GHz
- Add-in Card pkg loss allowance ~= -4 dB @ 16 GHz
- Total AIC loss budget estimate = ~9 dB @ 16 GHz
- PCIe 5.0 CEM Connector loss budget ~= 1.5 dB @ 16 GHz

PCIe 5.0 Reference Clock and PLL Bandwidth Requirements

HIGHER SPEEDS = TIGHTER PHASE JITTER LIMITS

Data Rate	CC Jitter Limit
2.5 GT/s	86 ps (pk-pk)
5 GT/s	3.1p s (RMS)
8 GT/s	1.0 ps (RMS)
16 GT/s	0.5 ps (RMS)
32 GT/s	0.15 ps (RMS)

- PCIe 5.0 specifies a short channel and a 50 ohm termination (100 ohm differential termination) for reference clock phase jitter measurements only.
- Lower PLL bandwidth limit for 8.0 and 16.0 GT/s reduced to 0.5 MHz
  - Revised model CDR at 16GT/s for backward compatibility
  - Reduced TX UTJ limit at 8GT/s for backward compatibility

PLL #1, PLL #2	0.01 dB peaking	2.0 dB peaking
BW_{PLL}(min) = 0.5 MHz	ω_{n1}= .112 Mrad/s ζ_1 = 14	ω_{n1}= 1.51 Mrad/s ζ_1 = 0.73
BW_{PLL}(max) = 1.8 MHz	ω_{n1}= .403 Mrad/s ζ_1 = 14	ω_{n1}= 5.42 Mrad/s ζ_1 = 0.73

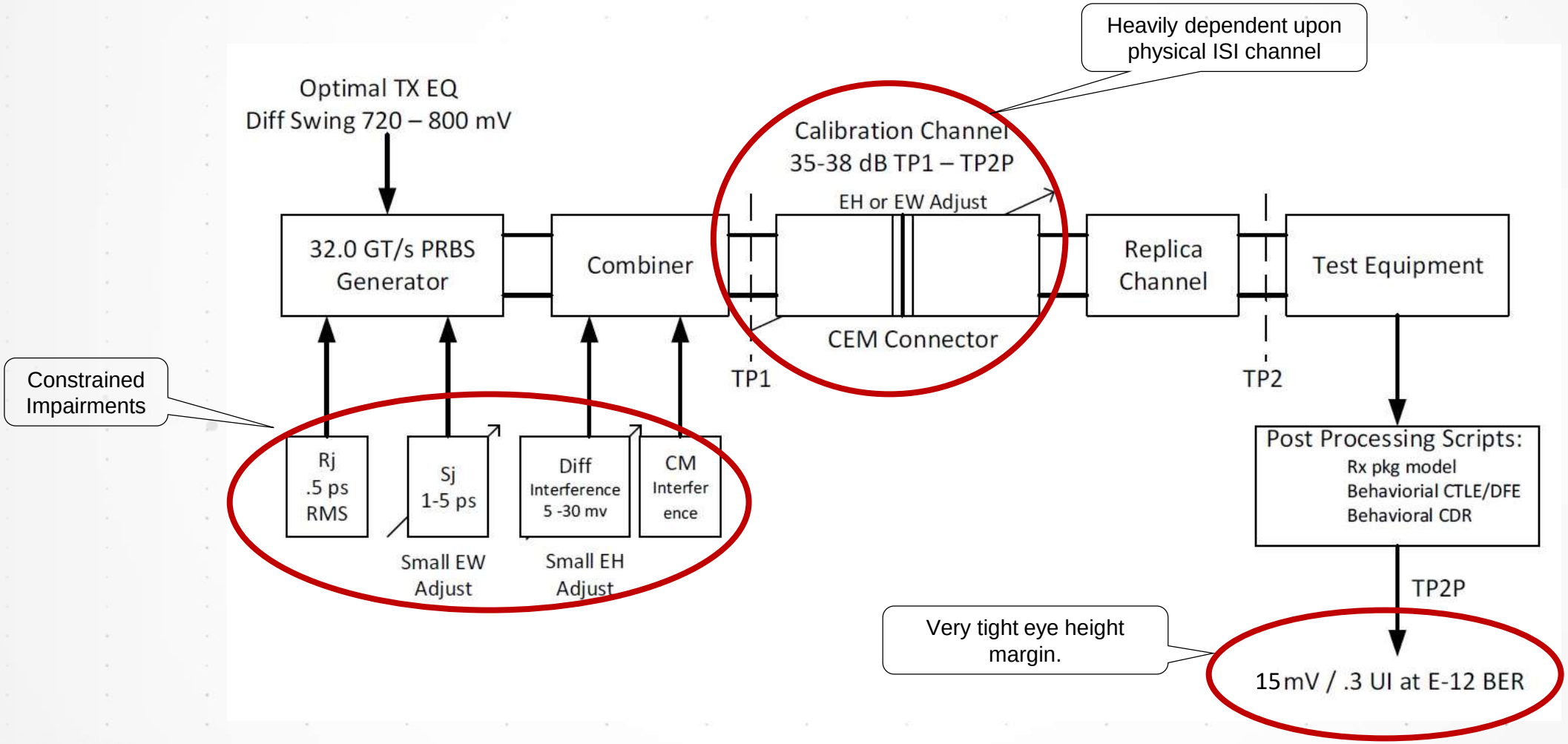
32.0 GT/s CC **CDR**

16 combinations

32.0 GT/s

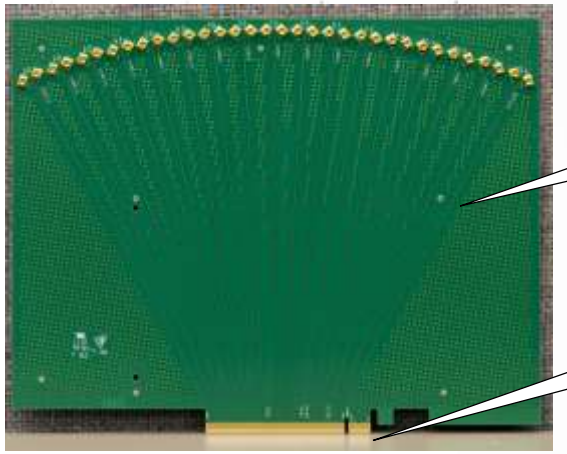
PCIe 5.0 32GT/s RX Calibration (BASE)

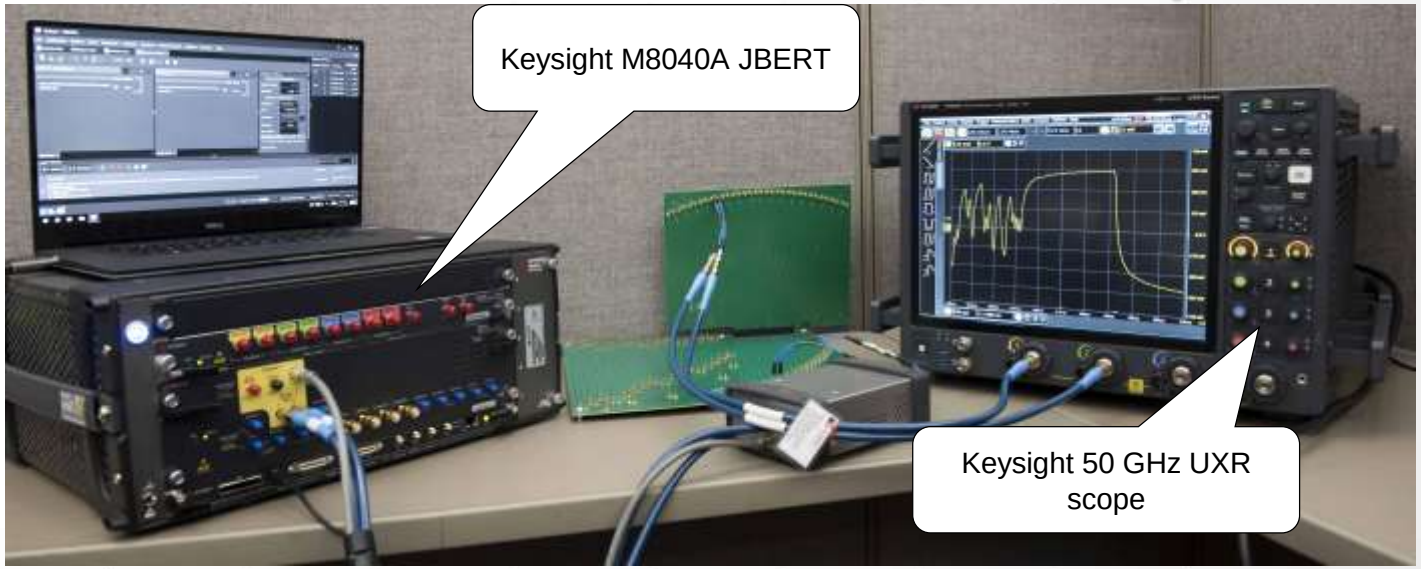
15 MV EYE HEIGHT POST EQ (0.3 UI EYE WIDTH) TARGET



PCIe 5.0 32GT/s RX Calibration (BASE) Example

TARGET TEST CHANNEL BOARD W/ NEW CEM SMT CONNECTOR





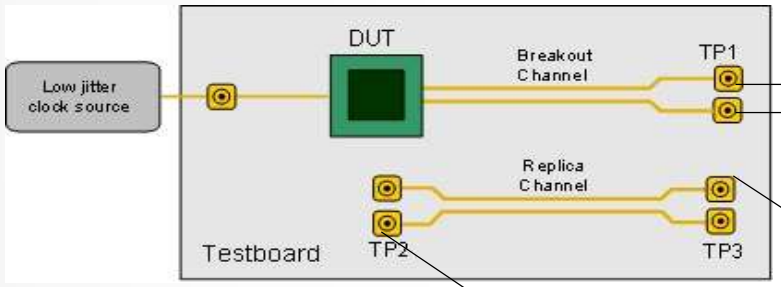
PCIe 5.0 TX Test Tools

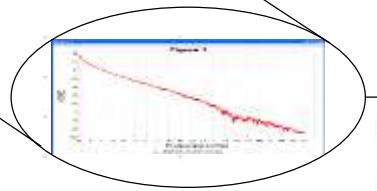
PCIe 5.0 32 GT/s TX Testing

BREAKOUT CHANNEL FOR ASIC REQUIRED

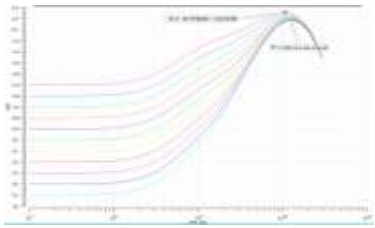
Keysight UXR-Series Real Time Oscilloscope

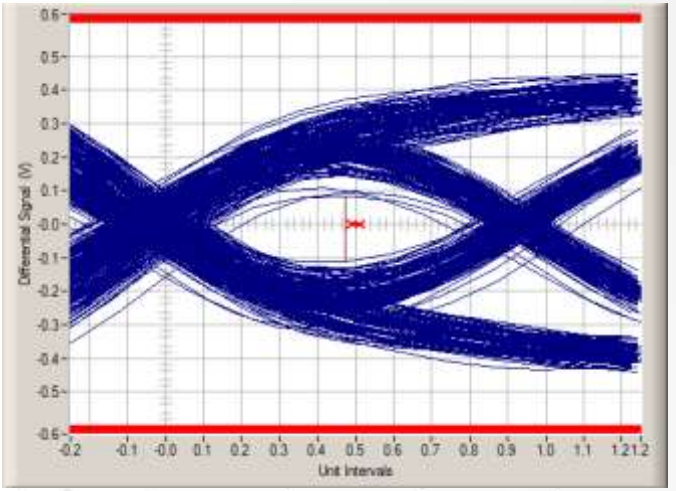
PCIe 5.0 ASIC/IC custom breakout board





S-Parameters of Replica Ch. Used to de-embed to pin or Ref CTLE can be used (12dB).





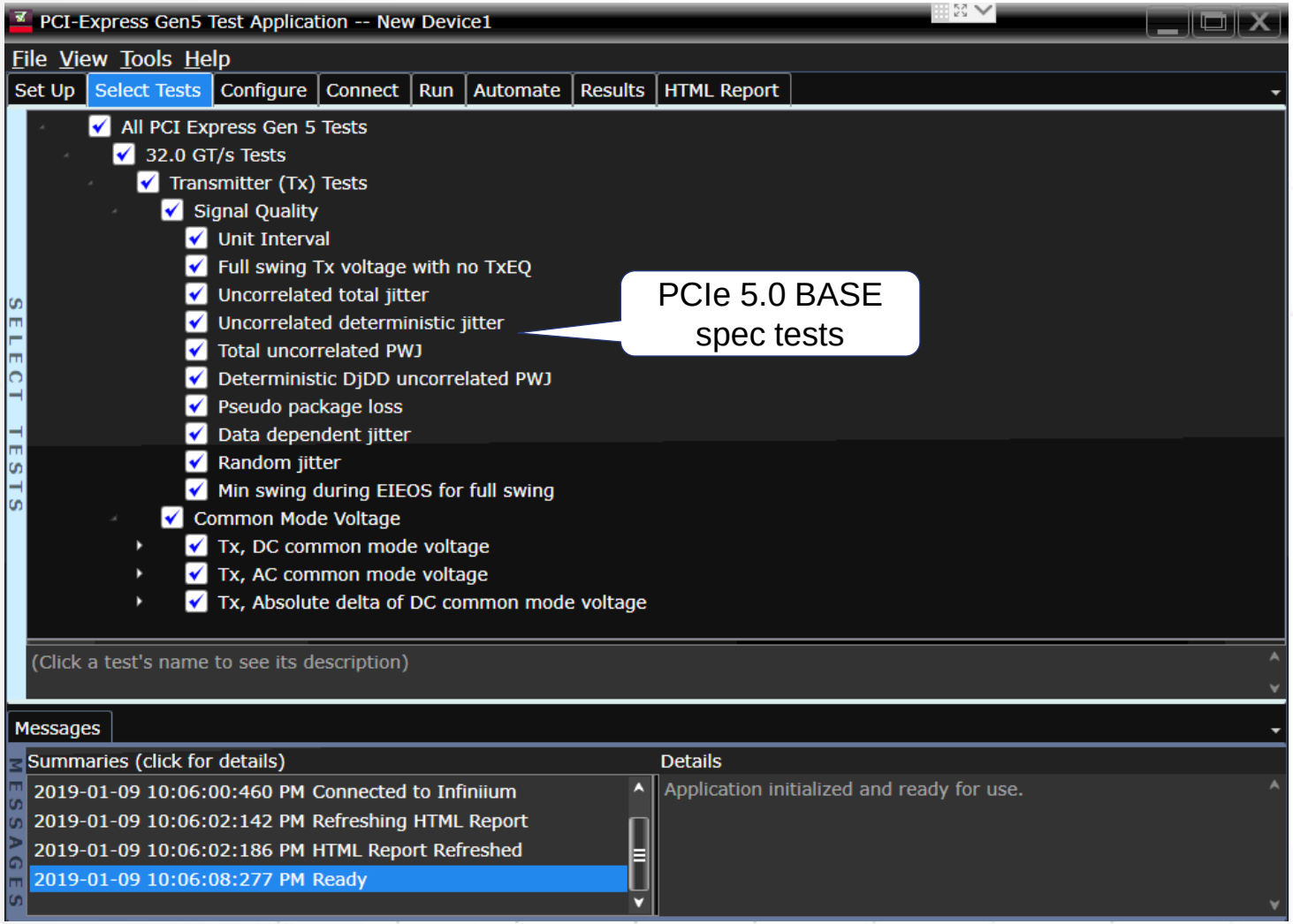
D9050PCIC New Features

MASTER YOUR BEST DESIGN

- Supports PCIe 5.0 BASE TX testing at 32 GT/s as well as 2.5G, 5G, 8G and 16GT/s (v0.9 BASE)
- Supports PCIe 5.0 reference clock tests (2.5G, 5G, 8G, 16G)
- Will support CEM tests for endpoints and root complexes (2.5G, 5G, 8G, 16G, 32G).
- Integrated De-embedding of break-out channel with optional InfiniiSim
- Automated DUT control using an 81150/60A pulse generator ARB.
- Enhanced switch matrix supporting arbitrary lane mapping
- Minimum oscilloscope BW: 50 GHz

Keysight D9050PCIC PCIe 5 (Gen5) TX Test Application

5.0 BASE SPEC TESTS



Test Report

Overall Result: PASS

Test Configuration Details	
Device Description	
Data Channel +	ChannelR-1
Data Channel -	ChannelR-3
Device Name	New Device1
Test Session Details	
Infiniium SW Version	06.30.00701
Infiniium Model Number	DSAZ634A
Infiniium Serial Number	MY57220110
Application SW Version	0.99.9029.0
Debug Mode Used	No
Compliance Limits	PCI-Express Gen5 Test Application (official)
Last Test Date	2019-01-12 22:03:19 UTC -06:00

PCIe 4.0 Dual Port Testing

EXCERPTS FROM PCIE 4.0 TEST SPEC V1.0

Results of the Board Election

PCI SIG

- 2019-2020 PCI-SIG Board of Directors
  - Gord Caruk — AMD
  - Dong Wei — arm
  - Greg Casey — DELL
  - Al Yanes — IBM
  - Debendra Das Sharma — intel
  - Rick Eads — KEYSIGHT TECHNOLOGIES
  - Michael Diamond — NVIDIA
  - Rick Wietfeldt — Qualcomm
  - Richard Solomon — SYNOPSYS Silicon to Software

PCI Express Specifications and Scope

SELECT THE SPECIFICATIONS THAT RELATE TO YOUR SPECIFIC NEED

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Phy Test Specification
- Defines compliance tests of CEM spec in detail

PCIe 4.0 Test Spec
Released Aug 2 at v1.0

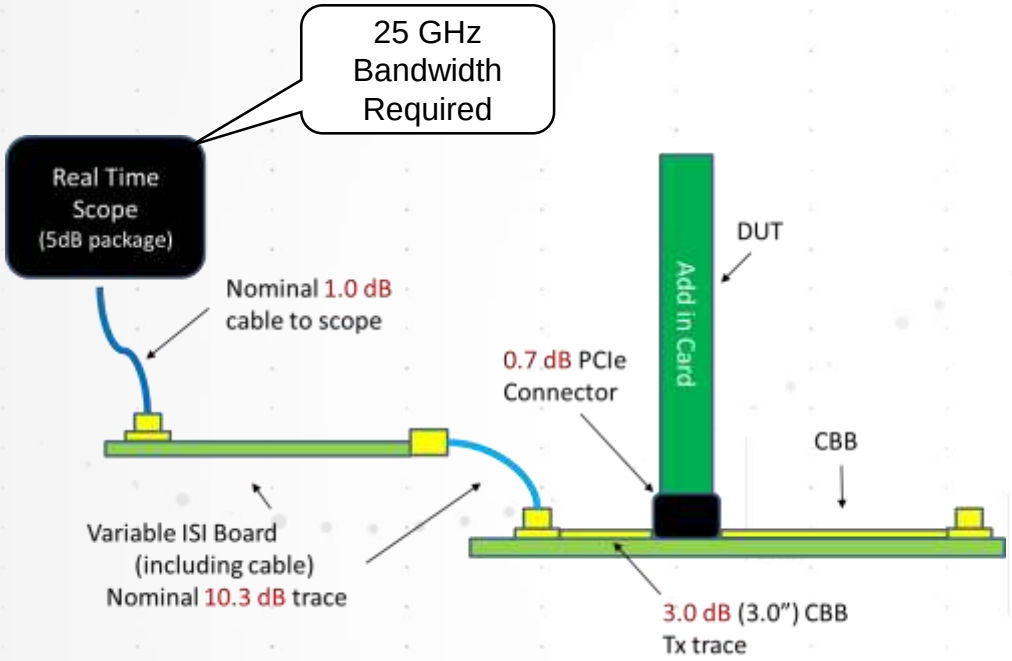
PCIe 4.0 Test Spec

PCIE 4.0 OFFICIAL INTEGRATORS LIST NOW OPEN

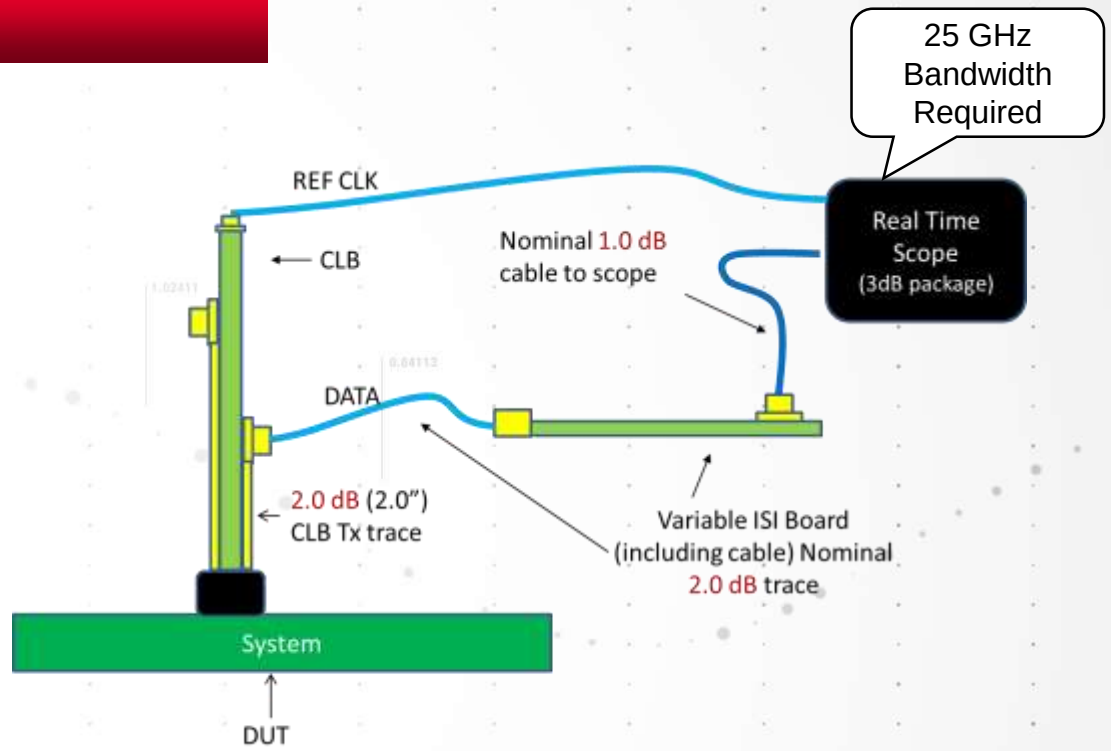
- PCIe 4.0 Test Spec v1.0 now approved
  - Some typos and minor corrections still linger
- Phy layer integrators list required testing:
  - System Board (16G)
    - TX signal quality (Preset tests, signal quality via dual port method)
    - RX: LinkEQ Response Test.
    - RX Link Equalization test
  - Add-in card (16G)
    - TX Signal quality (Preset tests, signal quality)
    - TX PLL
    - TX Pulse width jitter
    - RX: Initial TX EQ test
    - RX: LinkEQ Response Test.
    - RX Link Equalization test

PCIE 4.0 CEM Fixture Setup

PHY TX MEASUREMENTS



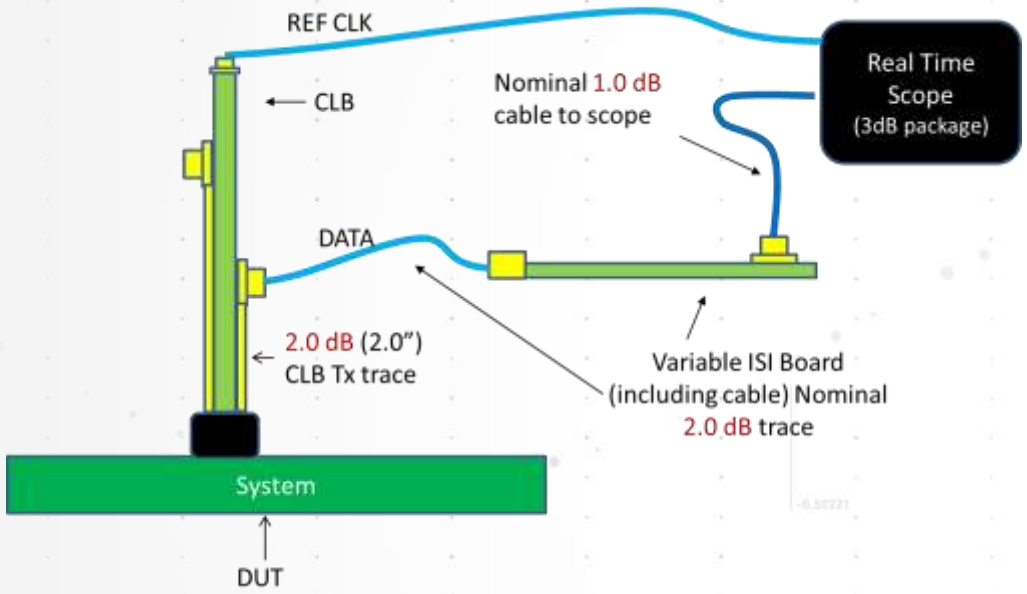
Add-in Card (end point)



System Board (root port)

PCIE 4.0 CEM Motherboard Tests

DUAL PORT TESTING IS THE REQUIRED METHOD



System Board (root port)

Appendix D. Alternate Method of System TX Signal Quality Test at 16GT/s

An alternate method of performing 16GT/s System Signal Quality test is provided in this note. The data and 100 MHz reference clock can be captured and post-processed separately. The data will be processed with SigTest using the 16GT/s Add-in Card Signal Quality template file (PCIe_4_16G_CEM.dat). The pass/fail limits for Eye Width at 1E-12 and Eye Height at 1E-12 will remain unchanged for 16 GT/s System Signal Quality Test. The reference clock will be post-processed with a separate clock tool to ensure the Random Jitter is less than or equal to 0.7 ps RMS as defined in the *PCI Express Base Specification*.

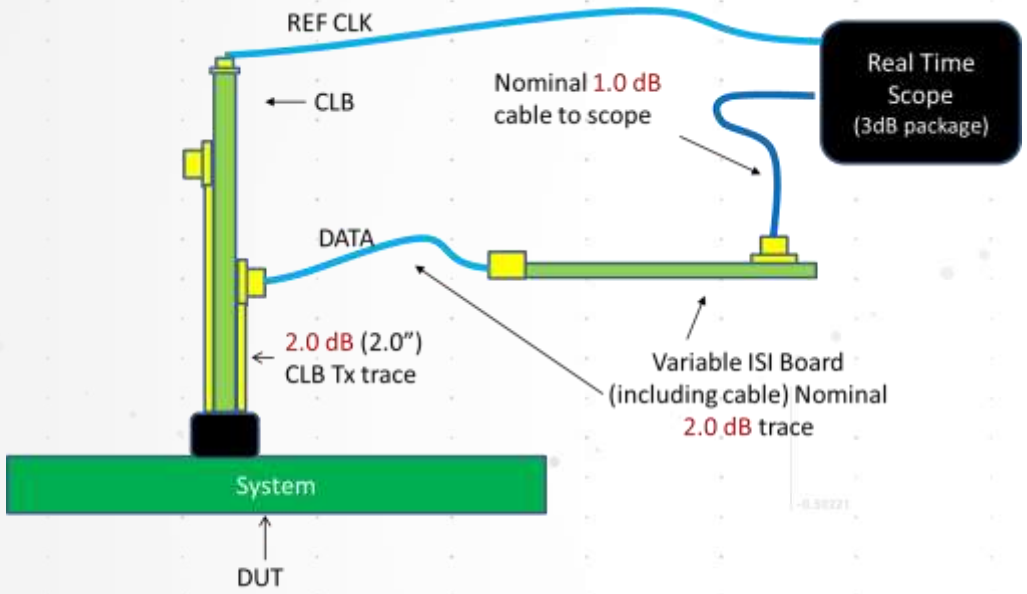
The signal quality test described in Section 2.7.5 is the required test method for System Tx Signal Quality testing at 16 GT/s. This alternate method is only to be used when the signal quality test described in Section 2.7.5 fails.

2.7.5 System Board Transmitter Electrical Compliance Test for 16.0 GT/s

1. Connect the Tx lane under test …
2. Connect the Reference Clock (REF CLK) on the CLB to a high-speed oscilloscope …
3. …push the compliance toggle button on the CLB until the correct Tx EQ is selected…
4. Measure transmitted clock and data waveforms simultaneously with a high-speed oscilloscope or equivalent data capture instrument with the maximum bandwidth set to 25GHz

PCIE 4.0 CEM Motherboard Tests

WHY HAVE TWO METHODS?



System Board (root port)

- Dual Port testing was always the POR for PCIe 4.0
- Appendix D was added as a contingency.
  - Initially Sigtest showed issues if max SSC was enabled.
  - New Intel developer resolved the Sigtest SSC issue with a novel approach.
  - All System Boards tested at WS#110 were tested using the dual port approach.
- Dual Port uses both clock and data and represents the AIC view of root port signal quality.
- System board vendors can trade off ref clock jitter for better TX jitter and still be compliant.

PCIe 5.0 RX Test Tools

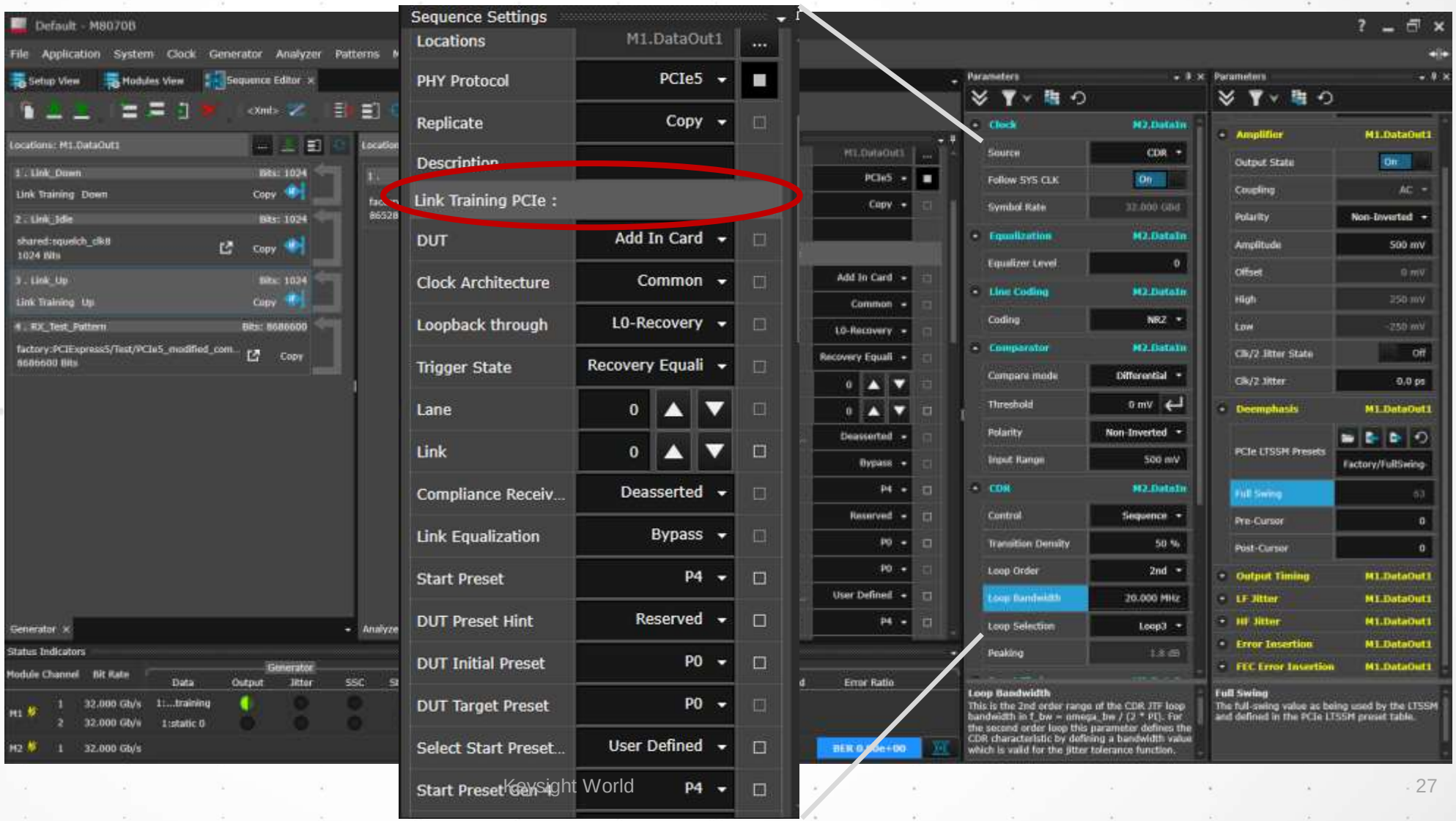
M8040A 64 GBaud High-Performance BERT

Master your next generation PCIe design

- Highly integrated for simplified RX test setup for 400G and PCIe5
- Upgrade paths towards 32 Gbaud PAM4 and 64 Gb/S NRZ
- Most complete solution with test automation
- PCI-SIG gold-suite approved vendor

New: PCI Express Interactive Link Training 8/16/32 GT/s

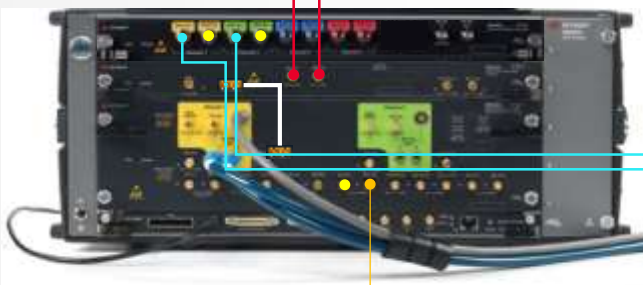
M8046A-0S1 INTERACTIVE LINK TRAINING FOR PCIE 32G/16G/8G



PCIe 32G/16G/8G RX Test Setup

SETUP USING M8040A 64G HIGH-PERFORMANCE BERT

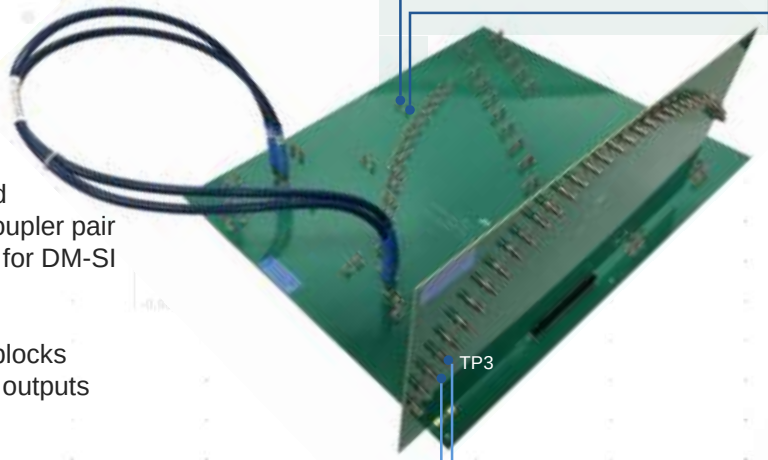
New interference source module M8054A for DM-SI & CM-SI

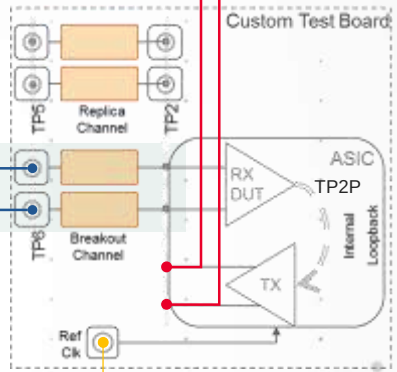


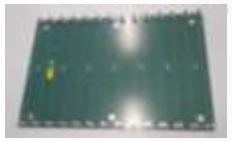
M8046A with integrated CDR option 0A4 / 0A5 and equalization with new option 0S2 SKP OS Filtering PCIe 8G/16G/32G and CCIX 20G/25G and option 0S1 Interactive Link Training PCIe 8G/16G/32G

New matched broadband coupler pair M8045A-803 for DM-SI & CM-SI

N9398F DC blocks used coupler outputs





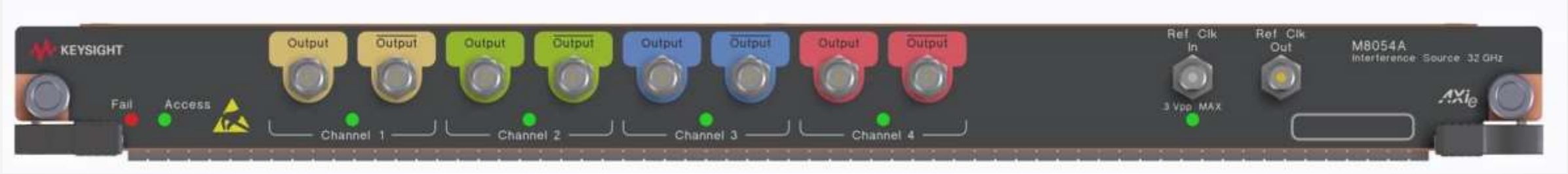


Substitute PCIe 5 base channel boards by new ISI traces M8049A-003 & M8049A-001

M8049A-001 offers traces from approximately 1.5 dB to 3.5 dB in 0.5 dB steps.

M8049A-003 offers tr aces from 10 dB to 22 dB in 2 dB steps, IL measured @ 16 GHz

New: Interference Source M8054A with Coupler

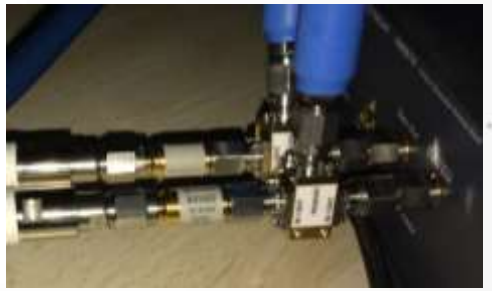


M8054A interference source module

Emulate level interference for RX stress test

- Designed specifically for M8070A or other dedicated Keysight RX test automation SW
- BW 32 GHz
- 4 ch outputs
- Drives combined Random Interference (RI) and Sinusoidal Interference (SI)
- Common mode and differential mode
- Near-end and far-end channel injection possible by use of couplers
- Specs similar to today‘s M8196A when used as RI/SI source in M8070A
- Control via M8070A/B

Interference source



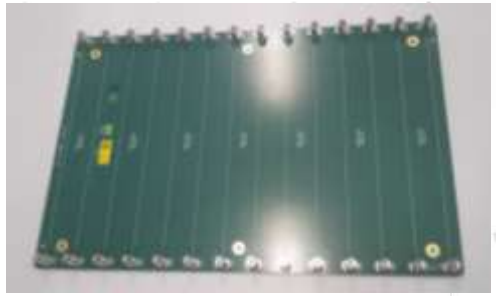
PG

M8045A-803 coupler

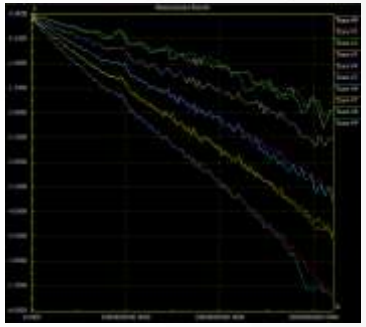
ISI Channels for High-Speed Receiver Test

new

M8049A



	M8049A-001	M8049A-002	M8049A-003
Description	ISI channel board with 5 traces from 1.4 to 5.5 inches	ISI channel board with 9 traces from 0.8 to 8.0 inches	ISI channel board with 7 traces from 9.1 to 22.3 inches
Traces dB	1.5, 2, 2.5, 3, 3.5 (estimated)	2.5, 3, 3.5, 4, 5, 6, 7, 8, 9 (estimated)	10, 12, 14, 16, 18, 20, 22 (estimated)



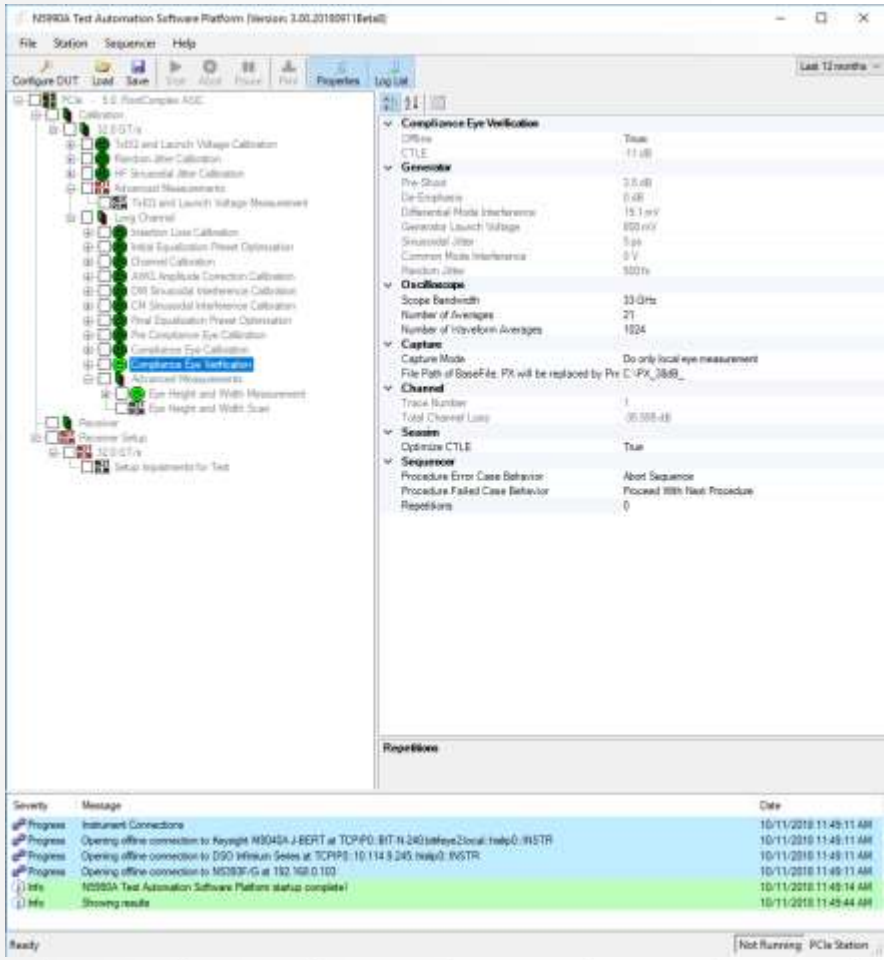
Preliminary S21 (Sep 2018)

Key features of ISI channel boards

- Emulate channel loss with fine granularity -> 3 separately orderable & cascadable boards
- Lower loss needed for 32 Gbaud signals
  Applications: PCIe 5, CCIX, IEEE 802.3, OIF-CEI-56G, Fibre Channel, other >20 Gbd applications
- Recommended cables for cascading: M8046A-802 (1 m matched cable pair 2.4 mm)

N5991PxxA

RX TEST AUTOMATION - CALIBRATION



- Guided and automated stress signal calibration for PCI Express 5.0 32 GT/s*)
- “Setup Impairment for Test” function sets the M8040A/M8020A system to user defined impairments. This function supports generator only systems as well as full RX test systems
- TxEQ matrix scan, JTOL test, sensitivity test and RX test
- Contact Keysight representative for latest release timing.


Product Number: PCIe PCIe Station Unknown User 04/10/2018 11:37:19

L0_Cal_32GTps_CompEye

for PCIe 5.0 RootComplex ASIC

BERT System	Keysight M8040A J-BERT, M8070A, SN: DE56C00245
Generator Channel Channel	M1:DataOut1
Offline	False
Scope Bandwidth	33 GHz
Number of Averages	21
Number of Waveform Averages	1024
Optimize CTLE	True
Trace Number	1
Total Channel Loss	-38.595 dB
Pre-Shoot	3.5 dB
De-Emphasis	0 dB
Max Number of Search Steps	7
Use nominal EH/EW results from Pre Comp Cal	True
Sinusoidal Jitter Frequency	100 MHz
Common Mode Interference	0 V
Random Jitter	800 fs
Transfer Function File for Package Model on Scope	PCIe5RxPackageModel_RootComplex.tf4
Scope Connection for Calibration	RealEdge

DMSI [mV]	RJ [ps]	Vdiff [mV]	Eye Height [mV]	Eye Width [ps]
19.1	6.00	800	14.22	9.61

PCI Express® 5.0 – Keysight Total Solution

Physical layer – interconnect design

ADS design software

86100D DCA-X/TDR

N5227B PNA w/ PLTS

Verify PCIe 5.0 compliant channels
Verify return loss compliance
Capture break-out channel S-params

Physical layer-transmitter test

UXR-Series, Z-Series real-time oscilloscopes

D9050PCIC PCI Express 5.0 TXeElectrical compliance software

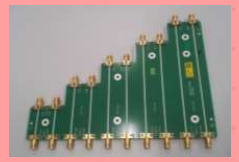
86100CU-400 PLL and jitter spectrum measurement SW

DSA UXR-Series & Z-Series real-time oscilloscopes

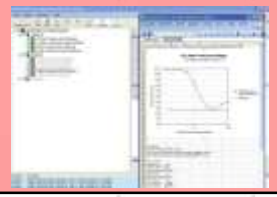
Physical layer-receiver test

M8046A J-BERT high performance BERT w/ integrated CDR + M80454A interference source

M8049A-1 substitute PCIe 5 BASE channel board



N5991PB5A
PCIe 5.0 32GT/s RX test software



Automated RX test software
- Accurate, efficient
- Comprehensive RX testing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