# Making Accurate Signal Integrity Measurements Using Frequency Domain Techniques


| | |
|---|---|
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KEYSIGHT TECHNOLOGIES

# How to Make Accurate Signal Integrity Measurements

## Measurement

**Prepare instrument for measurement**
- Calibration
- Fixture removal

**Acquire channel data**
- Multi-port S-parameter measurement

**Analyze channel performance**
- Single-ended vs. differential
- Eye diagrams (NRZ, PAM4),
- COM

## Demo

**Conclusion**
- What next?
- Future trends
- Resources

**Live Demo**
- Design case study
- Complete channel analysis
- TDR, PAM4 eye diagram, etc

**Q&A**

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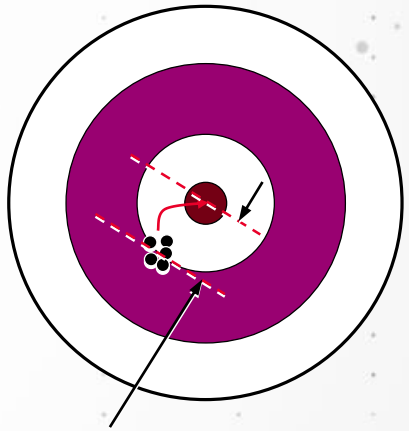
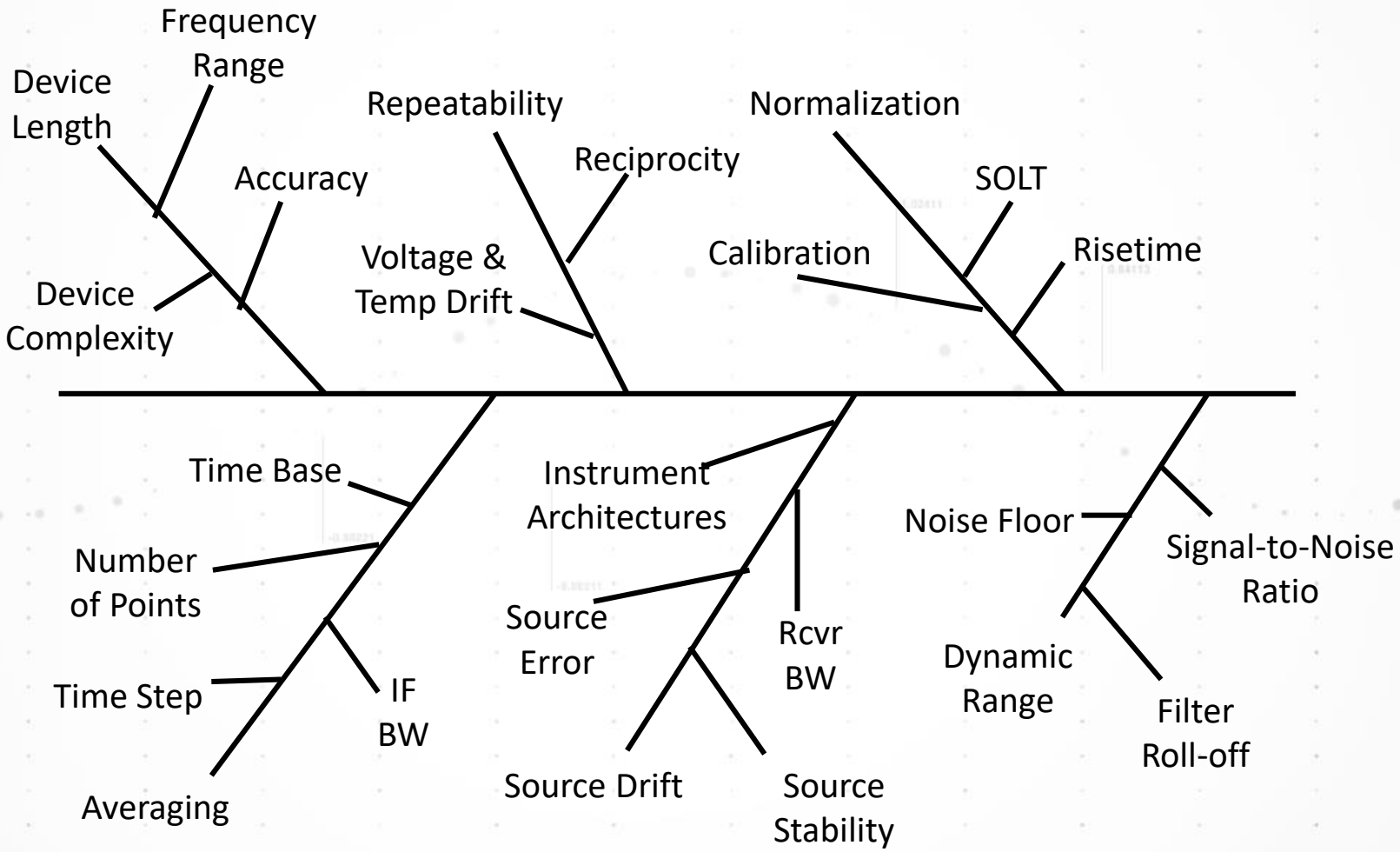
# The Need For Calibration

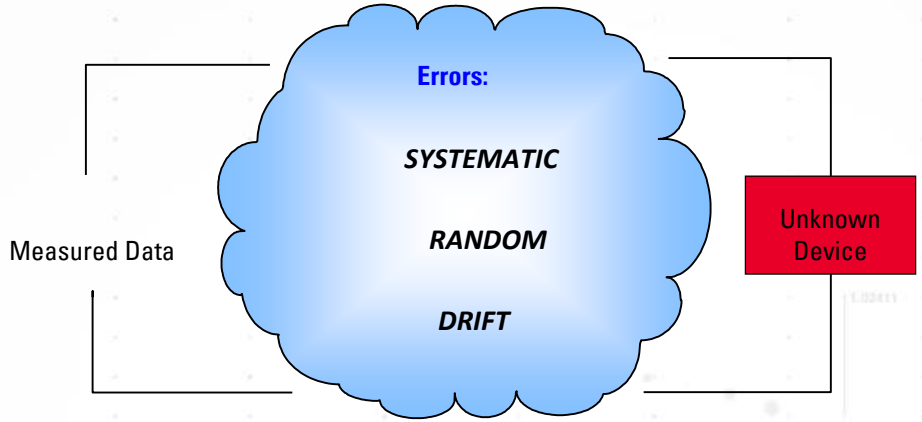
- **Why do we have to calibrate?**
  - It is impossible to make perfect hardware (couplers, switches, etc.)
  - Even with highest quality components, some error exists
- **How do we get accuracy?**
  - With vector-error-corrected calibration
  - Not the same as the yearly instrument calibration
- **What does calibration do for us?**
  - Removes the largest contributor to measurement uncertainty: systematic errors
  - Provides best picture of true performance of DUT



# Appreciating the Complexity of it All



# Measurement Error Modeling





## *Systematic errors*

- Due to **imperfections** in the analyzer and test setup
- Assumed to be **time invariant** (predictable)
- Generally, are largest sources or error

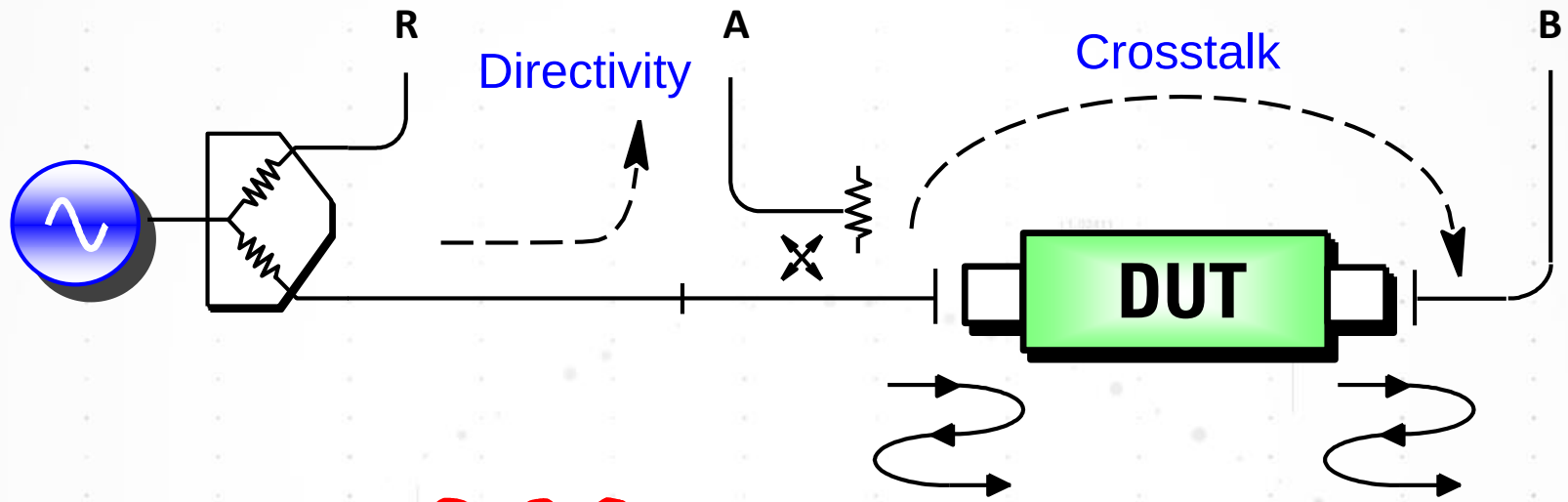
## *Random errors*

- **Vary** with time in random fashion (unpredictable)
- Main contributors: instrument **noise,** switch and connector **repeatability**


## *Drift errors*

- Due to system performance changing ***after*** a calibration has been done
- Primarily caused by **temperature variation and cabling**

# Systematic Measurement Errors

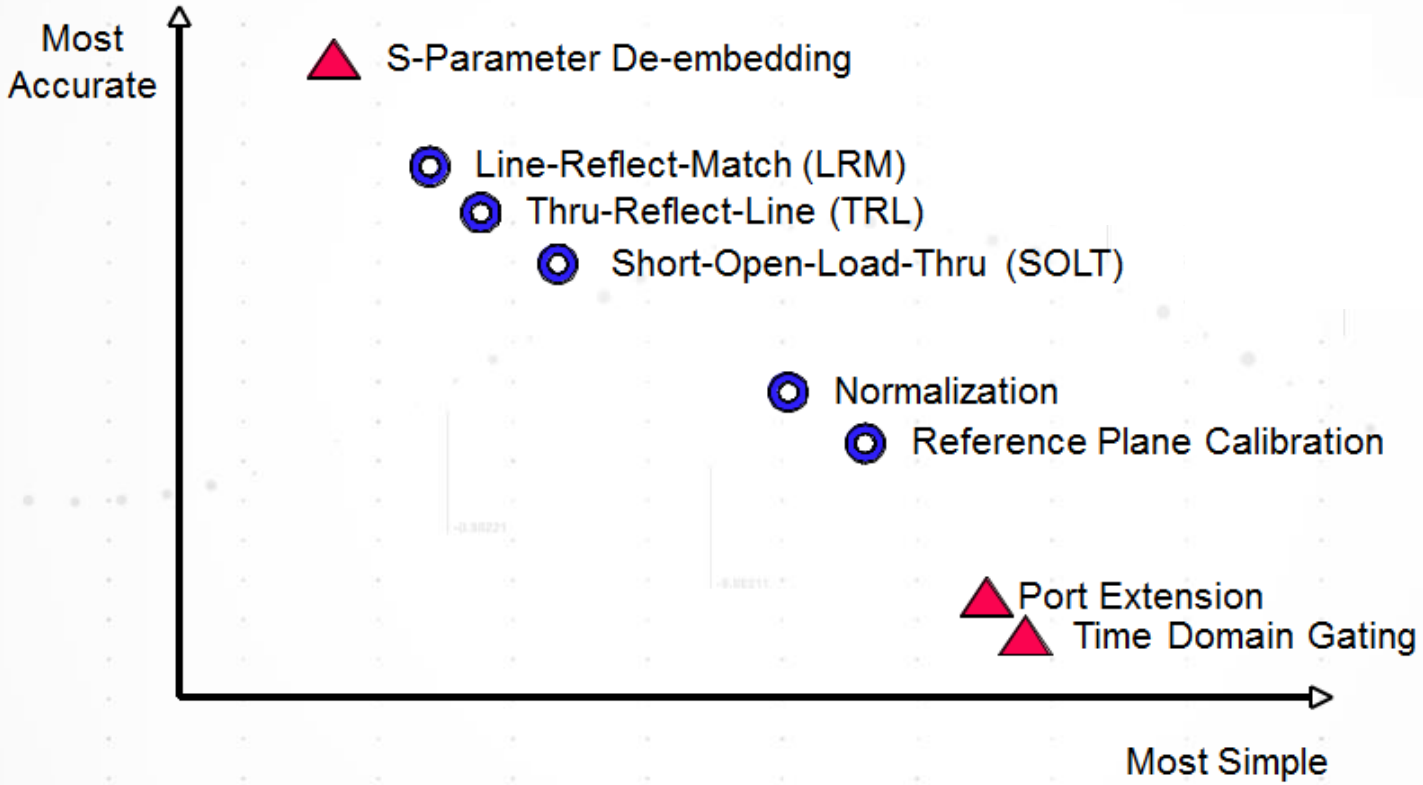



*Frequency response*

- Reflection tracking (A/R)
- Transmission tracking (B/R)

***Six forward and six reverse error terms yields 12 error terms for two-port devices***

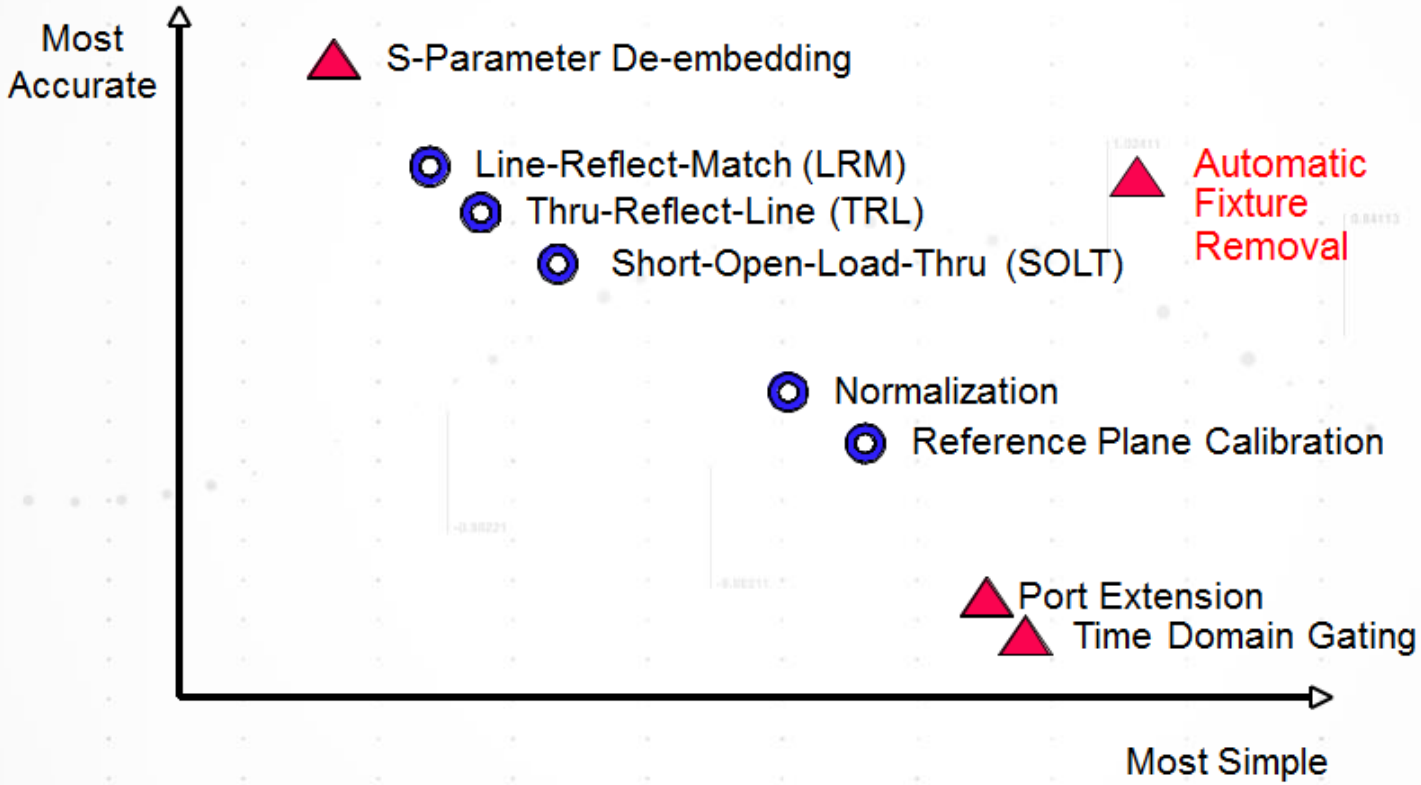
# Error Correction Techniques




= Pre-measurement error correction

= Post-measurement error correction

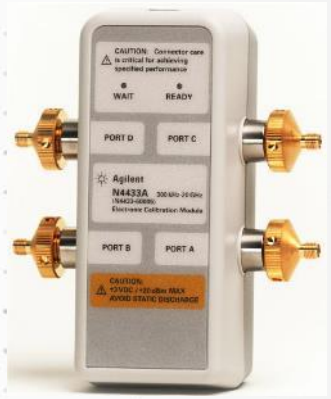
# Error Correction Techniques



# SOLT Calibration: Mechanical & E-Cal Module

Short
Open
Load
Through

| | Advantages | Disadvantages |
|---|---|---|
| **Electronic Calibration Module** | Easy, prevents cable/connector wear and SAVES TIME | N/A |
| **Mechanical Calibration Kit** | More accurate | Slow and tedious especially for multiport applications |



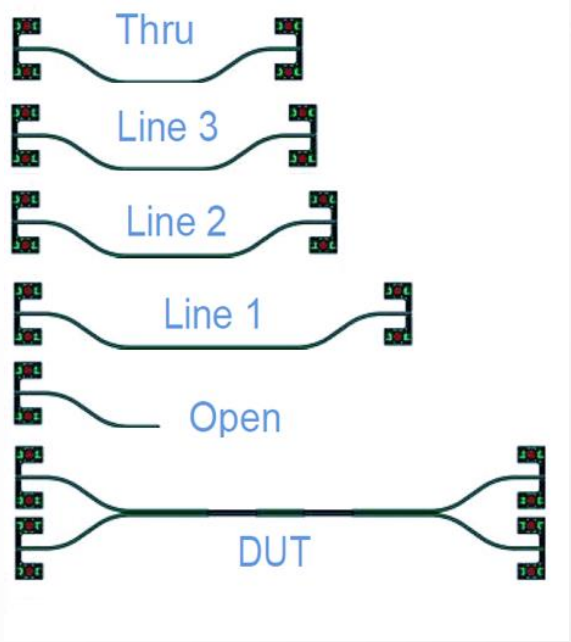


# Thru-Reflect-Line (TRL) Calibration

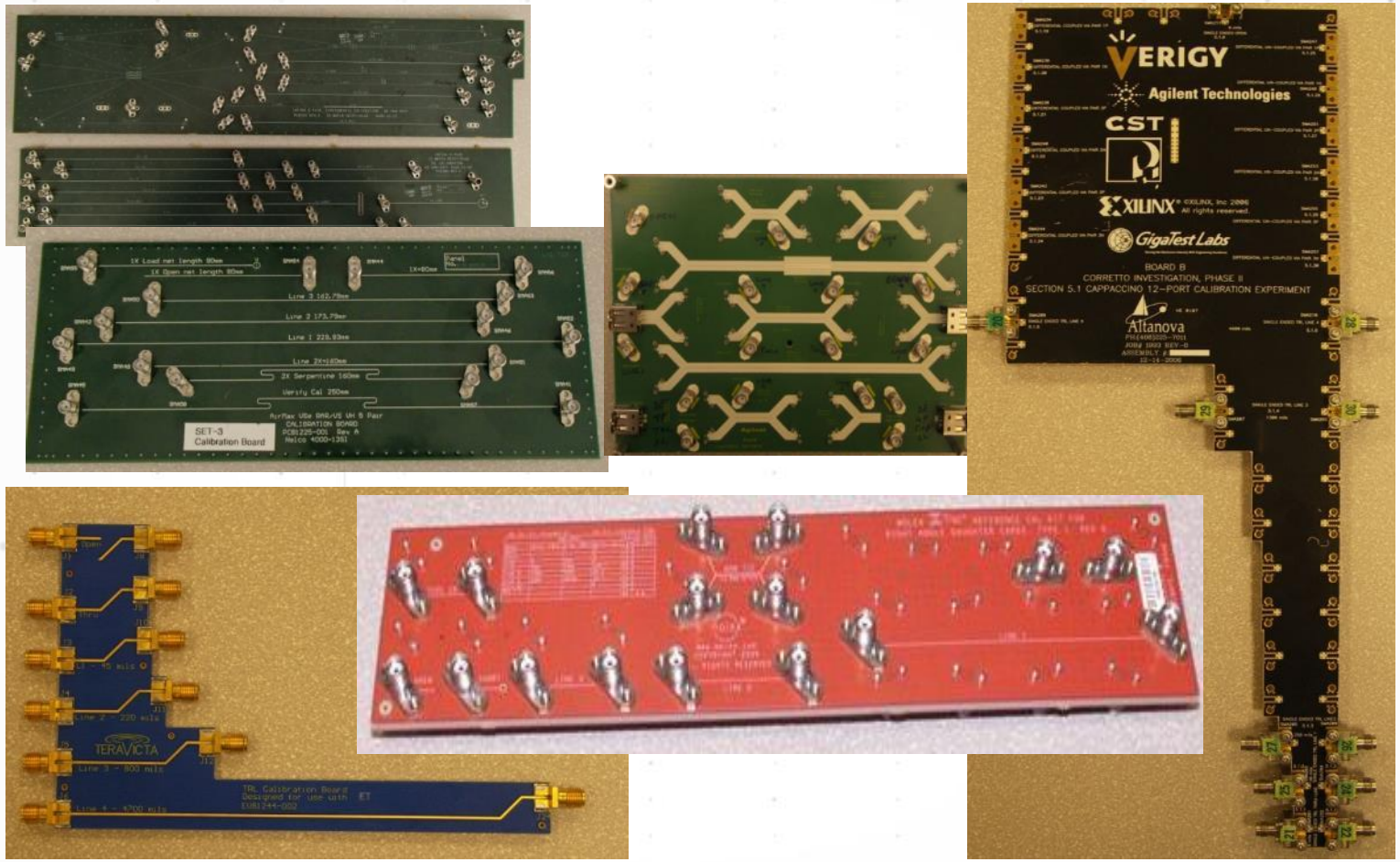
We know about Short-Open-Load-Thru (SOLT) calibration... What is TRL?

- Good for non-coaxial environments (PCBs, fixtures, wafer probing)
- Characterizes same 12 systematic errors as the more common SOLT cal
- Other variations: Line-Reflect-Match (LRM), Thru-Reflect-Match (TRM), plus many others
- User must fabricate the calibration standards

TRL was developed for **non-coaxial microwave** measurements



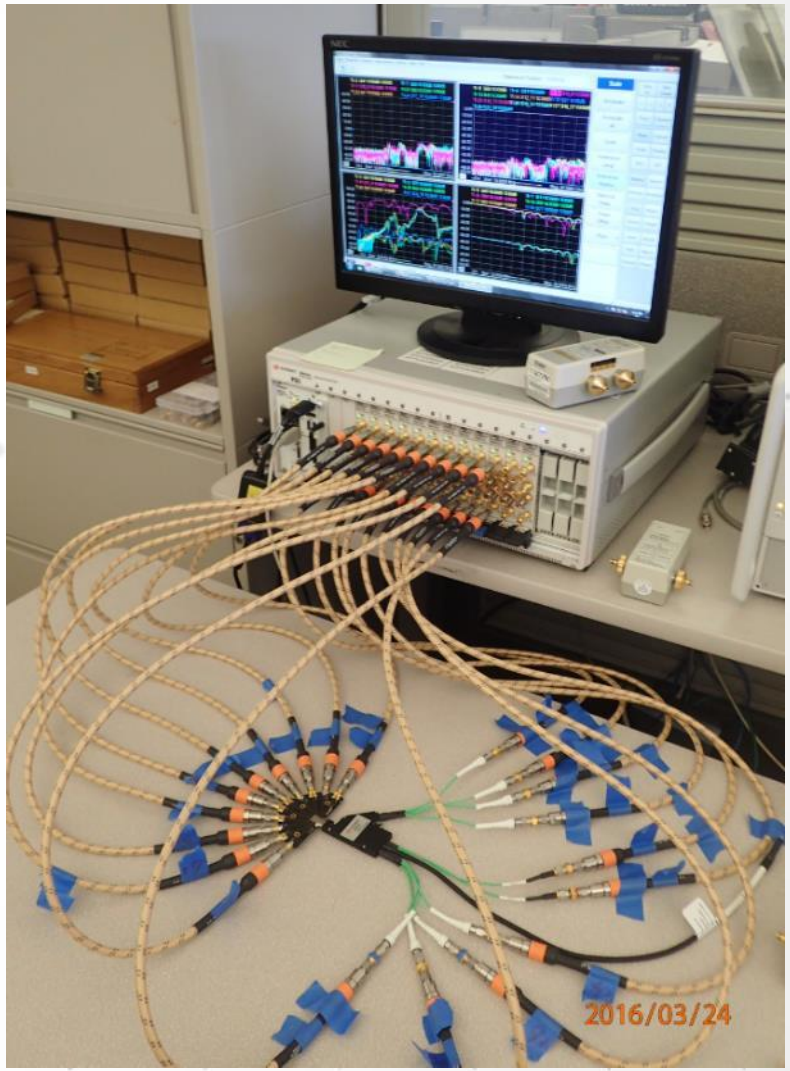
# PCB TRL Calibration Kits




A good TRL cal kit is difficult to design and fabricate due to launch repeatability, PCB impedance variations, and typical PCB manufacturing tolerances

# Taking Accuracy to the Next Level During Calibration

- **What else can be done?**
  - Make sure that the Ecal has an up-to-date factory calibration
  - Clean all the coaxial connectors as described in the Connector Care App Note
- **How important are the test cables?**
  - Extremely. Would you put bias ply tires on a Ferrari? Don't try to save money on test cables
  - Any movement of test cable between calibration and measurement shift phase of measurement. Don't exceed the recommended bend radius.
  - Tape down the test cables. Learn from the lab metrologists.



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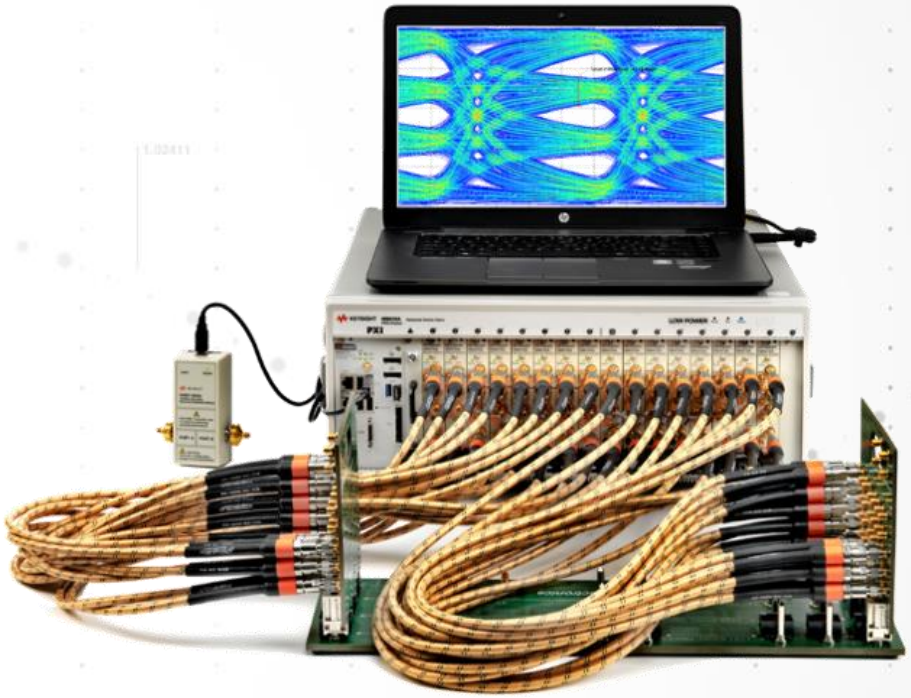
**Q&A**

# A Day in the Life of an SI Engineer…what now??

- Determine VNA testing requirements
  - Frequency Range?
  - Number of Ports?
- Active or Passive device test?
- Probing system or fixturing?
- Accessories and specialist software tools? (aka…here are some powerful PLTS features that allow you to play with data…)

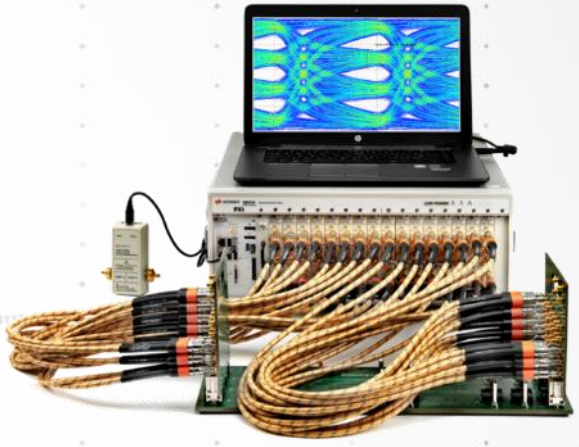
# Frequency Range and Number of Ports Needed?

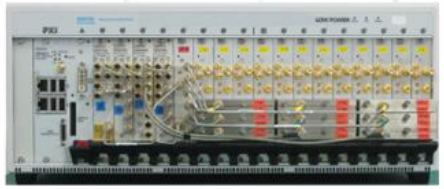
4-port 120GHz PNA+PLTS System



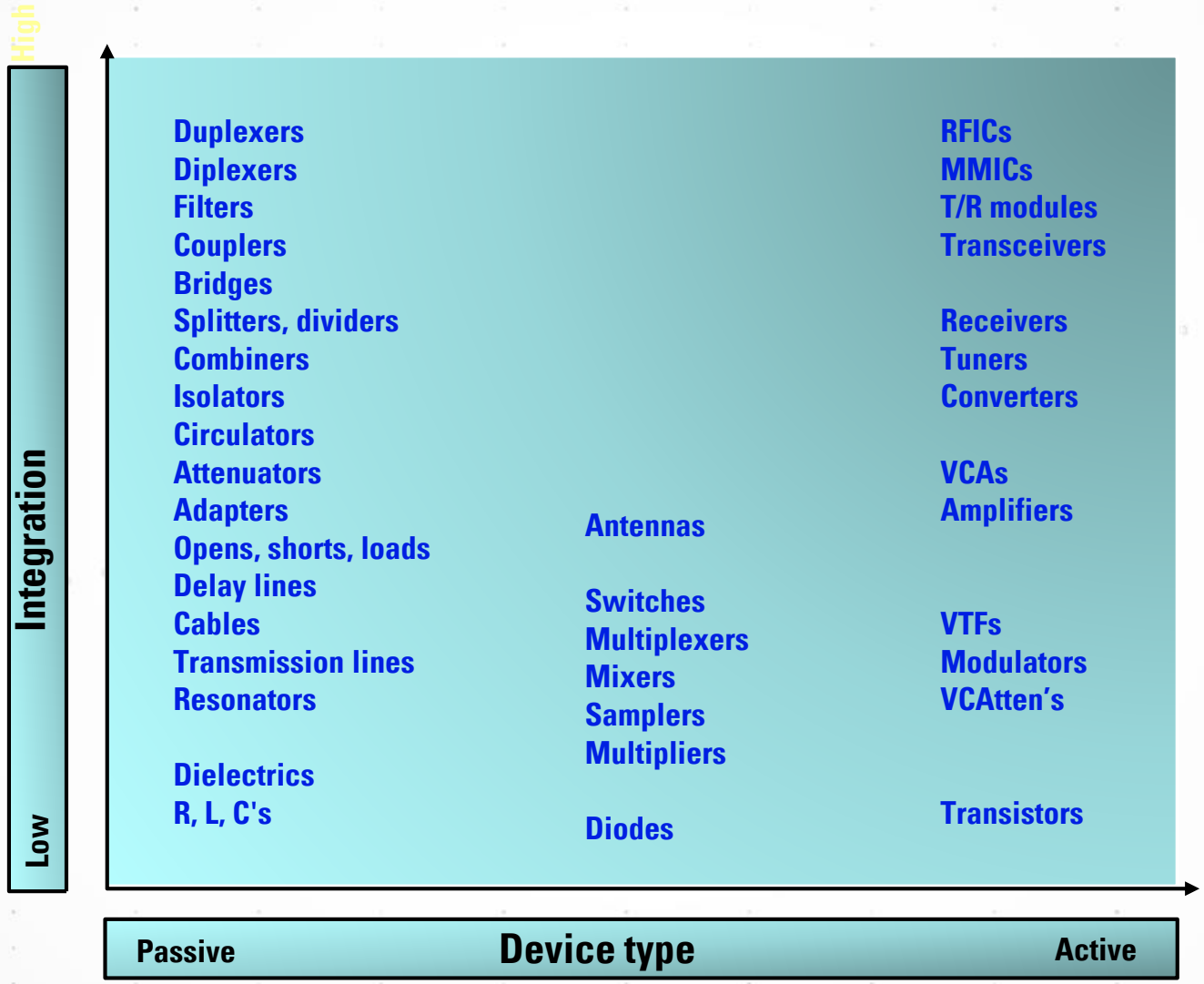
32-port 26.5GHz PXI-based PNA+PLTS System

# Frequency Range and Number of Ports Needed?





# Active or Passive Device Test?



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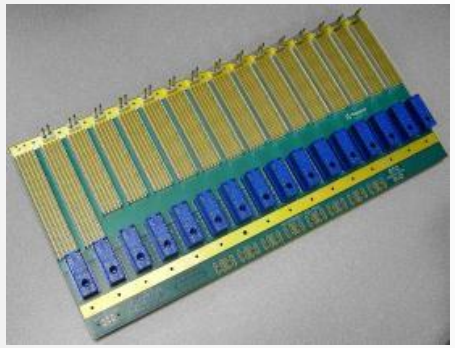
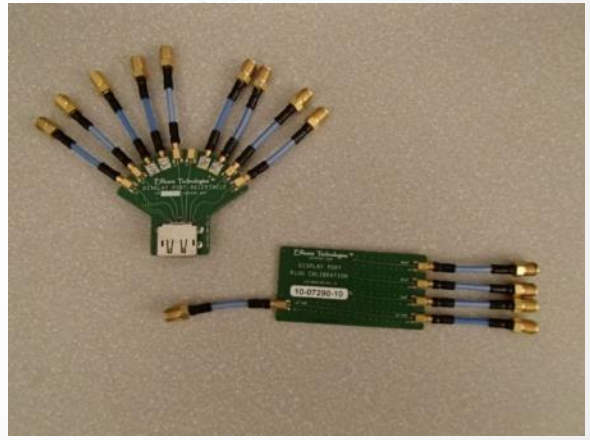
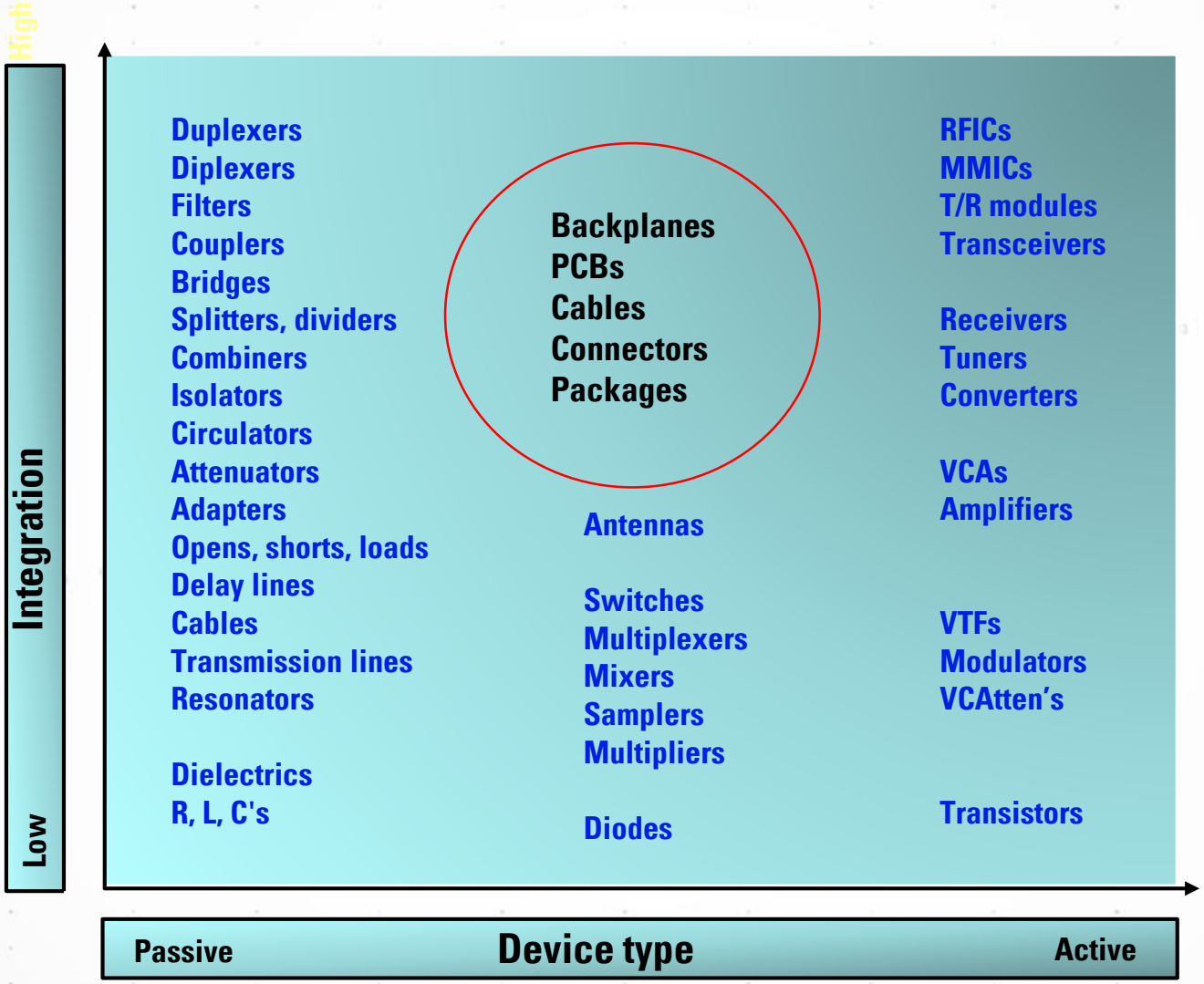
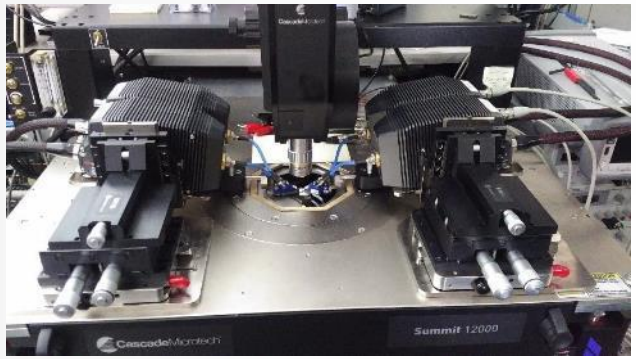
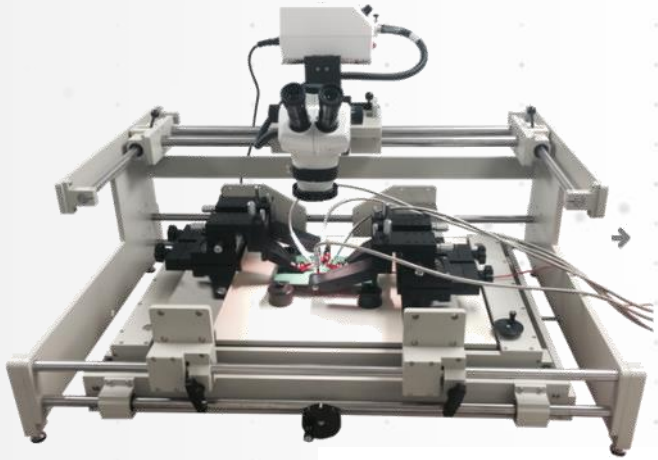






# Probing or Fixturing?



Probing

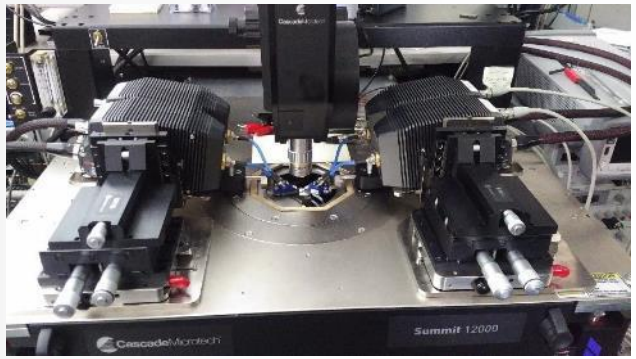
Advantage

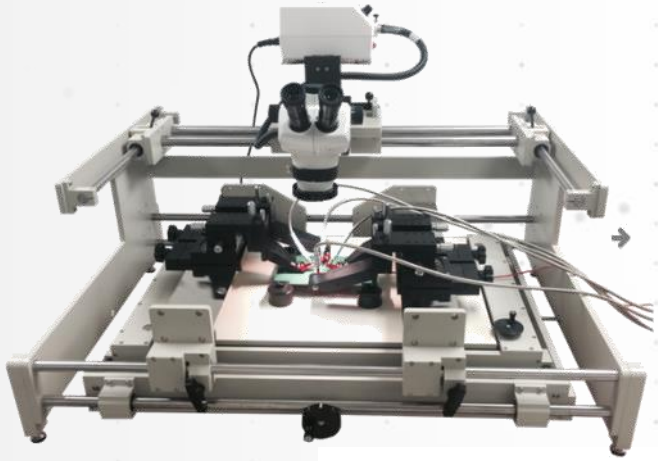
- Flexibility

Disadvantage

- Expensive
- Need ISS calibration substrate for probe tip ref plane

# Probing or Fixturing?



## Probing

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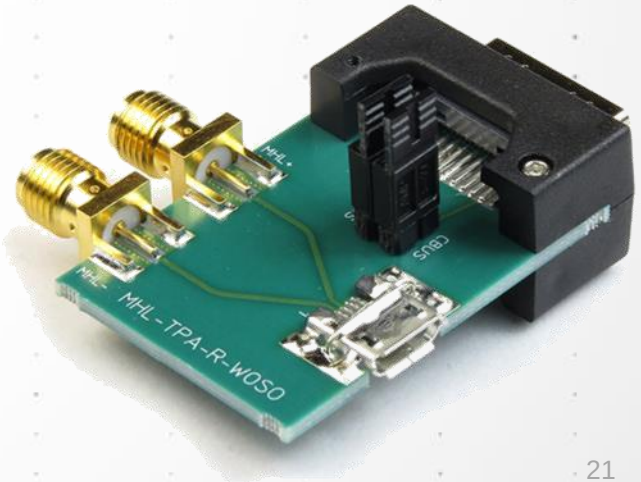
## Fixtures

Advantage

- Easy to Use

Disadvantage

- Each application requires different fixture
- Not electrically transparent, they have mismatch, loss and delay that must be characterized and removed from the DUT measurement (de-embed)



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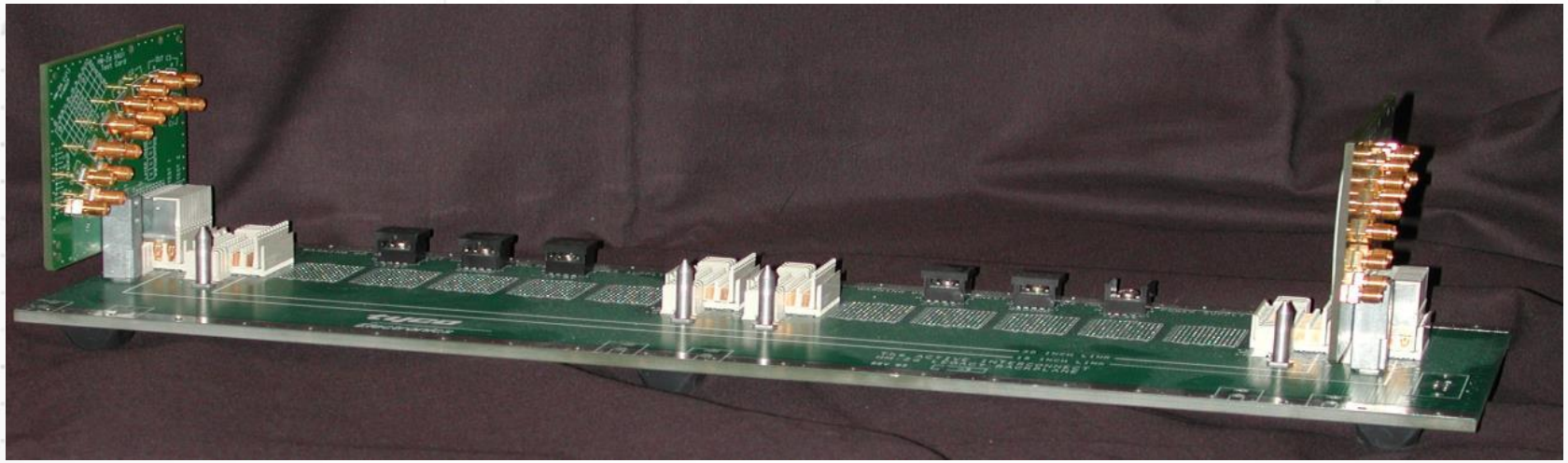
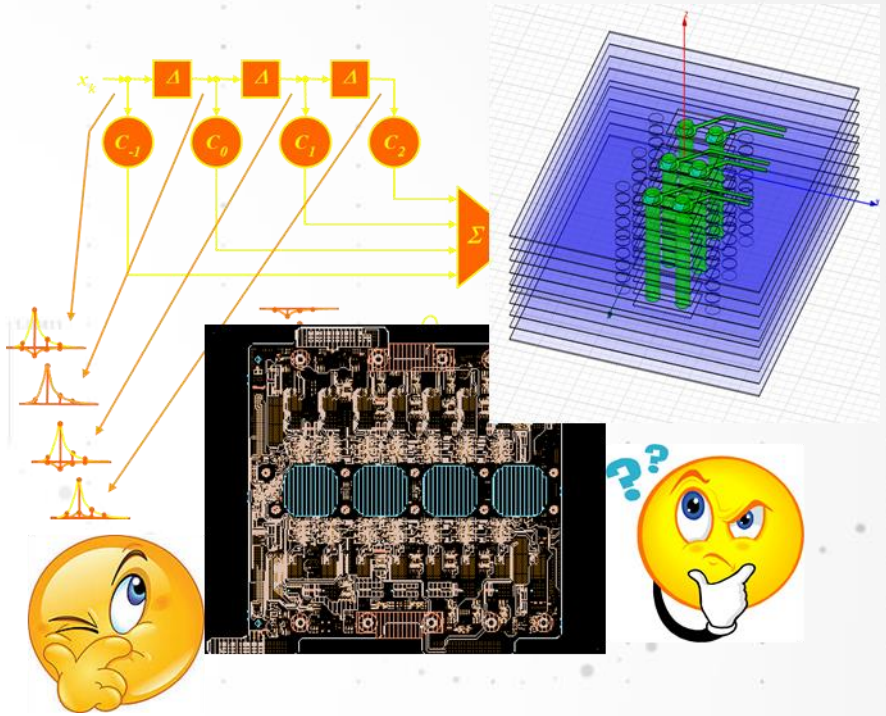
# Analyze Channel Performance

- Traditional analysis: IL, RL, Zo, NEXT,FEXT, Eye diagrams, etc
- Emerging standards proposing new test methods
- Complexity increases, software tools can minimize the learning curve
- New Figures of Merit are creating measurement challenges
  - PAM4 eye diagram
  - Channel Operating Margin (COM)
  - Effective Return Loss (ERL)



# COM Helps Engineers talk with Engineers



For a SerDes engineer COM is:

- A reference chip capability
- SNR budget of a receiver

For a channel engineer COM is:

- A budget between insertion loss, return loss, reflections, and crosstalk
- A management tool for trade offs between via stub, material selection, PCB constructions, connector choice.

Courtesy of Richard Mellitz of Samtec

# COM Configuration Spreadsheet

| Table 93A-1 parameters | | | |
|---|---|---|---|
| **Parameter** | **Setting** | **Units** | **Information** |
| f_b | 25.78125 | GBd | |
| f_min | 0.05 | GHz | |
| Delta_f | 0.005 | GHz | |
| C_d | [2.5e-4 2.5e-4] | nF | [TX RX] |
| z_p select | [1 2] | | [test cases to run] |
| z_p (TX) | [12 30] | mm | [test cases] |
| z_p (NEXT) | [12 12] | mm | [test cases] |
| z_p (FEXT) | [12 30] | mm | [test cases] |
| z_p (RX) | [12 30] | mm | [test cases] |
| C_p | [1.8e-4 1.8e-4] | nF | [TX RX] |
| R_0 | 50 | Ohm | |
| R_d | [55 55] | Ohm | [TX RX] |
| f_r | 0.75 | *fb | |
| c(0) | 0.62 | | min |
| c(-1) | [-0.18:0.02:0] | | [min:step:max] |
| c(1) | [-0.38:0.02:0] | | [min:step:max] |
| g_DC | [-12:1:0] | dB | [min:step:max] |
| f_z | 6.4453125 | GHz | |
| f_p1 | 6.4453125 | GHz | |
| f_p2 | 25.78125 | GHz | |
| A_v | 0.4 | V | |
| A_fe | 0.4 | V | |
| A_ne | 0.6 | V | |
| L | 2 | | |
| M | 32 | | |
| N_b | 14 | UI | |
| b_max(1) | 1 | | |
| b_max(2..N_b) | 1 | | |
| sigma_RJ | 0.01 | UI | |
| A_DD | 0.05 | UI | |
| eta_0 | 5.20E-08 | V^2/GHz | |

| I/O control | | |
|---|---|---|
| DIAGNOSTICS | 1 | logical |
| DISPLAY_WINDOW | 1 | logical |
| Display frequency domain | 1 | logical |
| CSV_REPORT | 1 | logical |
| SAVE_FIGURE_to_CSV | 0 | logical |
| RESULT_DIR | .\test_results_C92\ | |
| SAVE_FIGURES | 0 | logical |
| Port Order | [1 3 2 4] | |
| **Receiver testing** | | |
| RX_CALIBRATION | 0 | logical |
| Sigma BBN step | 5.00E-03 | V |
| IDEAL_TX_TERM | 0 | logical |
| T_r | 8.00E-03 | ns |
| **Non standard control options** | | |
| INC_PACKAGE | 1 | logical |
| IDEAL_RX_TERM | 0 | logical |
| INCLUDE_CTLE | 1 | logical |
| INCLUDE_TX_RX_FILTER | 1 | logical |

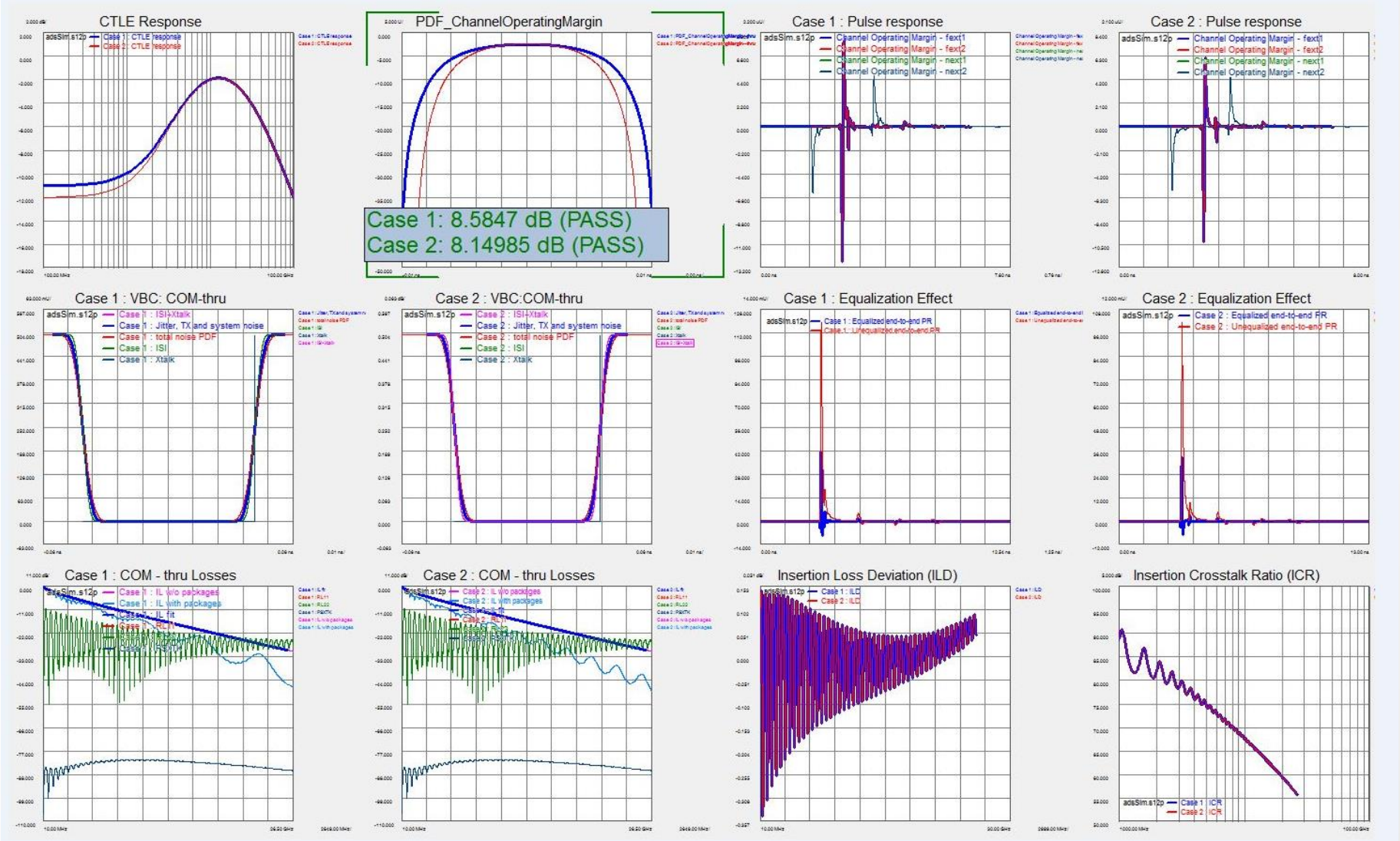
| Table 93A–3 parameters | | |
|---|---|---|
| **Parameter** | **Setting** | **Units** |
| package_tl_gamma0_a1_a2 | [0 1.734e-3 1.455e-4] | |
| package_tl_tau | 6.141E-03 | ns/mm |
| package_Z_c | 78.2 | Ohm |

| Table 92–12 parameters | | |
|---|---|---|
| **Parameter** | **Setting** | |
| board_tl_gamma0_a1_a2 | [0 4.114e-4 2.547e-4] | |
| board_tl_tau | 6.191E-03 | ns/mm |
| board_Z_c | 109.8 | Ohm |
| z_bp (TX) | 151 | mm |
| z_bp (NEXT) | 72 | mm |
| z_bp (FEXT) | 72 | mm |
| z_bp (RX) | 151 | mm |

COM_Settings

# Channel Operating Margin (COM)- How to Measure it?

- Measure passive channel
- Import data into PLTS
- Call MATLAB script
- Publish automatic results

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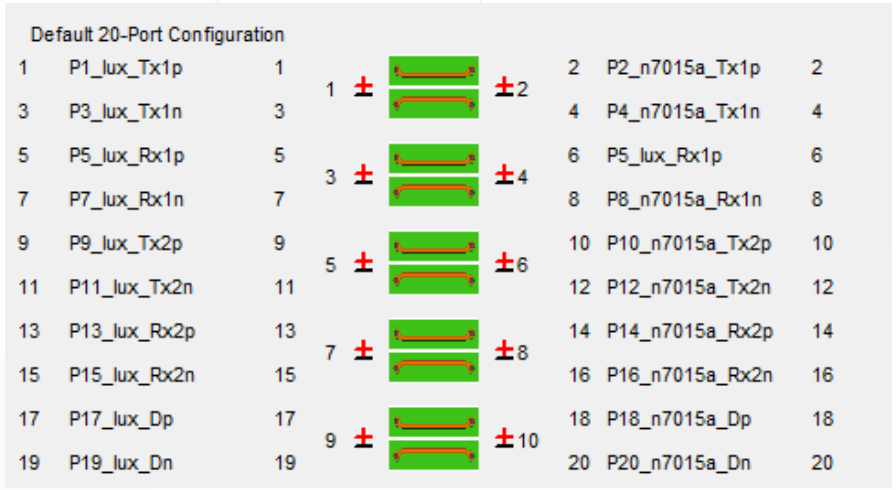
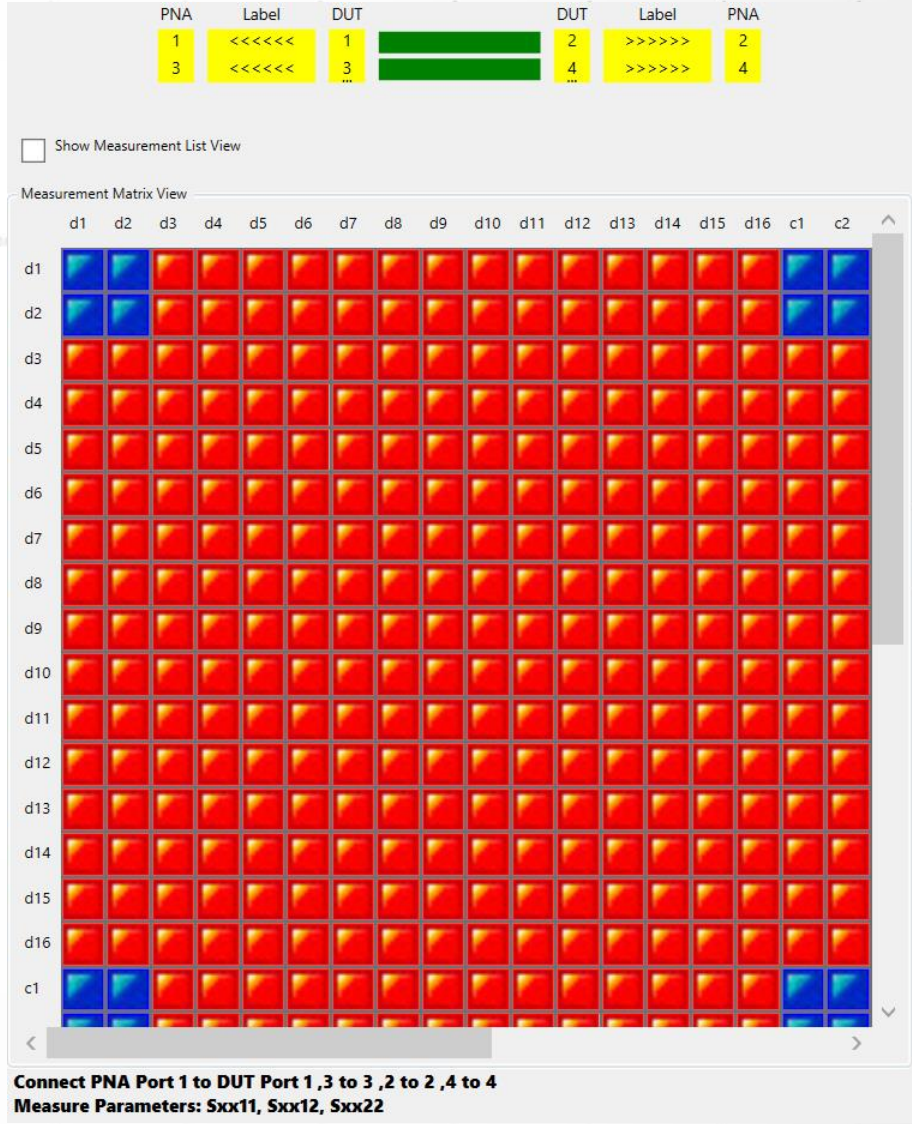
# Multiport s-Parameter Data: How to Manage it?

The Challenge: >12-port VNA Data
Typical Issues: Lost track of port numbering
Crosstalk data is unclear
Solution: Let the tool do the memory work
Scenario: Use N1930B PLTS 2018 software
Calibration
Measurement
Analysis

- Import data into PLTS
- Call MATLAB script
- Publish automatic results



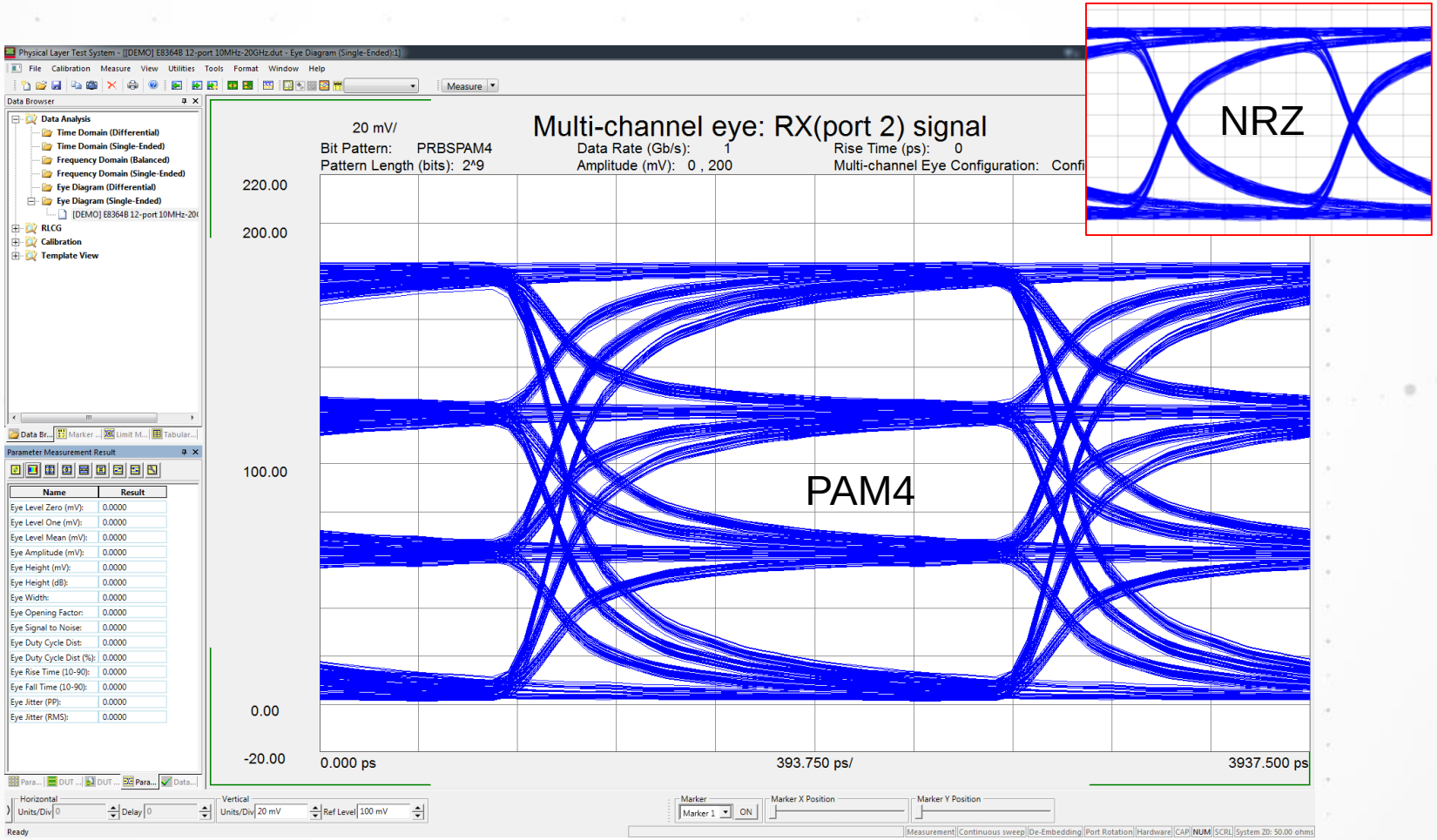

KEYSIGHT TECHNOLOGIES

# Pulse Amplitude Modulation (PAM4) – Why??

- Demand for increased network bandwidth in data centers
- 400G links will be the next step in meeting the need for speed
- Multi-level signaling formats such as Pulse Amplitude Modulation (PAM-N) are technologies that will enable 400G implementation

# Pulse Amplitude Modulation (PAM4) – What is it?

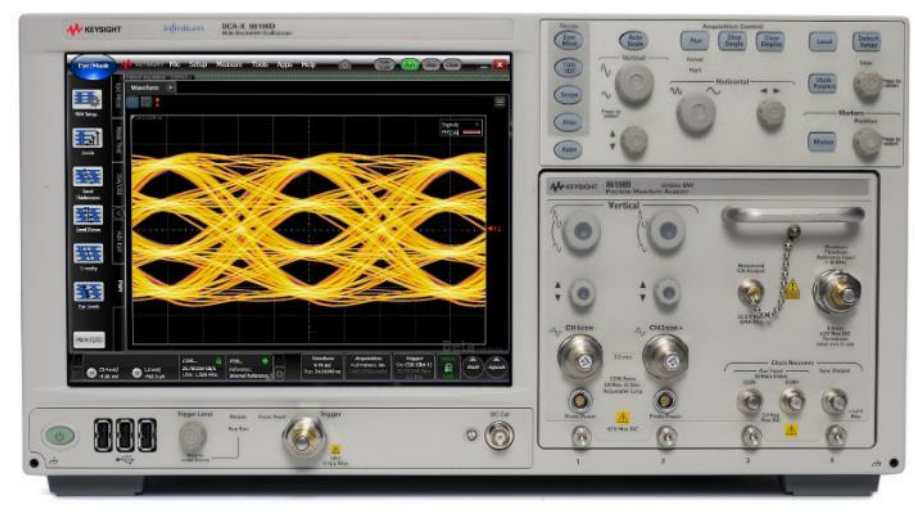
PAM4 is a next generation multilevel signaling architecture



# PAM4 – How Do I Measure it?

## Traditional Method

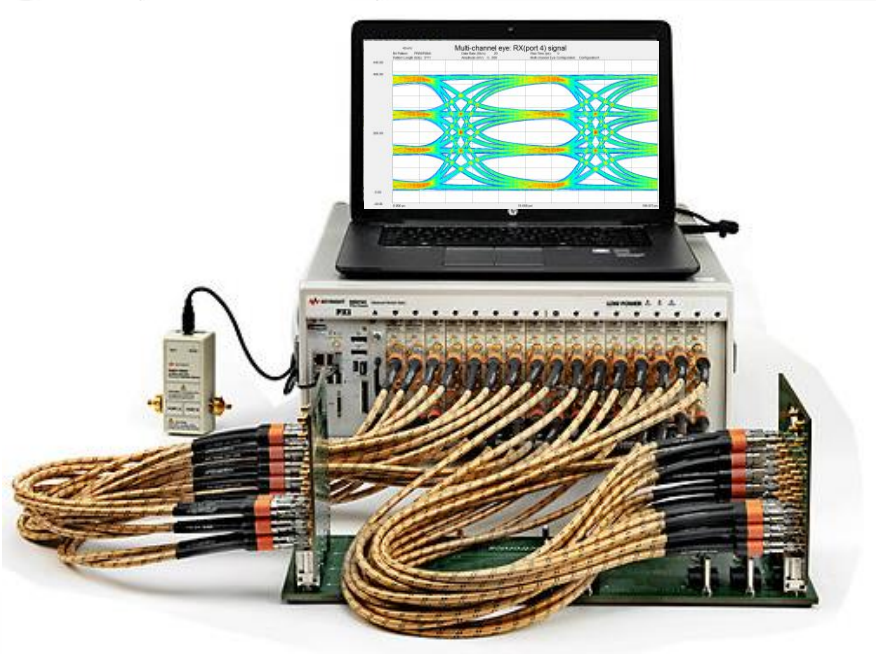
- PRBS pattern generator
- Drive DUT
- Measure w/Scope



86100D Digital Communications Analyzer

## Newer Method

- Measure s-parameters of DUT w/VNA
- Synthesize PAM4 mathematically



N1930B Physical Layer Test System

# De-Embedding Techniques Applied to 56G PAM4 Signals

**Introduction to Hyperscale Data Centers**
- Trends
- Technical Issues

**De-embedding Methods**
- Types of Error Correction
- Automatic Fixture Removal
- Before and After Comparison

**PAM4 Analysis**
- Why needed?
- Compare to NRZ

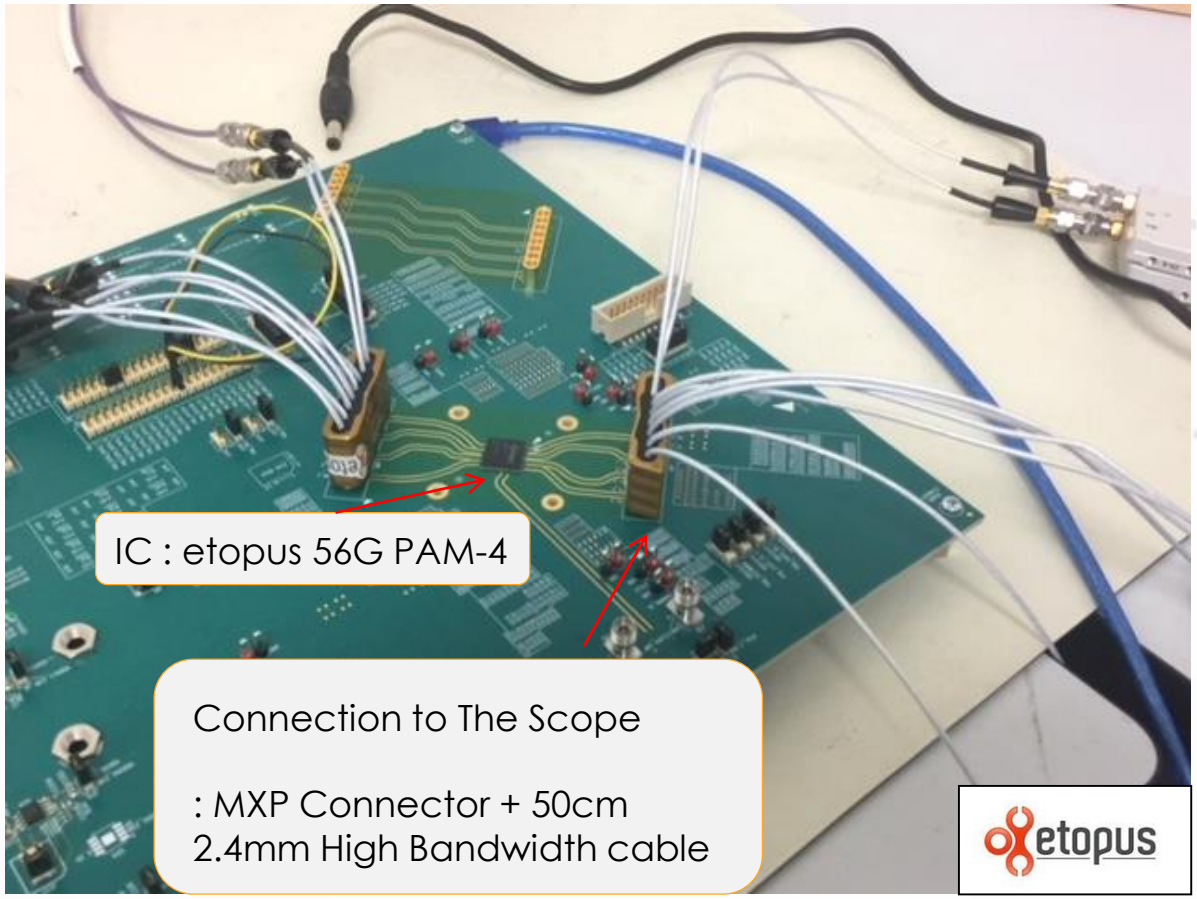
**Design Case Study #1**
- 56G PAM4 Channel

**Design Case Study #2**
- PCI-E Memory Bus Test Fixture

**Conclusion**

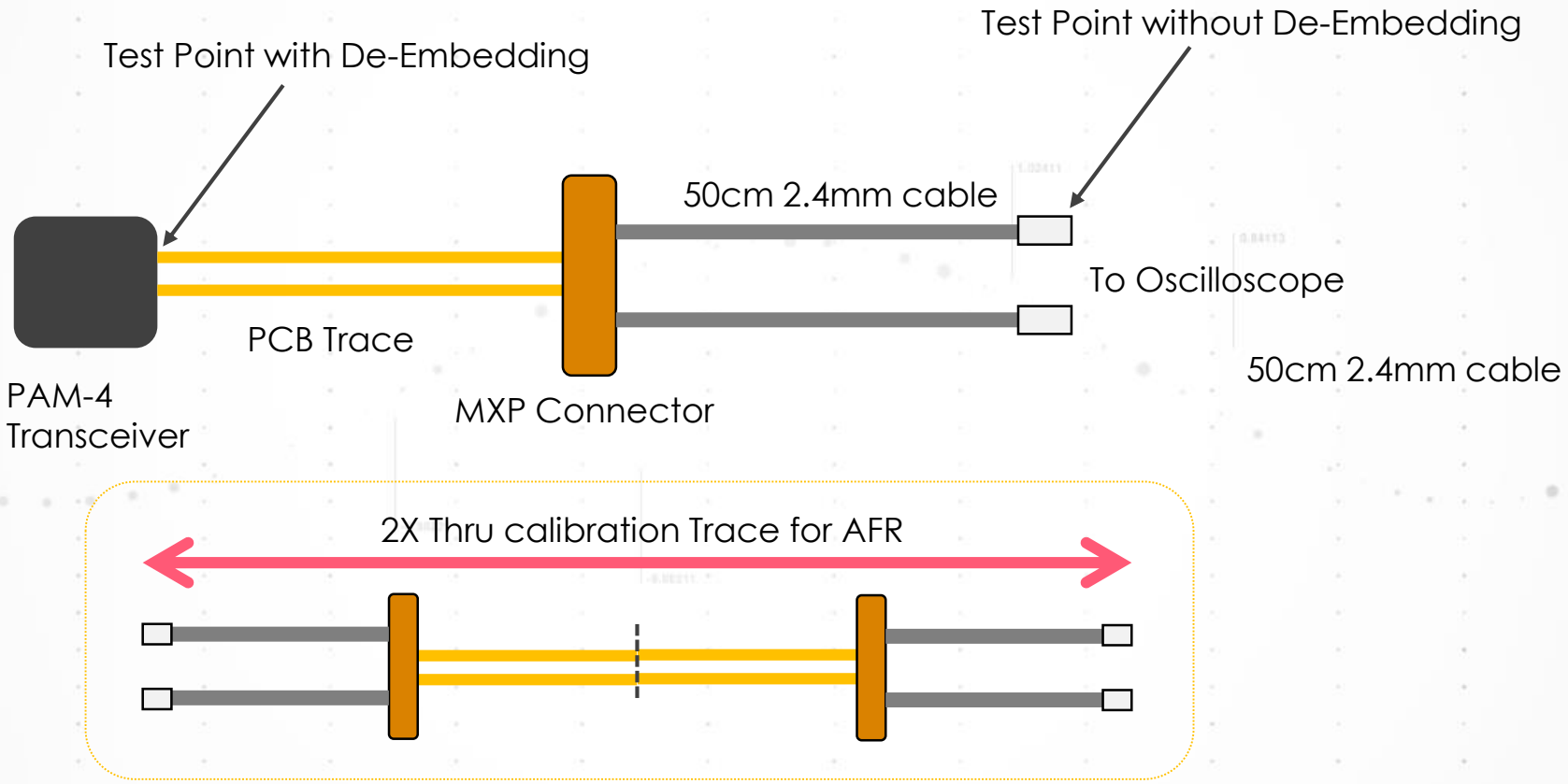
# Case Study for 56G PAM-4 Channel* (AFR 2X THRU Method)

## IC Evaluation Board




* Device Under Test courtesy of Etopus Company

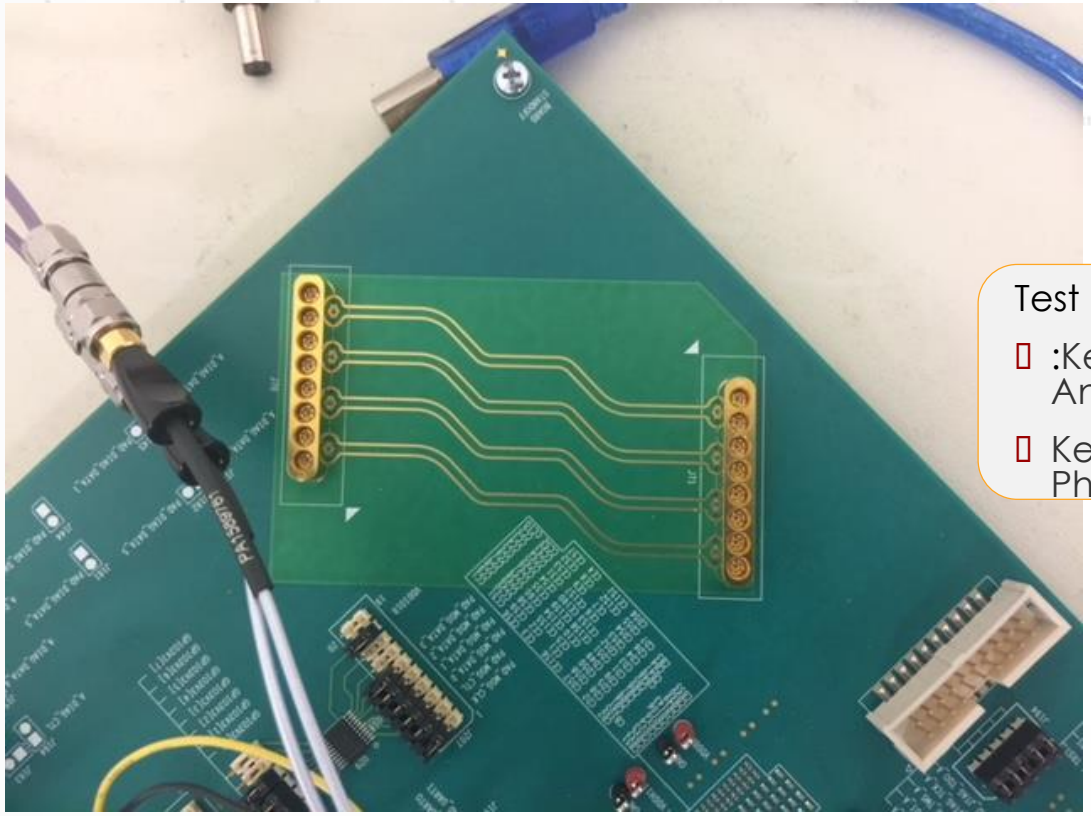
# Design Case Study for 56G PAM-4 Channel




Example: PAM4 PHY supporting 50/100/200/400 GbE Copper Interconnects for Hyperscale & Enterprise Data Centers

# Case Study for 56G PAM-4 Channel

## 2X Thru Replica Trace



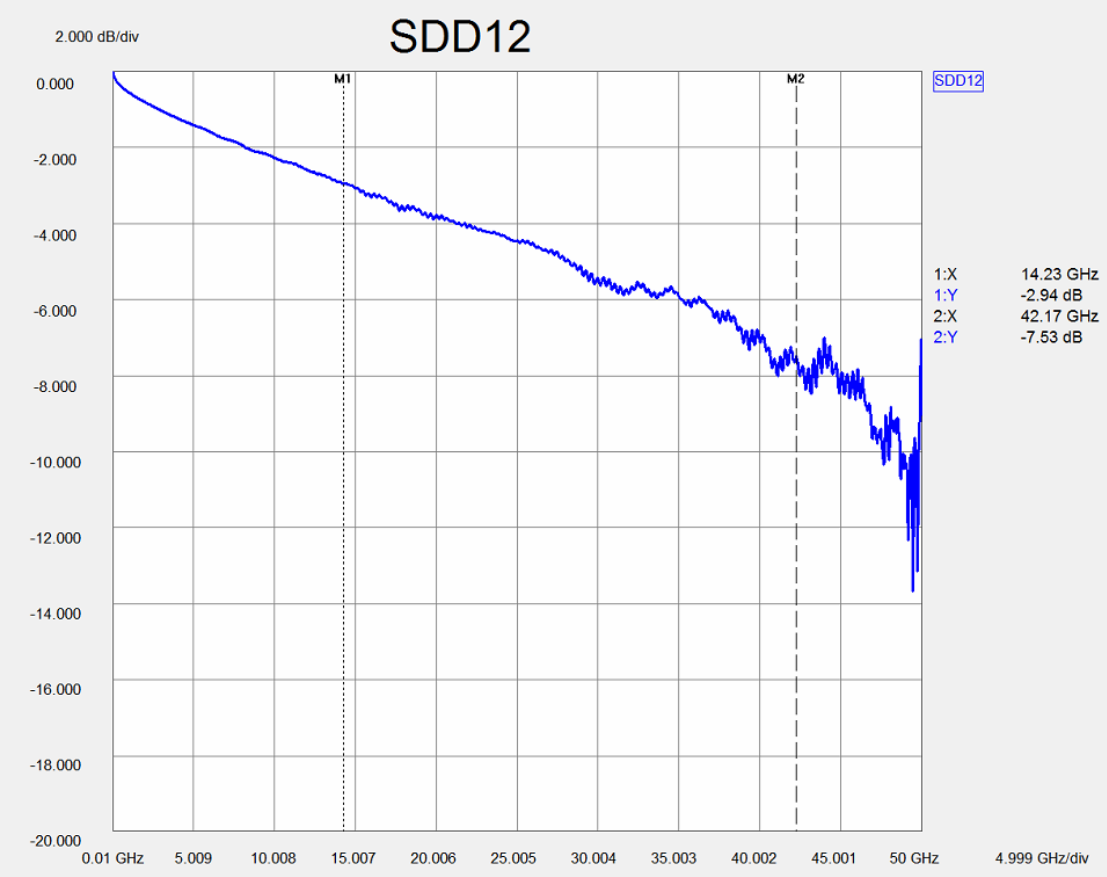
Extract S-parameter with 2.4mmm high bandwidth cable connected to MXP connector.

Test Equipment

- :Keysight N5225A Network Analyzer
- Keysight PLTS (N1930B Physical Layer Test System)

# Case Study for 56G PAM-4 Channel

De-Embed Model Extracted By AFR / Insertion Loss

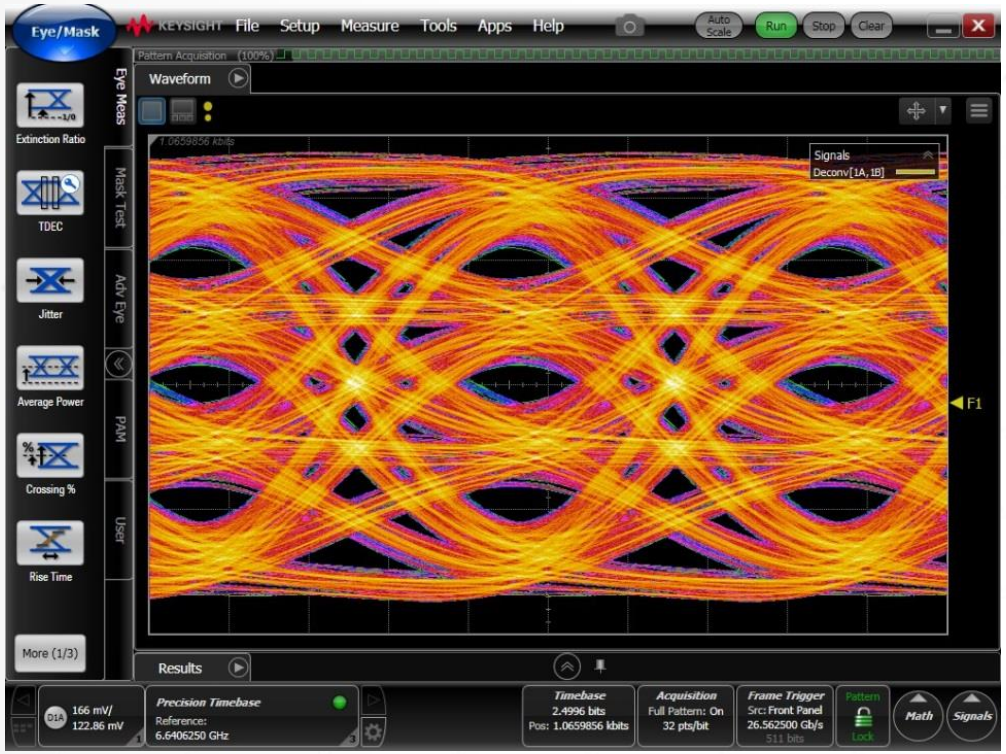



1X AFR model extracted using AFR

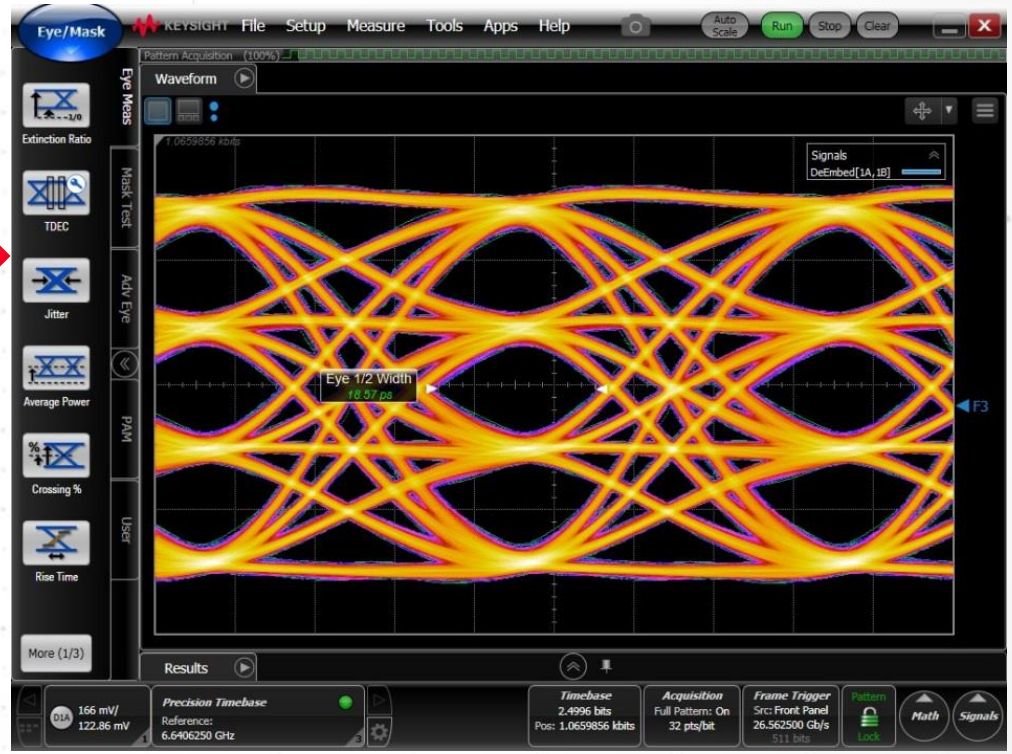
# Case Study for 56G PAM-4 Channel

PAM-4 Waveform Before/After De-Embedding

**BEFORE**




**AFTER**




**Excellent Waveform !**

This is true IC performance.

# Conclusion

- De-Embedding is very effective to analyze true signal characteristics in composite measurement especially for ultra high speed and complex signaling such as 56G PAM-4.
- Even if high quality connector and cable are used, the effect from those components are not negligible in 56G PAM-4. Channel analysis and modeling for the system is very important.

# How to Make Accurate Signal Integrity Measurements

## Measurement

**Prepare instrument for measurement**
- Calibration
- Fixture removal

**Acquire channel data**
- Multi-port S-parameter measurement

**Analyze channel performance**
- Single-ended vs. differential
- Eye diagrams (NRZ, PAM4),
- COM

## Demo

**Conclusion**
- What next?
- Future trends
- Resources

**Live Demo**
- Design case study
- Complete channel analysis
- TDR, PAM4 eye diagram, etc

**Q&A**

# Next Steps in the Design Flow

- Now we have accurate s-parameters, so what now?
  - Prepare data for analysis
  - Dissect the channel data
  - Explore the design space
  - Extract Dk, Loss/in/GHz
  - Analyze TDR impedance profile
  - Single Pulse Response
  - Correlate measurements/models

# Conclusion

- Accurate VNA measurements require an understanding of calibration and error correction
- Various hardware and software configurations can optimize your time in the measurement lab
- De-embedding is necessary to obtain true DUT measurement
- Viewing the measured data in different domains reveals a lot more information
- Overall, given proper measurement, analysis and simulation tools, you will be able to extract the material properties, create a channel model and optimize your channel for high speed

**Thank You**

# Resources

- Physical Layer Test System Home: www.keysight.com/find/plts
- Digital Interconnect Test System: www.keysight.com/find/diref
- Free Signal Integrity Book: www.keysight.com/find/RessoBook

S-parameters: Signal Integrity Analysis in the Blink of an Eye

https://tinyurl.com/ycmbvbgx

N1930B Physical Layer Test System (PLTS) | Keysight

Keysight Network Analyzers • 1/4 videos

https://tinyurl.com/y7prscu2

Tim's Blackboard

https://community.keysight.com/people/timwanglee/content

# Optimizing Signal Integrity Flow Chart

## Theory

**Overview**

- Brief history
- Internet infrastructure

**Transmission Lines**

- Differential impedance
- Multi-port S-parameters

**Measurement Metrics**

- Single-ended vs. differential
- Eye diagrams (NRZ, PAM4),

## Practical

**Typical PCB Issues**

- Vias, reflections, loss
- De-embedding

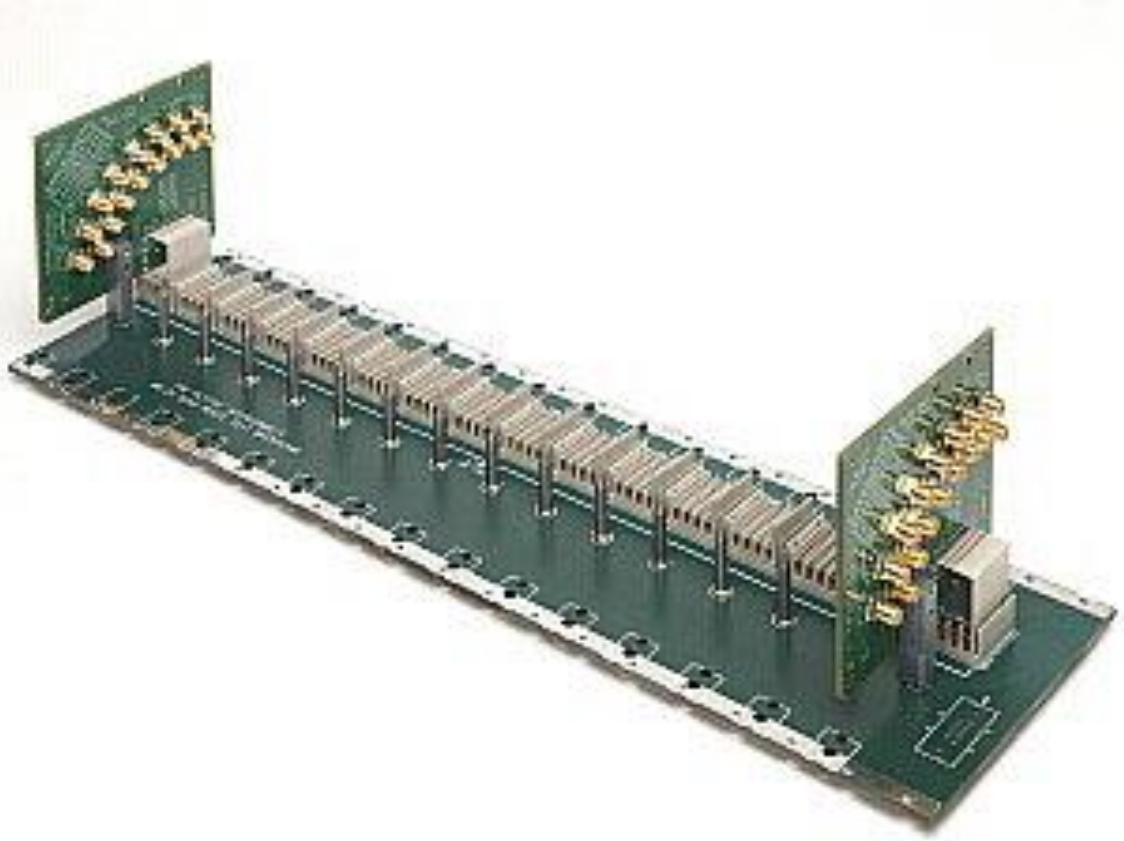
**Real World Measurements**

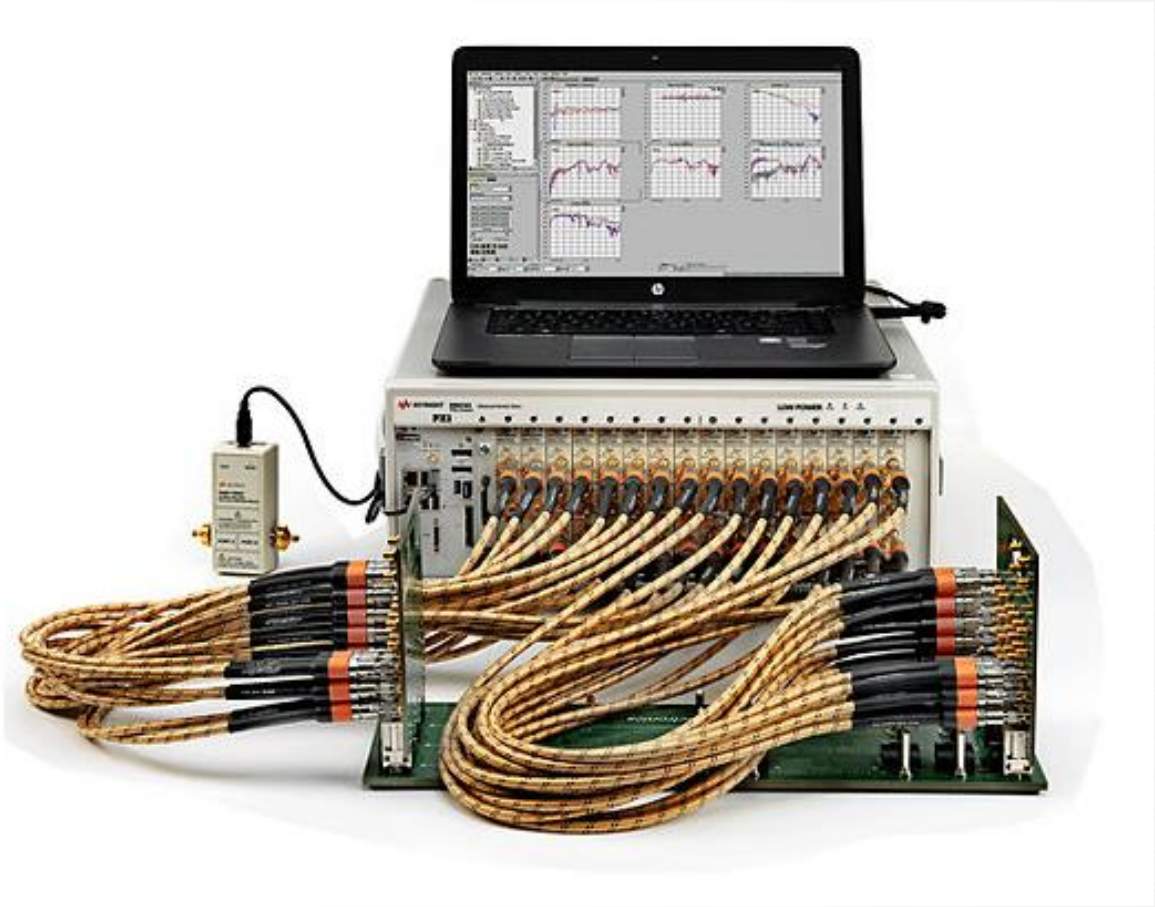
- Backplane Design Case Study

**Demonstration**

- Physical Layer Test System (PLTS)
- USB 3.0 compliance example

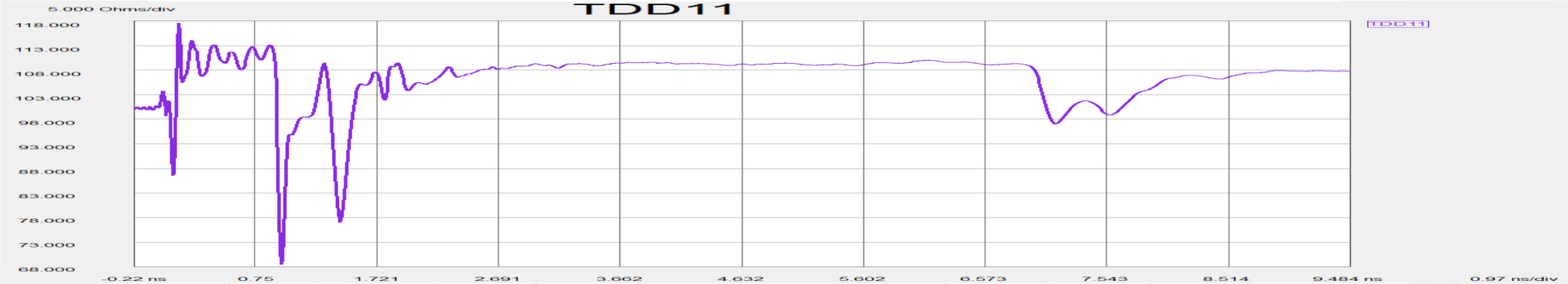
# High Speed Backplane Design Case Study



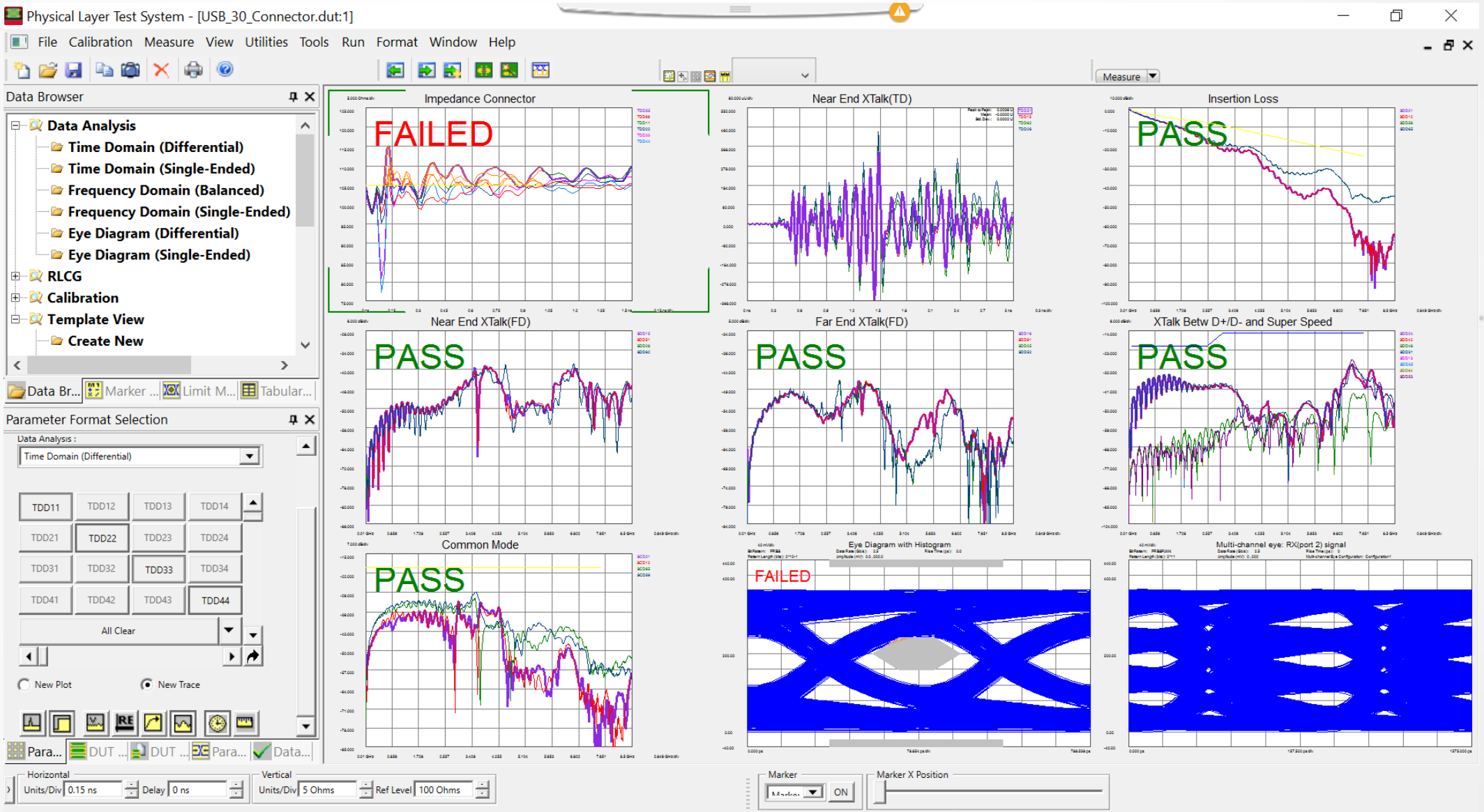


XAUI – e**X**tended **A**ttachment **U**nit **I**nterface

# High Speed Backplane Impedance Profile



# Complete Channel Analysis with PLTS: USB 3.0 Connector




KEYSIGHT TECHNOLOGIES

# PLTS USB 3.0 Demo Slide